

EiceDRIVER™ SIL

High Voltage IGBT Driver for Automotive Applications

1EDI2001AS

Single Channel Isolated Driver for Inverter Systems
AD Step

Datasheet

Hardware Description
Rev. 3.1, 2015-07-30

Edition 2015-07-30

**Published by
Infineon Technologies AG
81726 Munich, Germany**

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Revision History

| Page or Item | Subjects (major changes since previous revision) |
|----------------------------|---|
| Rev 2.2, 2014-07-25 | |
| Page 11 | Updated SP Number |
| Page 28 | Added note: "the contents of a frame..." |
| Page 28 | Added note: "in case of permanent..." |
| Page 42 | Added note: "the Pulse suppressor..." |
| Page 49 | Corrected Table 2-14 |
| Page 51 | Updated Chapter 2.4.10.1.9 |
| Page 51 | Updated Chapter 2.4.10.1.11 . |
| Page 76 | Update PID value. |
| Page 79 | Updated reset value of register PSTAT2 . |
| Page 93 | Update SID value. |
| Page 94 | Correct SSTAT definition of bits 15 and 14 to rh. |
| Page 106 | Updated definition of bit field DSATBT . |
| Page 107 | Updated definition of bit field OCGBT . |
| Page 116 | Updated Table 5-1 |
| Page 118 | Updated Figure 5-1 |
| Page 119 | Corrected Table 5-2 |
| Page 120 | Updated footnote ²⁾ in Table 5-3 . |
| Page 120 | Updated value $R_{thjcbot}$ in Table 5-4 |
| Page 121 | Updated parameters V_{UVLO2} and V_{OVLO2} in Table 5-5 . |
| Page 122 | Updated parameter f_{clk1} in Table 5-6 |
| Page 123 | Updated parameters R_{PDIN1} and I_{INPR1} in Table 5-7 |
| Page 125 | Updated parameters R_{PDIN2} and updated parameter R_{PDOSD2} in Table 5-13 |
| Page 127 | Updated parameters V_{GPON0} , V_{GPON1} , V_{GPON2} , t_{PDISTO} , V_{GPOF15} in Table 5-17 |
| Page 129 | Updated parameters $R_{PUDESAT2}$, V_{DESAT0} in Table 5-18 |
| Page 129 | Updated parameter R_{PUOCP2} in Table 5-19 |
| Page 131 | Updated parameter t_{DEAD} , $t_{OFFDESAT2}$ in Table 5-21 |
| Page 132 | Updated parameter t_{FSCLK} , removed parameter t_{SCLKp} Table 5-22 |

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1EDI2001AS

1 Product Definition

1.1 Overview

The 1EDI2001AS is a high-voltage IGBT gate driver designed for automotive motor drives above 5 kW. The 1EDI2001AS is based on Infineon's Coreless Transformer (CLT) technology, providing galvanic insulation between low voltage and high voltage domains. The device has been designed to support 400 V, 600 V and 1200 V IGBT technologies.

The 1EDI2001AS can be connected on the low voltage side ("primary" side) to 5 V logic. A standard SPI interface allows the logic to configure and to control the advanced functions implemented in the driver.

On the high voltage side ("secondary" side), the 1EDI2001AS is dimensioned to drive an external booster stage. Short propagation delays and controlled internal tolerances lead to minimal distortion of the PWM signal.

A large panel of safety-related functions has been implemented in the 1EDI2001AS, in order to support functional safety requirements at system level (as per ISO 26262). Besides, those integrated features ease the implementation of Active Short Circuit (ASC) strategies.

The 1EDI2001AS can be used optimally with Infineon's 1EBN100XAE "EiceDRIVER™ Boost" booster stage family.



1.2 Feature Overview

The following features are supported by the 1EDI2001AS:

Functional Features

- Single Channel IGBT Driver.
- On-chip galvanic insulation (up to 6kV).
- Support of 600 V and 1200 V IGBT technologies.
- Low propagation delay and minimal PWM distortion.
- Support of 5 V logic levels (primary side).
- 16-bit Standard SPI interface (up to 2 Mbaud) with daisy chain support (primary side).
- Enable input pin (primary side).
- Pseudo-differential inputs for critical signals (primary side).
- Power-On Reset pin (primary side).
- Debug mode.
- Pulse Suppressor.

| Product Name | Ordering Code | Package |
|--------------|---------------|-----------|
| 1EDI2001AS | SP001361862 | PG-DSO-36 |

- Fully Programmable Active Clamping Inhibit signal (secondary side).
- Optimal support of EiceBoost functions.
- 36-pin PG-DSO-36 green package.
- Automotive qualified (as per AEC Q100).

Safety Relevant Features

- Desaturation monitoring.
- Overcurrent protection.
- Fully programmable Two-Level Turn-Off.
- Automatic Emergency Turn-Off in failure case.
- Automatic or externally triggered disabling of the output stage (tristate).
- Under- and over-voltage supervision of all the power supplies (both primary and secondary sides).
- NFLTA and NFLTB notification pins for fast system response time (primary side).
- Safe internal state machine.
- Weak Turn-On functionality.
- Internal overtemperature sensor (secondary side).
- Internal clock monitoring.
- Gate signal monitoring.
- Individual error and status flags readable via SPI.
- Support for Active Short Circuit strategies.
- Full diagnosticability.
- In-application testability of safety critical functions.
- Suitable for systems up to ASIL D requirements (as per ISO 26262).

1.3 Target Applications

- Inverters for automotive Hybrid Electric Vehicles (HEV) and Electric Vehicles (EV).
- High Voltage DC/DC converter.
- Industrial Drive.

2 Functional Description

2.1 Introduction

The 1EDI2001AS is an advanced single channel IGBT driver that can also be used for driving power MOS devices. The device has been developed in order to optimize the design of high performance safety relevant automotive systems.

The device is based on Infineon's Coreless Transformer Technology and consist of two chips separated by a galvanic isolation. The low voltage (primary) side can be connected to a standard 5 V logic. The high voltage (secondary) side is in the DC-link voltage domain.

Internally, the data transfers are ensured by two independent communication channels. One channel is dedicated to transferring the ON and OFF information of the PWM input signal only. This channel is unidirectional (from primary to secondary). Because this channel is dedicated to the PWM information, latency time and PWM distortion are minimized. The second channel is bidirectional and is used for all the other data transfers (e.g. status information, etc).

The 1EDI2001AS supports advanced functions in order to optimize the switching behavior of the IGBT. Furthermore, it supports several monitoring and protection functions, making it suitable for systems having to fulfill ASIL requirements (as per ISO 26262).

2.2 Pin Configuration and Functionality

2.2.1 Pin Configuration

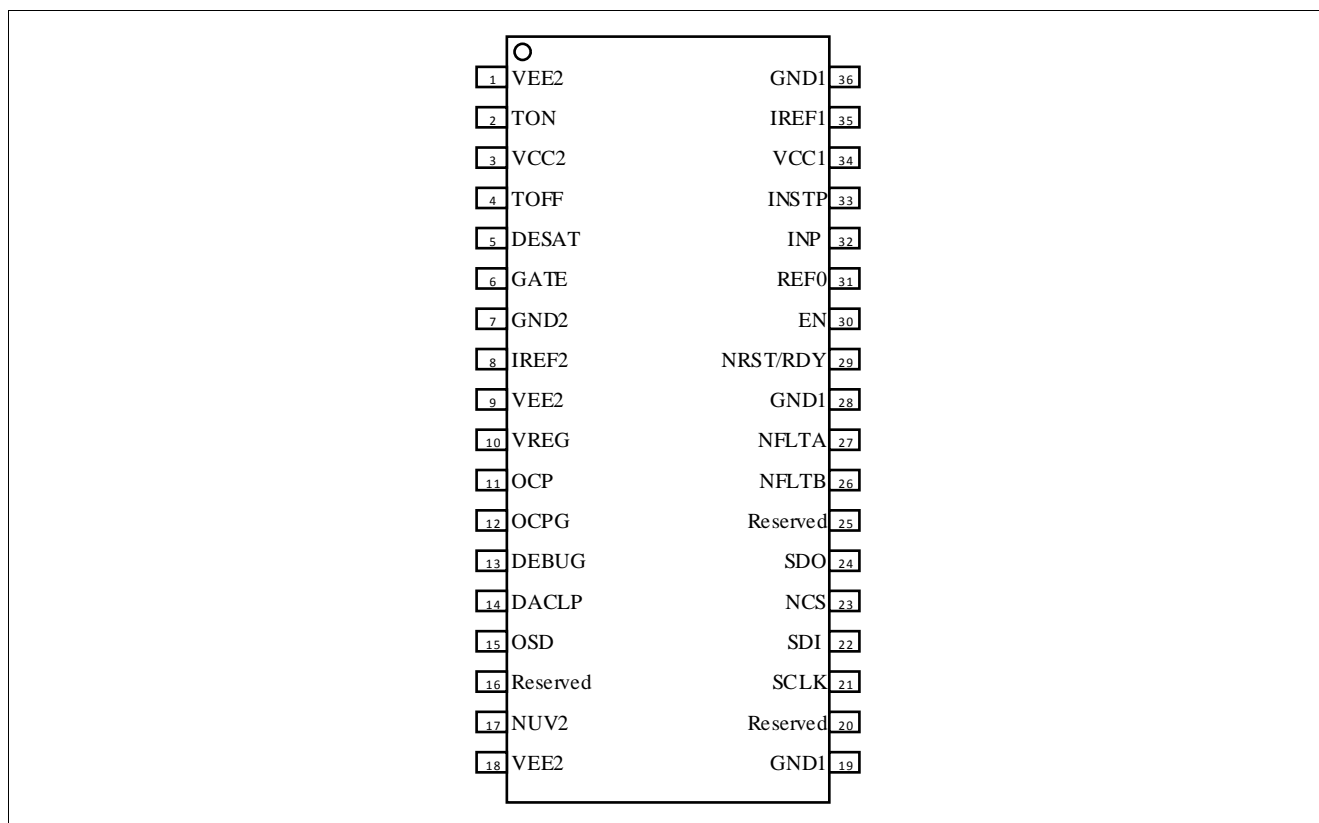


Figure 2-1 Pin Configuration

Table 2-1 Pin Configuration

| Pin Number | Symbol | I/O | Voltage Class | Function |
|------------|--------|--------|---------------|---------------------------------------|
| 1,9,18 | VEE2 | Supply | Supply | Negative Power Supply ¹⁾ . |
| 2 | TON | Output | 15V Secondary | Turn-On Output. |
| 3 | VCC2 | Supply | Supply | Positive Power Supply. |
| 4 | TOFF | Output | 15V Secondary | Turn-Off Output. |
| 5 | DESAT | Input | 15V Secondary | Desaturation Protection Input. |
| 6 | GATE | Input | 15V Secondary | Gate Monitoring Input. |
| 7 | GND2 | Ground | Ground | Ground. |
| 8 | IREF2 | Input | 5V Secondary | External Reference Input. |
| 10 | VREG | Output | 5V Secondary | Reference Output Voltage. |
| 11 | OCP | Input | 5V Secondary | Over Current Protection. |
| 12 | OCPG | Ground | Ground | Ground for the OCP function, |
| 13 | DEBUG | Input | 5V Secondary | Debug Input. |

Functional Description
Table 2-1 Pin Configuration (cont'd)

| Pin Number | Symbol | I/O | Voltage Class | Function |
|------------|----------|--------------|---------------|--|
| 14 | DACLP | Output | 5V Secondary | Active Clamping Disable Output. |
| 15 | OSD | Input | 5V Secondary | Output Stage Disable Input. |
| 16 | Reserved | Reserved | Reserved | Reserved. This pin shall be connected to GND2 . |
| 17 | NUV2 | Output | 5V Secondary | V _{CC2} not valid notification output. |
| 19, 28, 36 | GND1 | Ground | Ground | Ground ²⁾ . |
| 20 | Reserved | Reserved | Reserved | Reserved. This pin shall be connected to GND1 . |
| 21 | SCLK | Input | 5V Primary | SPI Serial Clock Input. |
| 22 | SDI | Input | 5V Primary | SPI Serial Data Input. |
| 23 | NCS | Input | 5V Primary | SPI Chip Select Input (low active). |
| 24 | SDO | Output | 5V Primary | SPI Serial Data Output. |
| 25 | Reserved | Reserved | Reserved | Reserved. This pin shall be connected to GND1 . |
| 26 | NFLT B | Output | 5V Primary | Fault B Output (low active, open drain). |
| 27 | NFLT A | Output | 5V Primary | Fault A Output (low active, open drain). |
| 29 | NRST/RDY | Input/Output | 5V Primary | Reset Input (low active, open drain). This signal notifies that the device is "ready". |
| 30 | EN | Input | 5V Primary | Enable Input. |
| 31 | REF0 | Ref. Ground | Ground | Reference Ground for signals INP , INSTP , EN . |
| 32 | INP | Input | 5V Primary | Positive PWM Input. |
| 33 | INSTP | Input | 5V Primary | Monitoring PWM Input. |
| 34 | VCC1 | Supply Input | Supply | Positive Power Supply. |
| 35 | IREF1 | Input | 5V Primary | External Reference Input. |

1) All **VEE2** pins must be connected together.

2) All **GND1** pins must be connected together.

2.2.2 Pin Functionality

2.2.2.1 Primary Side

GND1

Ground connection for the primary side.

VCC1

5V power supply for the primary side (referring to GND1).

INP

Non-inverting PWM input of the driver. The internal structure of the pad makes the IC robust against glitches. An internal weak pull-down resistor to V_{REF0} drives this input to Low state in case the pin is floating.

INSTP

Monitoring PWM input for shoot through protection. The internal structure of the pad makes the IC robust against glitches. An internal weak pull-down resistor to V_{REF0} drives this input to Low state in case the pin is floating.

REF0

Reference Ground signal for the signals **INP**, **INSTP**, **EN**. This pin should be connected to the ground signal of the logic issuing those signals.

EN

Enable Input Signal. This signal allows the logic on the primary side to turn-off and deactivate the device. An internal weak pull-down resistor to V_{REF0} drives this input to Low state in case the pin is floating. This pin reacts on logic levels.

NFLTA

Open-Drain Output signal used to report major failure events (Event Class A). In case of an error event, **NFLTA** is driven to Low state. This pin shall be connected externally to V_{CC1} with a pull-up resistance.

NFLTB

Open-Drain Output signal used to report major failure events (Event Class B). In case of an error event, **NFLTB** is driven to Low state. This pin shall be connected externally to V_{CC1} with a pull-up resistance.

SCLK

Serial Clock Input for the SPI interface. An internal weak pull-up device to V_{CC1} drives this input to high state in case the pin is floating.

SDO

Serial Data Output (push-pull) or the SPI interface.

SDI

Serial Data Input for the SPI interface. An internal weak pull-up device to V_{CC1} drives this input to high state in case the pin is floating.

NCS

Chip Select input for the SPI interface. This signal is low active. An internal weak pull-up device to V_{CC1} drives this input to High state in case the pin is floating.

IREF1

Reference input of the primary chip. This pin shall be connected to V_{GND1} via an external resistor.

NRST/RDY

Open drain reset input. This signal is low-active. When a valid signal is received on this pin, the device is brought in its default state. This signal is also used as a “ready notification”. A high level on this pin indicates that the primary chip is functional.

2.2.2.2 Secondary Side**VEE2**

Negative power supply for the secondary side, referring to V_{GND2} .

VCC2

Positive power supply for the secondary side, referring to V_{GND2} .

GND2

Reference ground for the secondary side.

DESAT

Desaturation Protection input pin. The function associated with this pin monitors the V_{CE} voltage of the IGBT. An internal pull-up resistor to V_{CC2} drives this signal to High level in case it is floating.

OCP

Over Current Protection input pin. The function associated with this pin monitors the voltage across a sensing resistance located on the auxiliary path of a Current Sense IGBT. An internal weak pull-up resistor to the internal 5V reference drives this input to High state in case the pin is floating.

OCPG

Over Current Protection Ground.

TON

Output pin for turning on the IGBT.

TOFF

Output pin for turning off the IGBT.

GATE

Input pin used to monitor the IGBT gate voltage.

OSD

Output Stage Disable input. A High Level on this pin tristates the output stage. An internal weak pull-down resistor to V_{GND2} drives this input to Low state in case the pin is floating.

DACL

Output pin used to disable the active clamping function of the booster.

DEBUG

Debug input pin. This pin is latched at power-up. When a High level is detected on this pin, the device enters a special mode where it can be operated without SPI interface. This feature is for development purpose only. This pin should normally be tied to V_{GND2} . An internal weak pull-down resistor to V_{GND2} drives this input to Low state in case the pin is floating.

IREF2

Reference input of the secondary chip. This pin shall be connected to V_{GND2} via an external resistor.

VREG

Reference Output voltage. This pin shall be connected to an external capacitance to V_{GND2} .

NUV2

V_{CC2} not valid notification signal (Open Drain). This signal drives a low level when V_{CC2} is not valid or when the internal 5V digital supply is not valid. When both supplies are valid, this pin is in high impedance state. This pin shall be connected externally to a 5V reference with a pull-up resistance.

2.2.2.3 Pull Devices

Some of the pins are connected internally to pull-up or pull-down devices. This is summarized in [Table 2-2](#).

Table 2-2 Internal pull devices

| Signal | Device |
|--------------|---------------------------------------|
| INP | Weak pull down to V_{REF0} |
| INSTP | Weak pull down to V_{REF0} |
| EN | Weak pull down to V_{REF0} |
| SCLK | Weak pull up to V_{CC1} |
| SDI | Weak pull up to V_{CC1} |
| NCS | Weak pull up to V_{CC1} |
| DESAT | Weak pull up to V_{CC2} |
| OSD | Weak pull down to V_{GND2} |
| OCP | Weak pull up to 5V internal reference |
| DEBUG | Weak pull down to V_{GND2} |

2.3 Block Diagram

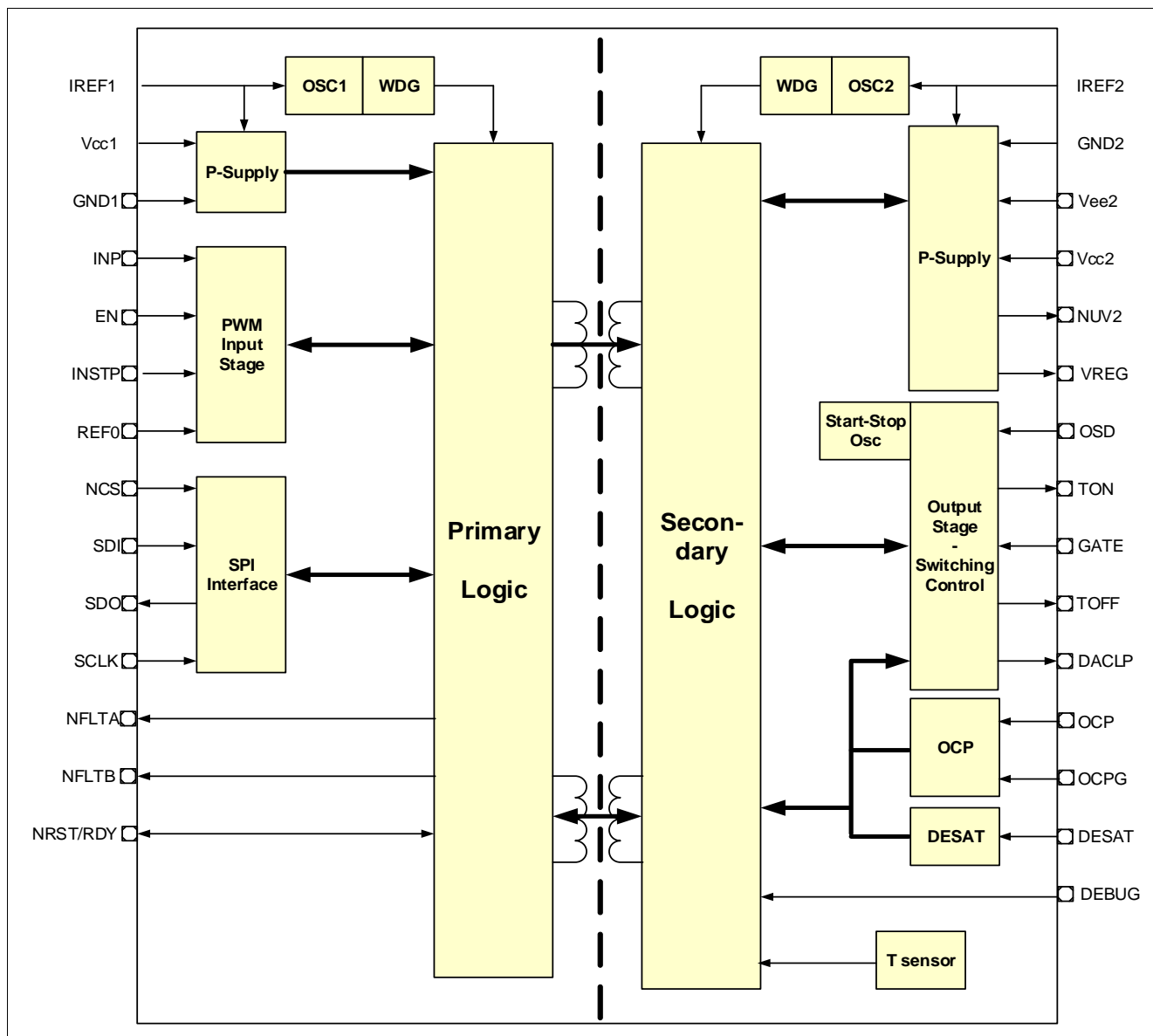


Figure 2-2 Block Diagram

2.4 Functional Block Description

2.4.1 Power Supplies

On the primary side, the 1EDI2001AS needs a single 5 V supply source V_{CC1} for proper operation. This makes the device compatible to most of the microcontrollers available for automotive applications.

On the secondary side, the 1EDI2001AS needs two power supplies for proper operation.

- The positive power supply V_{CC2} is typically set to 15 V (referring to V_{GND2}).
- The negative supply V_{EE2} is typically set to -8 V (referring to V_{GND2}).

Under- and over-voltage monitoring is performed continuously during operation of the device (see [Chapter 3.3.1](#)).

A 5V supply for the digital domain on the secondary side is generated internally (present at pin **VREG**).

2.4.2 Clock Domains

The clock system of the 1EDI2001AS is based on three oscillators defining each a clock domain:

- One RC oscillator (OSC1) for the primary chip.
- One RC oscillator (OSC2) for the secondary chip excepting the output stage.
- One Start-Stop oscillator (SSOSC2) for the output stage on the secondary side.

The two RC oscillators are running constantly. They are also monitored constantly, and large deviations from the nominal frequency are identified as a system failure (Event Class B, see [Chapter 3.3.2.2](#)).

The Start Stop oscillator is controlled by the PWM command.

2.4.3 PWM Input Stage

The PWM input stage generates from the external signals **INP**, **INSTP** and **EN** the turn-on and turn-off commands to the secondary side. The general structure of the PWM input block is shown **Figure 2-3**.

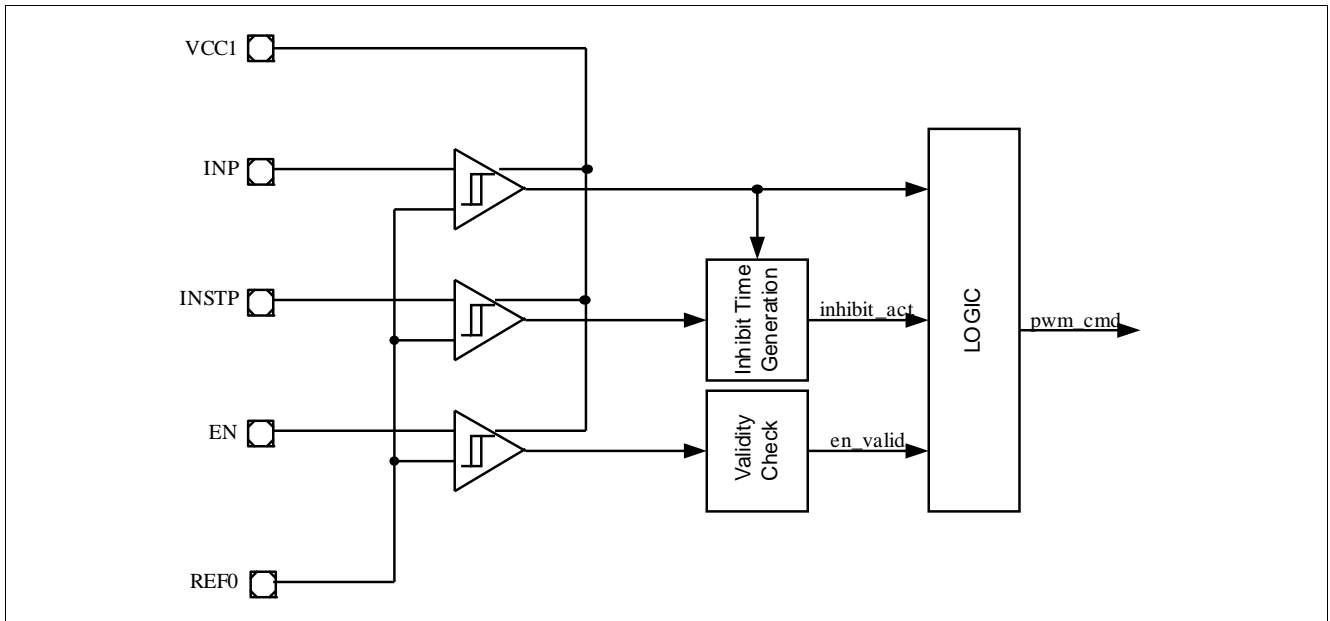


Figure 2-3 PWM Input Stage

Signals **INP**, **INSTP** and **EN** are pseudo-differential, in the sense that they are not referenced to the common ground **GND1** but to signal **REF0**. This is intended to make the device more robust against ground bouncing effects.

*Note: Glitches shorter than t_{INPR1} occurring at signal **INP** are filtered internally.*

*Note: Pulses at **INP** below t_{INPPD} might be distorted or suppressed.*

The 1EDI2001AS supports non-inverted PWM signals only. When a High level on pin **INP** is detected while signals **INSTP** and **EN** are valid, a turn-on command is issued to the secondary chip. A Low level at pin **INP** issues a turn-off command to the secondary chip.

Signal **EN** can inhibit turn-on commands received at pin **INP**. A valid signal **EN** is required in order to have turn-on commands issued to the secondary chip. If an invalid signal is provided, the PWM input stage issues constantly turn-off commands to the secondary chip. The functionality of signal **EN** is detailed in **Chapter 2.4.8**.

*Note: After an invalid-to valid-transition of signal **EN**, a minimum delay of t_{INPEN} should be inserted before turning **INP** on.*

As shown in **Figure 2-4**, signal **INSTP** provides a Shoot-Through Protection (STP) to the system. When signal at pin **INSTP** is at High level, the internal signal `inhibit_act` is activated. The inhibition time is defined as the pulse duration of signal `inhibit_act`. It corresponds to the pulse duration of signal **INSTP** to which a minimum dead time is added. During the inhibition time, rising edges of signal **INP** are inhibited. Bit **PSTAT2.STP** is set for the duration of the inhibition time.

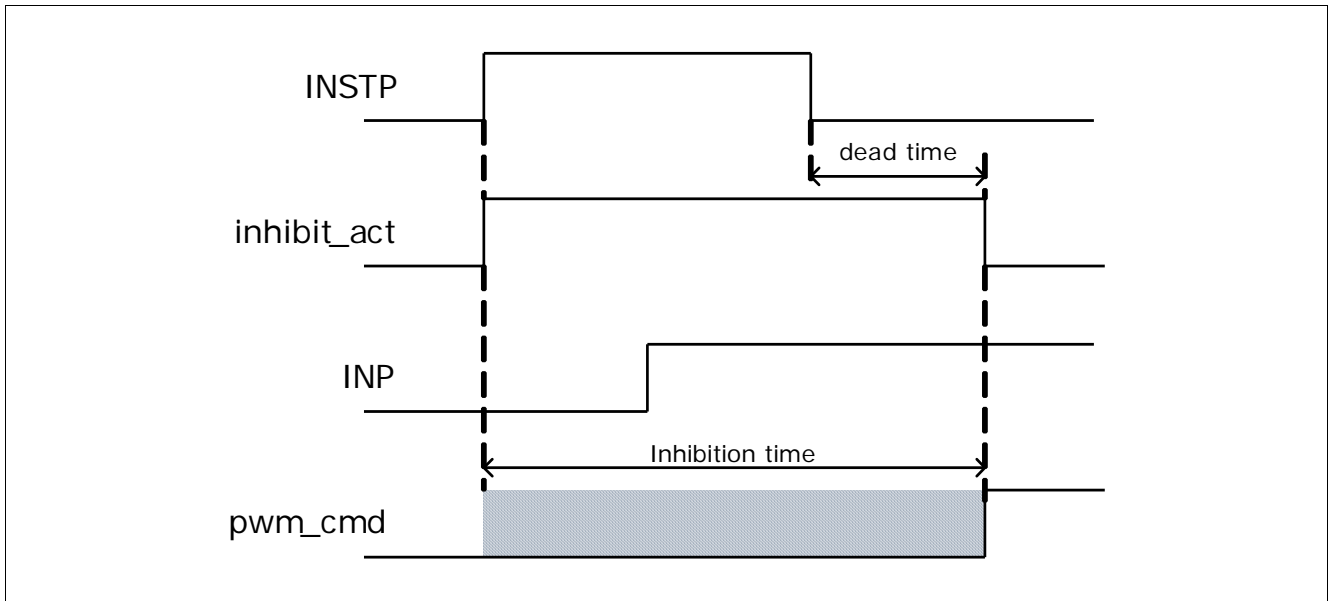


Figure 2-4 STP: Inhibition Time Definition

It shall be noted that during the inhibition time, signal `pwm_cmd` is not forced to Low. It means that if the device is already turned-on when **INSTP** is High, it stays turned-on until the signal at pin **INP** goes Low. This is depicted in [Figure 2-5](#).

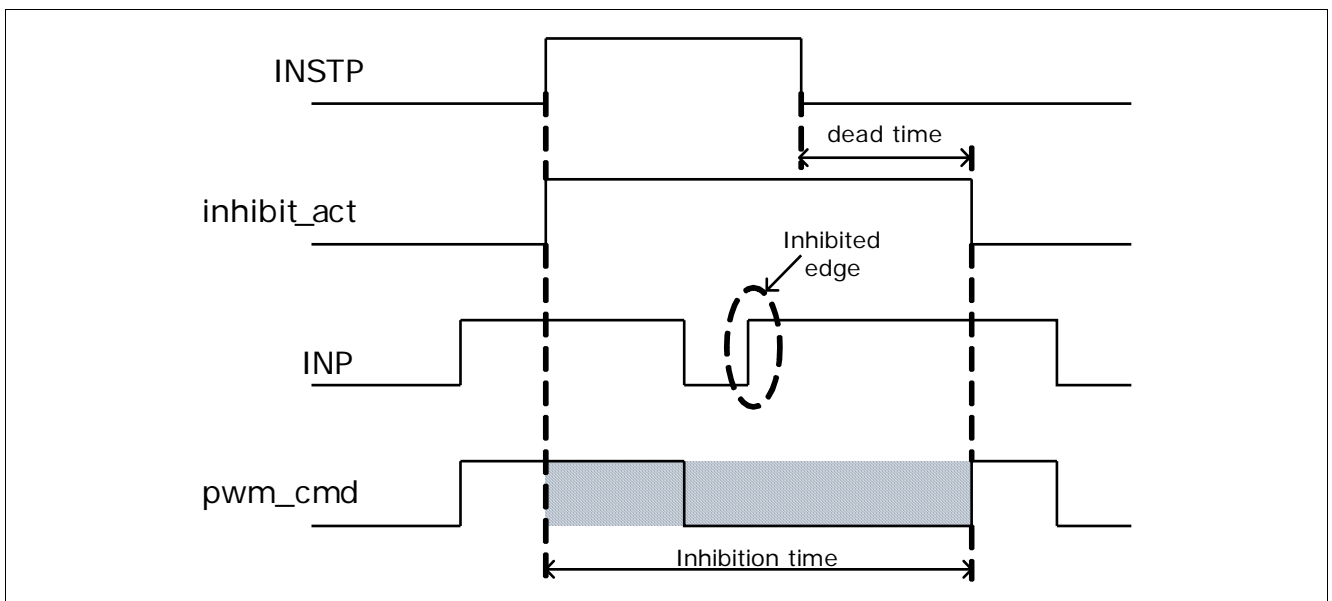


Figure 2-5 STP: Example of Operation

When a condition occurs where a rising edge of signal **INP** is inhibited, an error notification is issued. See [Chapter 3.4.1](#) for more details.

2.4.4 SPI Interface

This chapter describes the functionality of the SPI block.

2.4.4.1 Overview

The standard SPI interface implemented on the 1EDI2001AS is compatible with most of the microcontrollers available for automotive and industrial applications. The following features are supported by the SPI interface:

- Full-duplex bidirectional communication link.
- SPI Slave mode (only).
- 16-bit frame format.
- Daisy chain capability.
- MSB first.
- Parity Check (optional) and Parity Bit generation (LSB).

The SPI interface of the 1EDI2001AS provides a standardized bidirectional communication interface to the main microcontroller. From the architectural point of view, it fulfills the following functions:

- Initialization of the device.
- Configuration of the device (static and runtime).
- Reading of the status of the device (static and runtime).
- Operation of the verification modes of the device.

The purpose of the SPI interface is to exchange data which have relaxed timing constraints compared to the PWM signals (from the point of view of the motor control algorithm). The IGBT switching behavior is for example controlled directly by the PWM input. Similarly, critical application failures requiring fast reaction are notified on the primary side via the feedback signals **NFLTA**, **NFLTB** and **NRST/RDY**.

In order to minimize the complexity of the end-application and to optimize the microcontroller's resources, the implemented interface has daisy chain capability. Several (typically 6) 1EDI2001AS devices can be combined into a single SPI bus.

2.4.4.2 General Operation

The SPI interface of the 1EDI2001AS supports full duplex operation. The interface relies on four communication signals:

- **NCS:** (Not) Chip Select.
- **SCLK:** Serial Clock.
- **SDI:** Serial Data In.
- **SDO:** Serial Data Out.

The SPI interface of the 1EDI2001AS supports slave operation only. An SPI master (typically, the main microcontroller) is connected to one or several 1EDI2001AS devices, forming an SPI bus. Several bus topologies are supported.

A regular SPI bus topology can be used where each of the slaves is controlled by an individual chip select signal (**Figure 2-6**). In this case, the number of slaves on the bus is only limited by the application's constraints.

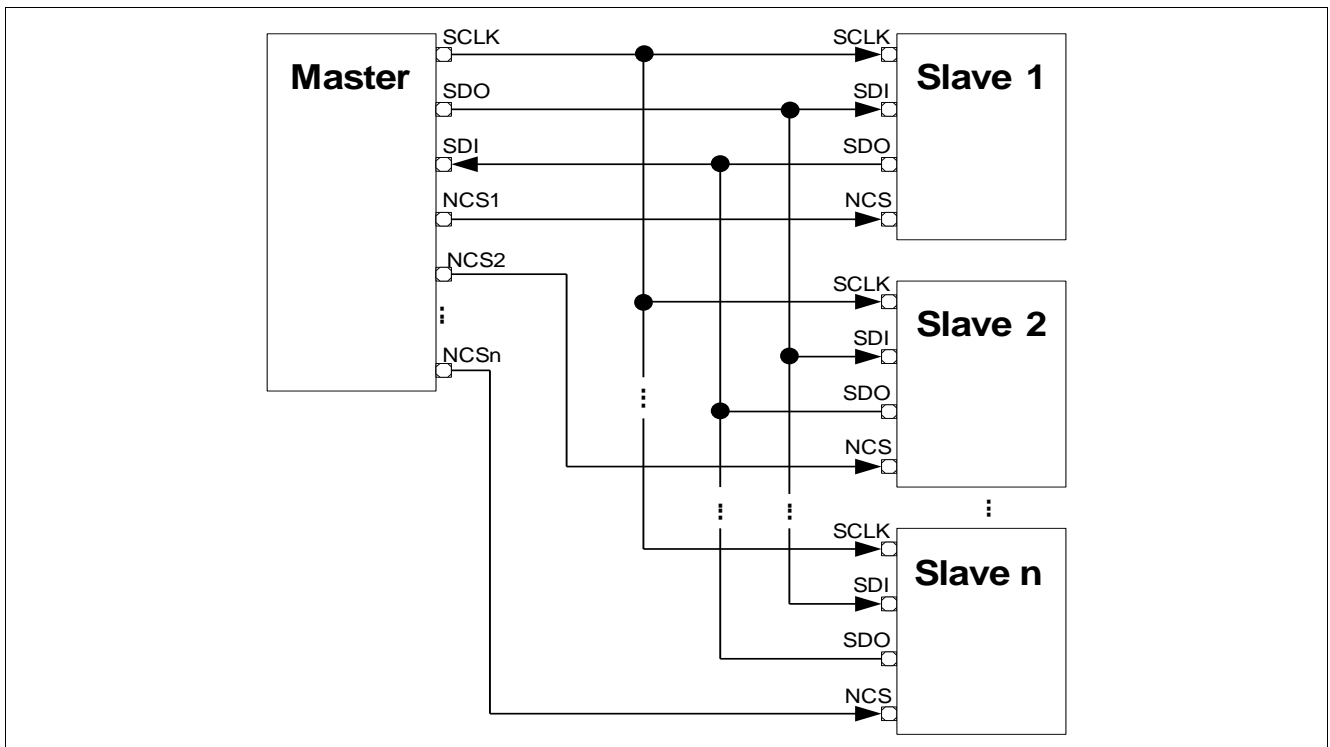


Figure 2-6 SPI Regular Bus Topology

In order to simplify the layout of the PCB and to reduce the number of pins used on the microcontroller's side, a daisy chain topology can also be used. The chain's depth is not limited by the 1EDI2001AS itself. A possible topology is shown **Figure 2-7**.

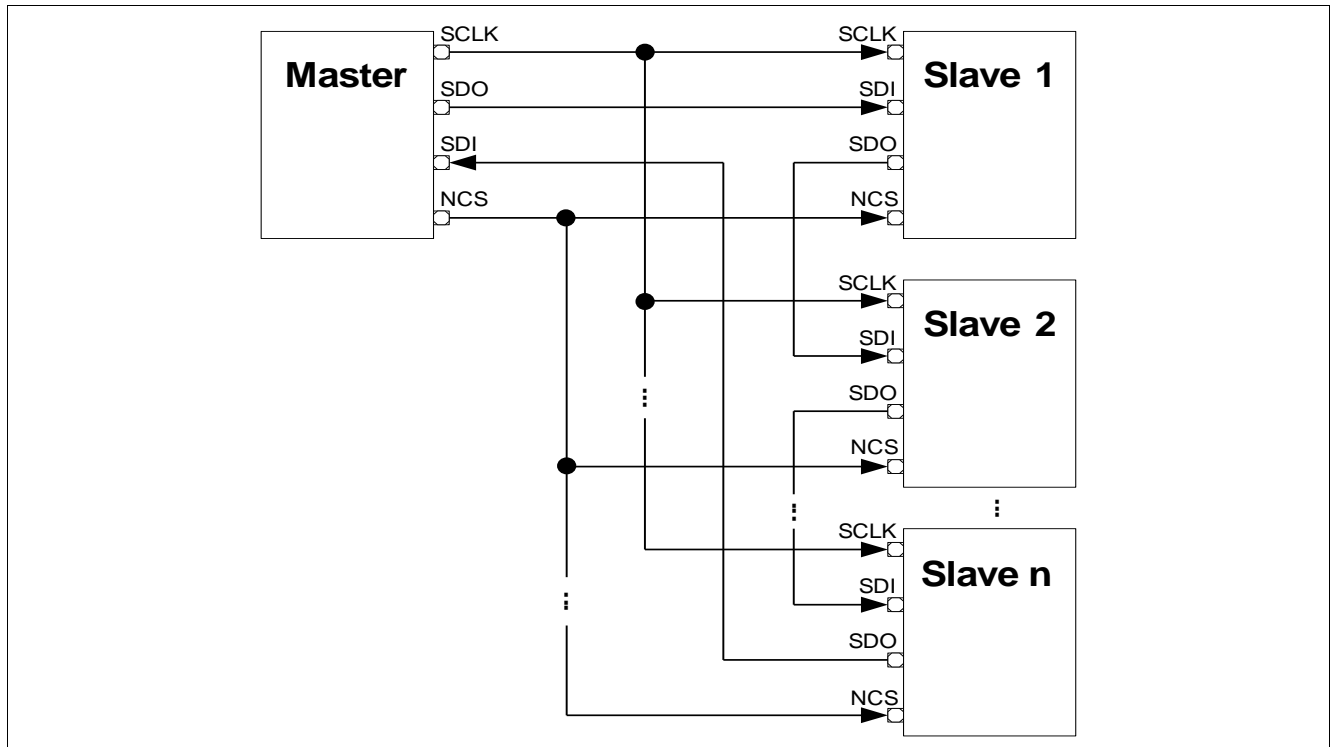


Figure 2-7 SPI Daisy Chain Bus Topology

Physical Layer

The SPI interface relies on two shift registers:

- A shift output register, reacting on the rising edges of **SCLK**.
- A shift input register, reacting on the falling edges of **SCLK**.

When signal **NCS** is inactive, the signals at pins **SCLK** and **SDI** are ignored. The output **SDO** is in tristate.

When **NCS** is activated, the shift output register is updated internally with the value requested by the previous SPI access.

At each rising edge of the **SCLK** signal (while **NCS** is active), the shift output register is serially shifted out by one bit on the **SDO** pin (MSB first). At each falling edge of the clock pulse, the data bit available at the input **SDI** is latched and serially shifted into the shift input register.

At the deactivation of **NCS**, the SPI logic checks how many rising and falling edges of the **SCLK** signal have been received. In case both counts differ and / or are not a multiple of 16, an SPI Error is generated. The SPI block then checks the validity of the received 16-bit word. In case of a non valid data, an SPI error is generated. In case no error is detected, the data is decoded by the internal logic.

The **NCS** signal is active low.

Input Debouncing Filters

The input stages of signals **SDI**, **SCLK**, and **NCS** include each a Debouncing Filter. The input signals are that way filtered from glitches and noise.

The input signals **SDI** and **SCLK** are analyzed at each edge of the internal clock derived from OSC1. If the same external signal value is sampled three times consecutively, the signal is considered as valid and is processed by the SPI logic. Otherwise, the transition is considered as a glitch and is discarded.

The input signal **NCS** is sampled at a rate corresponding to the period of the internal clock derived from OSC1. If the same external signal value is sampled two times consecutively, the signal is considered as valid and is processed by the SPI logic. Otherwise, the transition is considered as a glitch and is discarded.

2.4.4.3 Definitions

Command

A command is a high-level command issued by the SPI master which aims at generating a specific reaction in the addressed slave. The command is physically translated into a Request Message by the SPI master. The correct reception of the Request Message by the SPI slave leads to a specific action inside the slave and to the emission of an Answer Message by the slave.

Example: the READ command leads to the transfer of the value of the specified register from the device to the SPI master.

Word

A word is a 16-bit sequence of shifted data bits.

Transfer

A transfer is defined as the SPI data transfers (in both directions) occurring between a falling edge of **NCS** and the next consecutive rising edge of **NCS**.

Request Message

A request message is a word issued by the SPI master and addressing a single slave. A request message relates to a specific command.

Answer Message

An answer message is a well-defined word issued by a single SPI slave as a response to a request message.

Transmit Frame

A transmit frame is a sequence of one or several words sent by the SPI Master within one SPI transfer. In regular SPI topologies, a transmit frame is in practice identical to a data word. In daisy chain topologies, a transmit frame is a sequence of data words belonging to different request messages.

Receive Frame

A receive frame is a sequence of one or several words received by the SPI Master within one SPI transfer. In regular SPI topologies, a receive frame is in practice identical to a data word. In daisy chain topologies, a receive frame is a sequence of data words belonging to different Answer Messages.

The SPI protocol supported by the 1EDI2001AS is based on the Request / Answer principle. The master sends a defined request message to which the slave answers with the corresponding answer message (**Figure 2-8, Figure 2-9**). Due to the nature of the SPI interface, the Answer Message is shifted, compared to the Request Message, by one SPI transfer. It means, for example, that the last word of answer message n is transmitted by the slave while the master sends the first word of request message n+1.

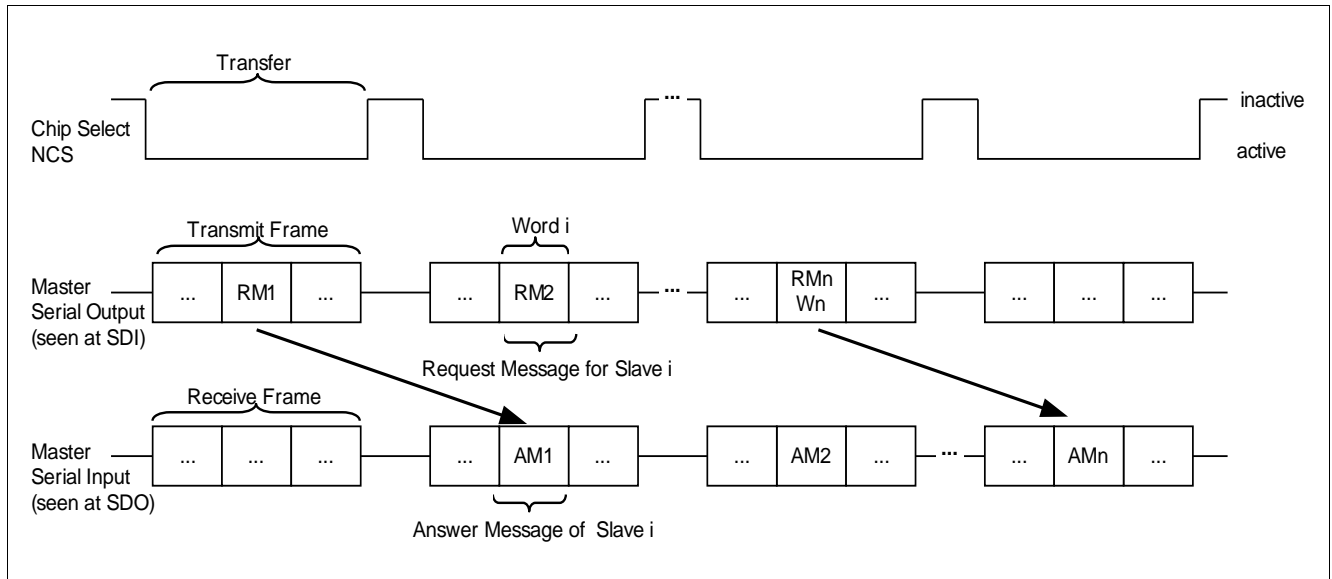


Figure 2-8 Response Answer Principle - Daisy Chain Topology

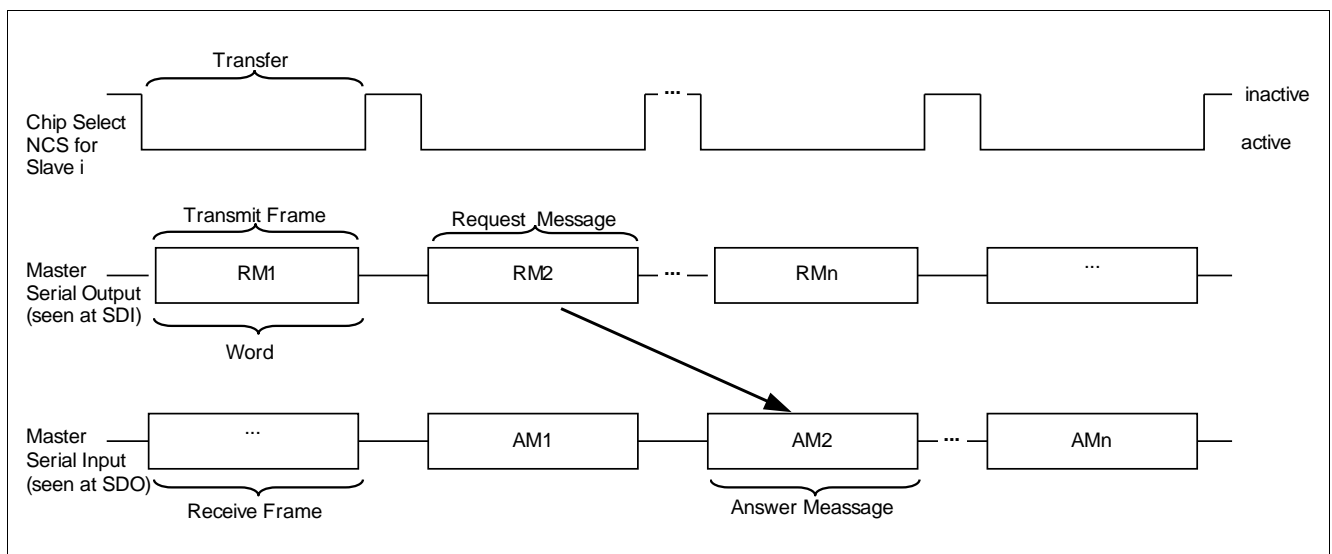


Figure 2-9 Response Answer Principle - Regular Topology

The first word transmitted by the device after power-up is the content of register **PSTAT**.

2.4.4.4 SPI Data Integrity Support

2.4.4.4.1 Parity Bit

By default, the SPI link relies on an odd parity protection scheme for each transmitted or received 16-bit word of the SPI message. The parity bit corresponds to the LSB of the 16-bit word. Therefore, the effective payload of a 16-bit word is 15 data bit (plus one parity bit). The parity bit check (on the received data) can be disabled by clearing bit **PCFG.PAREN**. In this case, the parity bit is considered as “don’t care”. The generation of the parity bit by the driver for transmitted words can not be disabled (but can be considered as “don’t care” by the SPI master).

Note: For fixed value commands (ENTER_CMODE, ENTER_VMODE, EXIT_CMODE, NOP), it has to be ensured that the value of the parity bit is correct even if parity check is disabled. Otherwise, an SPI error will be generated.

2.4.4.4.2 SPI Error

When the device is not able to process an incoming request message, an SPI error is generated: the received message is discarded by the driver, bit **PER.SPIER** is set and the erroneous message is answered with an error notification (bit **LMI** set).

Several failures generate an SPI error:

- A parity error is detected on the received word.
- An invalid data word format is received (e.g. not a 16 bit word).
- A word is received, which does not corresponding to a valid Request Message.
- A command is received which can not be processed. For example, the driver receives in Active Mode a command which is only valid in other operating modes. Another typical example is a read access to the secondary while the previous read access is not yet completed (device “busy”).
- An SPI access to an invalid address.

*Note: the content of a frame with LMI bit set is the value of register **PSTAT**.*

*Note: In case of permanent LMI error induced by system failures, it is recommended to apply a reset via pin **NRST/RDY**.*

2.4.4.5 Protocol Description

2.4.4.5.1 Command Catalog

Table 2-3 gives an overview of the command catalog supported by the device. The full description of the commands and of the corresponding request and answer messages is provided in the following sections.

Table 2-3 SPI Command Catalog

| Acronym | Short Description | Valid in Mode |
|-------------|--|-------------------------|
| ENTER_CMODE | Enters into Configuration Mode. | OPM0, OPM1 |
| ENTER_VMODE | Enters into Verification Mode. | OPM2 |
| EXIT_CMODE | Leaves Configuration Mode to enter into Configured Mode. | OPM2 |
| READ | Reads the register value at the specified address. | All |
| NOP | Triggers no action in the device (equivalent to a “nop”). | All |
| WRITEH | Update the most significant byte of the internal write buffer. | All |
| WRITEL | Updates the least significant byte of the internal write buffer, and copies the contents of the complete buffer into the addressed register. The write buffer is cleared afterwards. | All (with restrictions) |

An overview of the commands is given **Figure 2-10**.

| Message | Command | | | | Data | | | | | | | | | | | | P |
|-------------|---------|---|---|---|------|----|----|-----|-----|-----|-----|-----|-----|----|----|---|---|
| ENTER_CMODE | 0 | 0 | 0 | 1 | 1 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| ENTER_VMODE | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 1 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| EXIT_CMODE | 0 | 0 | 0 | 1 | 0 | 0 | 1 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 |
| NOP | 0 | 0 | 0 | 1 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 0 | 0 | 0 | 0 |
| READ | 0 | 0 | 0 | 0 | A4 | A3 | A2 | A1 | A0 | 0 | 1 | 0 | 1 | 0 | 1 | X | |
| WRITEH | 0 | 1 | 0 | 0 | 0 | 1 | 0 | D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 | X | |
| WRITEL | 1 | 0 | 1 | 0 | A4 | A3 | A2 | A1 | A0 | D7 | D6 | D5 | D4 | D3 | D2 | X | |

Figure 2-10 SPI Commands Overview

2.4.4.5.2 Word Convention

In order to simplify the description of the SPI commands, the following conventions are used (**Table 2-4**).

Table 2-4 Word Convention

| Acronym | Value |
|----------------|----------------------------|
| Va(REGISTER) | Value of register REGISTER |
| P _B | Parity Bit |

Table 2-4 Word Convention (cont'd)

| Acronym | Value |
|---------------------------------|---|
| <<n | Left shift operation of n bits. |
| x _H y _H | Result of the operation: x _H OR y _H |

2.4.4.5.3 ENTER_CMODE Command

The goal of this function is to set the device into Configuration Mode. After reception of a valid ENTER_CMODE command, mode OPM2 is active. This command is only valid in Default Mode (OPM0 and OPM1). In case the request message is received while OPM1 is not active, the complete command is discarded and an SPI error occurs.

Table 2-5 describes the request message and the corresponding answer message.

Table 2-5 ENTER_CMODE request and answer messages

| | Transfer 1 | Transfer 2 |
|-----------------|-------------------|--------------------|
| Request message | 1880 _H | N.a. |
| Answer message | N.a. | Va(PSTAT) |

2.4.4.5.4 ENTER_VMODE Command

The goal of this function is to set the device into Verification Mode. After reception of a valid ENTER_VMODE command, mode OPM5 is active. This command is only valid in Configuration Mode (OPM2). In case the request message is received while OPM2 is not active, the complete command is discarded and an SPI error occurs.

Table 2-6 describes the request message and the corresponding answer message.

Table 2-6 ENTER_VMODE request and answer messages

| | Transfer 1 | Transfer 2 |
|-----------------|-------------------|--------------------|
| Request message | 1140 _H | N.a. |
| Answer message | N.a. | Va(PSTAT) |

2.4.4.5.5 EXIT_CMODE Command

When a valid EXIT_CMODE is received by the device, the Configuration Mode is left to Configured Mode (Mode OPM3 active). This command is only valid in Configuration Mode (OPM2). In case the request message is received while OPM2 is not active, the complete command is discarded and an SPI error occurs.

Table 2-7 describes the request message and the corresponding answer message.

Table 2-7 EXIT_CMODE request and answer messages

| | Transfer 1 | Transfer 2 |
|-----------------|-------------------|--------------------|
| Request message | 1220 _H | N.a. |
| Answer message | N.a. | Va(PSTAT) |

2.4.4.5.6 NOP Command

This command triggers no specific action in the driver (equivalent to a “nop”). However, the mechanisms verifying the validity of the word are active. This command is valid in all operating modes.

Table 2-8 describes the request message and the corresponding answer message.

Table 2-8 NOP request and answer messages

| | Transfer 1 | Transfer 2 |
|-----------------|-------------------|--------------------|
| Request message | 1410 _H | N.a. |
| Answer message | N.a. | Va(PSTAT) |

2.4.4.5.7 READ Command

This command aims at reading the value of the register whose address is specified in the request message. This command is valid in all operating modes. However, in OPM4 and OPM6, the use of the READ command is restricted (see **Table 4-3**). If an access outside the allowed address range is performed, the access is discarded as invalid and an SPI error occurs.

Table 2-9 describes the request message and the corresponding answer message.

Table 2-9 READ request and answer messages

| | Transfer 1 | Transfer 2 |
|-----------------|------------|--------------|
| Request message | See below | N.a. |
| Answer message | N.a. | Va(Register) |

Request message words

Word 1: (ADDRESS_5BIT << 7) | 002A_H | P_B.

Answer message words

Word 1: Value of REGISTER.

2.4.4.5.8 WRITEH

This command aims at writing the upper byte of the internal write buffer with the specified value. This command has no other effect on the functionality of the device. This command is valid in all operating modes.

Table 2-10 describes the request message and the corresponding answer message.

Table 2-10 WRITEH request and answer messages

| | Transfer 1 | Transfer 2 |
|-----------------|------------|--------------------|
| Request message | See below | N.a. |
| Answer message | N.a. | Va(PSTAT) |

Request message words

Word 1: 4400_H | (DATA_8BIT << 1) | P_B

2.4.4.5.9 WRITEL

This command aims at updating the value of the register whose address is specified in the request message. This command is valid in all operating modes. However, depending on the active operating mode, this command is restricted to a given address range or specific registers (see [Table 4-4](#)). If an access outside the allowed address range is performed, the access is discarded as invalid and an SPI error occurs.

At the reception of this command, the least significant byte of the internal buffer is written with the specified value, the contents of the buffer is copied to the register at the specified address and the complete write buffer is cleared.

[Table 2-11](#) describes the request message and the corresponding answer message.

Table 2-11 WRITEL request and answer messages

| | Transfer 1 | Transfer 2 |
|-----------------|------------|--------------------|
| Request message | See below | N.a. |
| Answer message | N.a. | Va(PSTAT) |

Request message words

Word 1: $A000_H \mid (ADDRESS_5BIT \ll 7) \mid (DATA_6BIT \ll 1) \mid P_B$.

2.4.5 Operating Modes

2.4.5.1 General Operation

At any time, the driver can be in one out of seven possible operating modes:

- OPM0: Default Mode (default after reset, device is disabled).
- OPM1: Error Mode (reached after Event Class B, device is disabled).
- OPM2: Configuration Mode (device is disabled, configuration of the device can be modified).
- OPM3: Configured Mode (device is configured and disabled).
- OPM4: Active Mode (normal operation).
- OPM5: Verification mode (intrusive diagnostic functions can be triggered).
- OPM6: Weak active mode (the device can be turned on but with restrictions)

The current active mode of the device is given by bit field **SSTAT.OPM**.

The concept of the device is based on the following general ideas:

- The driver can only switch the IGBT on when OPM4 mode is active (exception: weak-turn on in OPM6).
- Starting from Mode OPM0 or OPM1, the Active Mode OPM4 can only be activated through a dedicated SPI command sequence and the activation of the hardware signal **EN**. As a result, the probability that the device goes to OPM4 mode due to random signals is negligible.
- Differentiations of errors: different classes of errors are defined, leading to different behavior of the device.

The state diagram for the operating modes is given in **Figure 2-11**:

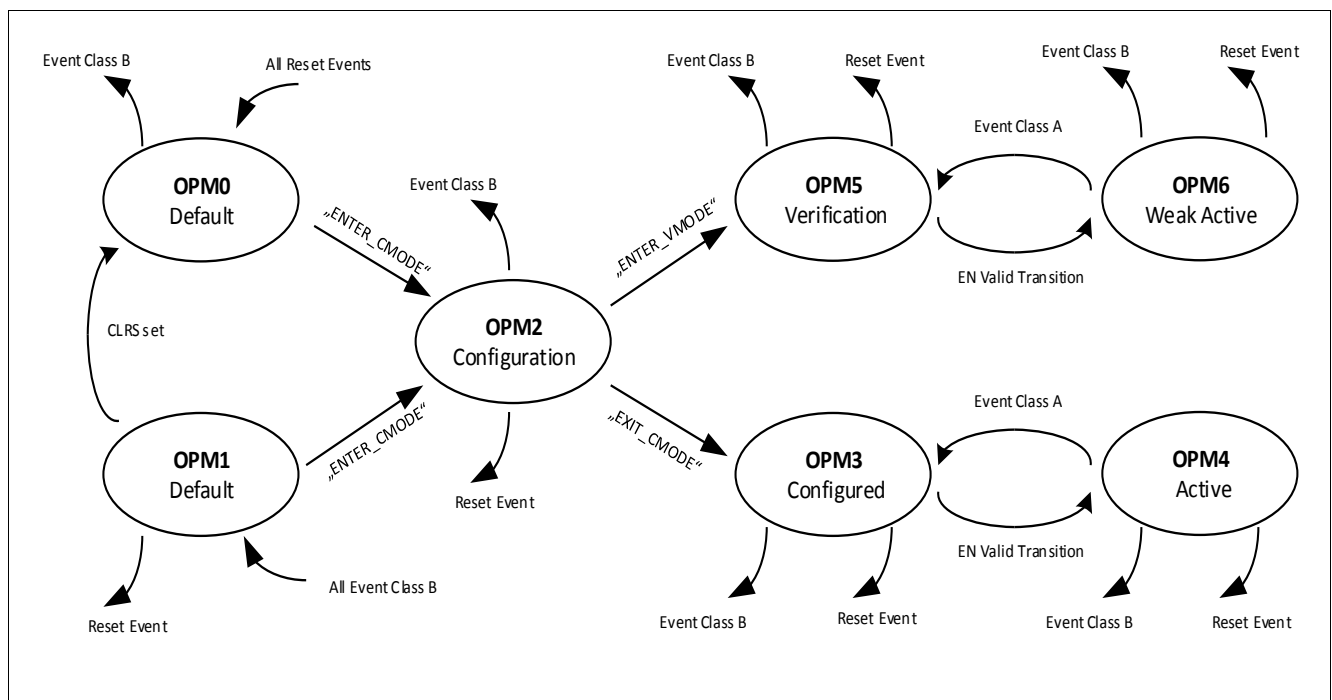


Figure 2-11 Operating Modes State Diagram

2.4.5.2 Definitions

2.4.5.2.1 Events and State Transitions

The transitions from one state to the other are based on “events” and / or SPI commands. The following classification is chosen for defining the events.

Events Class A

The following (exhaustive) list of events are defined as Events Class A:

- Occurrence of a DESAT event (leads to a safe turn-off sequence).
- Occurrence of an OCP event (leads to a safe turn-off sequence).
- Valid to Invalid transition on **EN** signal (leads to a regular turn-off sequence).
- Tristate event due to an Output Stage Monitoring event.
- Tristate event due to the activation of signal **OSD**.

When an Event Class A occurs, the output stage either initiates either a safe turn-off sequence (DESAT, OCP, or a regular turn-off sequence (**EN** event) or goes in tristate (tristate event). The event is notified via an error bit in the corresponding register.

Note: Contrarily to a reset event, an Event Class A does not affect the contents of the configuration registers.

When an Event Class A occurs, the device may change its operating mode depending on which mode is active when the event occurs:

- If it was in OPM4, it goes in OPM3.
- If it was in OPM6, it goes in OPM5.

In all other cases, the OPM is unaffected. A state transition due to an Event Class A leads to the activation of signal **NFLTA**. If no state transition occurs (if for example the device was not in OPM4 or OPM6), **NFLTA** is not activated (exception: tristate event - see [Chapter 2.4.7](#) for more details on failure notifications).

Events Class B

The following (exhaustive) list of events are defined as Events Class B:

- Occurrence of a UVLO2 event.
- Occurrence of a OVLO2 event.
- Occurrence of a UVLO3 event.
- Occurrence of a OVLO3 event.
- Internal Supervision Error.
- Verification Mode Time Out Error

When an Event Class B occurs, the output stage initiates a regular turn-off sequence. The event is notified via an error bit in the corresponding register and (possibly) via the signal **NFLTB**.

Note: Events Class B may affect the contents of the configuration registers.

When an Event Class B occurs, the device may change its operating mode depending on which mode is active when the event occurs: if it was not in OPM1, it goes to OPM1. It is unaffected otherwise

A state transition due to an Event Class B leads to the activation of signal **NFLTB**. If no state transition occurs (if for example the device was already in OPM1), **NFLTB** is not activated. See [Chapter 2.4.7](#) for more details on failure notifications.

Events Class C

Generally speaking, Events Class C are error events that do not lead to a change of the operating mode of the device. The following (non-exhaustive) list of events is comprised within the Event Class C:

- Over Temperature Warning.
- SPI Error.
- Shoot Through Protection error.
- Etc.

SPI Commands

The following SPI commands have an impact on the device's operating mode. The SPI commands are described in [Chapter 2.4.4.5](#).

- ENTER_CMODE.
- ENTER_VMODE.
- EXIT_CMODE.
- Setting of bit **SCTRL.CLRS** (by writing register **PCTRL**)

Reset Events

A reset sets the device (or part of the device) in its default state. Reset events are described in [Chapter 2.4.9](#).

2.4.5.2.2 Emergency Turn-Off Sequence

The denomination "Emergency Turn-Off Sequence" (ETO) is used to describe the sequence of actions executed by the output stage of the device when an Event Class A (exception: tristate event), Class B or a Reset Event is detected.

An ETO sequence is described by the following set of actions:

- A Turn-Off sequence is initiated. In case of DESAT or OCP event, a safe turn-off sequence is initiated. For the other events, a regular turn-off sequence is initiated.
- The device enters the corresponding OPM mode. As a consequence, the device is disabled.

Once an ETO has been initiated, the device can not be reenabled for a maximum duration consisting of 256 OSC2 clock cycles. Consequently, the user shall wait for this duration before reenabling the device and sending PWM turn-on command.

2.4.5.2.3 Ready, Disabled, Enabled and Active State

The device is said to be in Ready state in case no reset event is active on the primary chip. When the device is Ready, signal **NRST/RDY** is at High level.

When the device is in Disabled State, the PWM turn-on commands are ignored. This means that whatever the input signal **INP** is, the output stage (if not tristated) delivers a constant turn-off signal to the IGBT. Unless otherwise stated, all other functions of the device work normally.

When the device is not in Disabled State, it is said to be in Enabled State. In this case, the PWM signal command is processed normally (if the output stage is not tristated). Practically, the device is in Enabled State when either Mode OPM4 or Mode OPM6 is active.

Active State corresponds to the normal operating state of the device. Practically, the device is in Active State when Mode OPM4 is active.

Note: When the device is in Active State, it implicates it is in Enabled state.

2.4.5.3 Operation Modes Description

Default Mode (OPM0)

Mode OPM0 is the default operating mode of the device after power up or after a rest event. In OPM0, the device is in Disabled State.

The following exhaustive list of events bring the device in OPM0 Mode:

- Occurrence of a Reset Event.
- Bit **SCTRL.CLRS** set while the device was in OPM1.

Error Mode (OPM1)

Mode OPM1 is the operating mode of the device after an Event Class B.

The following exhaustive list of events bring the device in OPM1 Mode:

- Occurrence of an Event Class B.

In OPM1, when bit **SCTRL.CLRS** is set via the corresponding SPI command, the device shall normally jump to OPM0. However, in case the conditions for an Event Class B are met at that moment, no state transition occurs and the device stays in OPM1. The operation of bit **SCTRL.CLRS** on the secondary sticky bits works normally.

In OPM1, when a valid ENTER_CMODE command is received, the device shall normally jump to OPM2. However, in case the conditions for an Event Class B are met at that moment, no state transition occurs and the device stays in OPM1 for the duration of the event. The state transition to OPM2 is executed as soon as the conditions leading to the Event Class B disappear. It shall be noted that no LMI error notification is issued.

Configuration Mode (OPM2)

Configuration Mode is the mode where the configuration of the device can be modified. When OPM2 is active, the device is in Disabled State.

The following exhaustive list of events bring the device in Configuration Mode:

- Reception of a valid ENTER_CMODE command **while** Mode OPM0 or OPM1 active.

Configured Mode (OPM3)

Configured Mode is the mode where the device is ready to be enabled. When OPM3 is active, the device is in Disabled State.

The following exhaustive list of events bring the device in Mode OPM3:

- Reception of a valid EXIT_CMODE command **while** Mode OPM2 active.
- Event Class A **while** Mode OPM4 active.

Active Mode (OPM4)

The Active Mode corresponds to the normal operating mode of the device. When OPM4 is active, the device is in Active State. The following exhaustive list of event bring the device in Active Mode:

- Invalid to Valid Transition on signal **EN** while Mode OPM3 active.

Verification Mode (OPM5)

Verification Mode is the mode where intrusive verification functions can be started. When OPM5 is active, the device is in disabled state.

The following exhaustive list of event bring the device in Verification Mode:

- Reception of a valid ENTER_VMODE command **while** Mode OPM2 active.
- Occurrence of an Event Class A **while** Mode OPM6 active.

After a transition from Mode OPM2 to OPM5, an internal watchdog timer is started. If after time t_{VMTO} , the device has not left both modes OPM5 or OPM6, a time-out event occurs and an Event Class B is generated.

Weak Active Mode (OPM6)

Weak Active Mode is the mode where the device can be activated to run diagnosis tests at system level. When OPM6 is active, the device is in Enabled State. A PWM turn-on command issues a Weak Turn-On on the secondary side.

The following exhaustive list of event bring the device in Weak Active Mode:

- Invalid to Valid Transition on signal **EN** while Mode OPM5 active.

The watchdog counter started when entering Mode OPM5 is not reset when entering OPM6.

Implementation Notes related to State Transitions

- An Event Class A or Class B detected on the secondary side lead to an immediate reaction of the device's output stage. Due to the latency of the inter-chip communication, the notification on the primary side is slightly delayed.
- The activation of signal **NFLTA** or **NFLTB** is simultaneous to the corresponding state transition on the primary side.
- It is possible to change the operating mode while a failure condition is present. This may however lead to a new immediate error notification and state transition.

2.4.5.4 Activating the device after reset

After a reset event, the device is in Mode OPM0 and disabled. In order to be active, the device needs to enter Configuration Mode with the ENTER_CM0DE command. Once all the configurations have been performed, the Configuration Mode has to be exited with an EXIT_CM0DE command. Once this is done, the device can enter the Active Mode when Invalid to Valid transition on pin **EN** is detected.

2.4.5.5 Activating the device after an Event Class A or B

If during operation, an Event Class A occurs, the device enters the OPM3 (or OPM5). Bit field **SSTAT.OPM** is updated accordingly. In order to reactivate the device, an invalid-to-valid transition has to be applied to signal **EN**. It means that a Low-level and then a High level is applied to **EN**. If no Event Class A event is active, the device will enter OPM4 (respectively OPM6).

If during operation, an Event Class B occurs, the device enters the Default Mode OPM1. Bit field **SSTAT.OPM** is updated accordingly. In order to reactivate the device, the steps defined in [Chapter 2.4.5.4](#) need to be performed.

2.4.5.6 Debug Mode

The **DEBUG** pin gives the possibility to operate the device in the so-called Debug Mode. The goal of the Debug Mode is to operate the device without SPI interface. This mode should be used for development purpose only and is not intended to be used in final applications.

At V_{CC2} power-on, the level at pin **DEBUG** is latched. In case a High level is detected, the device enters the Debug Mode. Bit **SSTAT.DBG** is then set.

In Debug Mode, the regular operation of the internal state machine is modified, so that the device can only enter OPM3 or OPM4. As a result Modes OPM0, OPM1, OPM2, OPM5 and OPM6 are completely bypassed. In case of a Reset event, the device goes to OPM3 (instead of OPM0). Besides, in Debug Mode, events leading normally to an Event Class B are replaced an Event Class A, resulting in the activation of signal **NFLTA**. Event Class B are therefore not generated by the device in Debug Mode (and signal **NFLT B** shall not be used).

It should be noted that the configuration of the device in Debug Mode corresponds to the default settings and can not be changed (for example, the DESAT function is completely deactivated).

In Debug Mode, the operation of the device is otherwise similar to regular operation. It means in particular that the signal **EN** has to be managed properly: when the device is in OPM3, a Low to High level transition has to be applied to the device in order to enter OPM4 (Active Mode).

*Note: Once it has been latched at power-on, the level on the pin **DEBUG** has no impact on the device until the next power-on event on the secondary side.*

For a Safe Turn-Off sequence, the TTOFF delay is defined by bit field **SSTOF.STVAL**. Setting this field to 00_H completely disables the TTOFF function for all Safe Turn-Off sequences (but this has no effect on Regular Turn-Off sequences). If this function is to be activated, a minimum value for the delay time has to be programmed. The plateau level is defined by **SSTOF.GPS**.

The timing of a Safe Turn-Off event is in the clock domain of the main secondary oscillator (OSC2). The timing of a Regular Turn-Off event is in the clock domain of the Start-Stop Oscillator (SSOSC2), leading to high accuracy and low PWM distortion

When using the TTOFF function (with a non-zero delay), the PWM command is received on pin **INP** is delayed by the programmed delay time (**Figure 2-13**). For pulses larger than the TTOFF delay ($t_{PULSE} > t_{TTOFF} + 2 \text{ SSOSC cycles}$), the output pulse width is kept identical to the input pulse width. For smaller pulses ($t_{PULSE} < t_{TTOFF} + 2 \text{ SSOSC cycles}$), the output pulse is identical to the programmed delay. The minimum pulse width delivered by the device to the IGBT is therefore the programmed delay time extended by two SSOSC cycles.

The device allows for external booster voltage compensation at the IGBT gate. When bit **SCFG.VBEC** is cleared, the voltage at **TOFF** at the plateau corresponds to the programmed value. When bit **SCFG.VBEC** is set, an additional V_{BE} (base emitter junction voltage of an internal pn diode) is subtracted from the programmed voltage at **TOFF** in order to compensate for the V_{BE} of an external booster.

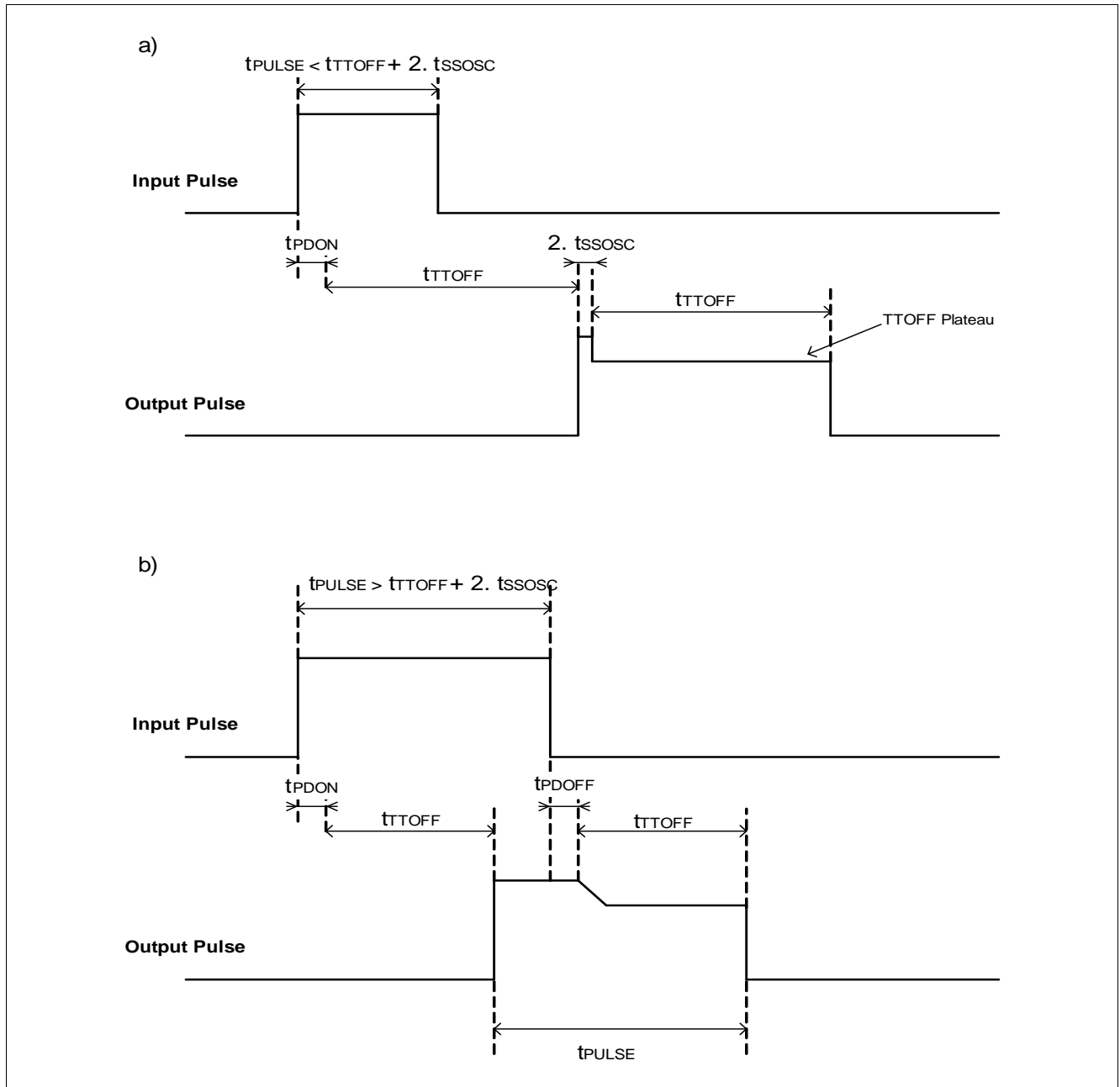


Figure 2-13 TTOFF: Principle of Operation

Pulse Suppressor

In order to increase the device's robustness against external disturbances, a pulse suppressor can be enabled by setting bit **SCFG.PSEN**. Register **SRTTOF** shall also be programmed with a value higher than 2_H . When a PWM turn-on sequence occurs, the activation of the output stage is delayed by the programmed TTOFF number of cycles, as for a normal TTOFF sequence. However, the PWM command received by the secondary chip signal is internally sampled at every SSOSC cycle before the actual turn-on command is executed by the output stage. If at least one of the sampling points does not detect a high level, the turn-on sequence is aborted and the device is not switched on.

In case a valid PWM ON command is detected by the secondary side after the decision point the previous sequence has been aborted, a new turn-on sequence is initiated.

Functional Description

One of the consequence of activating the pulse suppressor is that all PWM pulses shorter than the programmed TTOFF plateau time are filtered out ([Figure 2-14](#)).

Note: The Pulse Suppressor only acts on turn-on pulses, not on turn-off pulses.

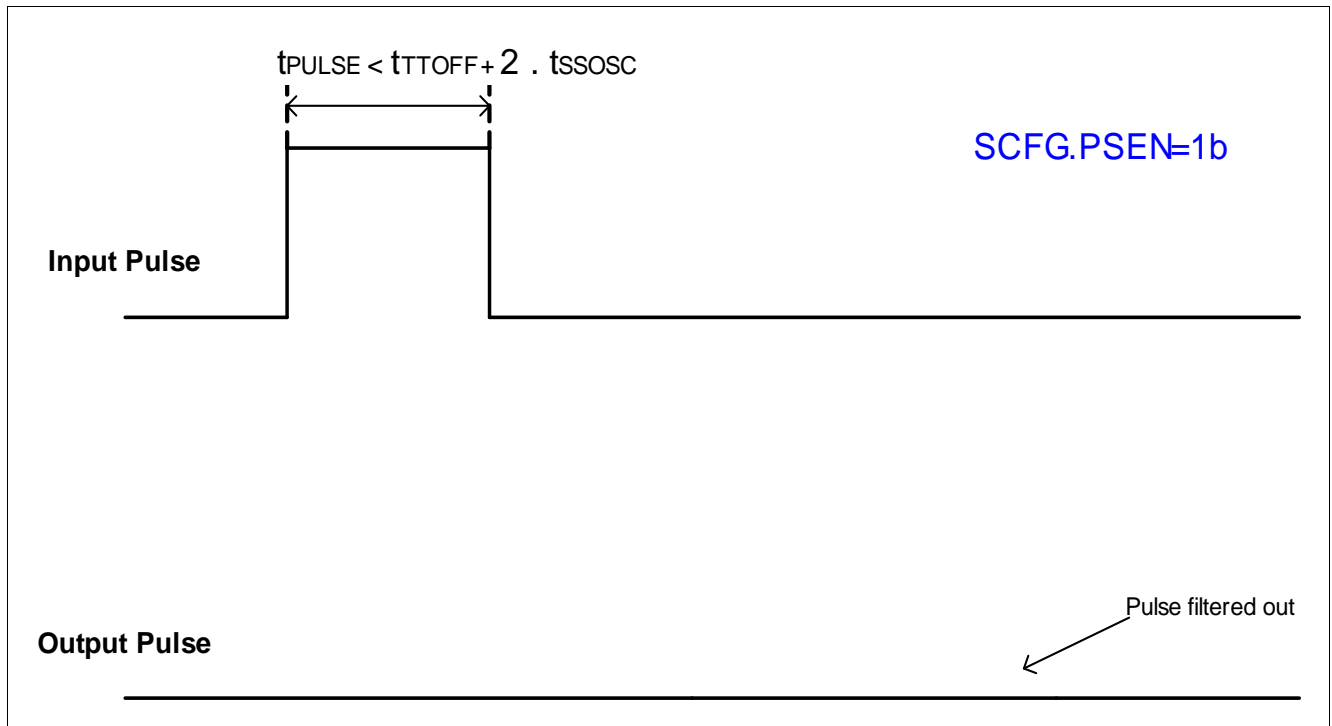


Figure 2-14 TTOFF: pulse suppressor aborting a turn-on sequence

2.4.6.2 Switching Sequence Description

Figure 2-15 shows an idealized switching sequence. When a valid turn-on command is detected, a certain propagation time t_{PDON} is needed by the logic to transfer the PWM command to the secondary side. At this point the TTOFF delay time t_{TTOFF} defined by bit field **SRTTOF.RTVAL** is added before the turn-on command is executed. Signal **TON** is then activated, while signal **TOFF** is deactivated.

When a valid turn-off command is detected, a certain propagation time t_{DOFF} is needed by the command to be processed by the logic on the secondary side. This propagation time depends on the event having generated the turn-off action (non exhaustive list):

- In case of a PWM turn-off command at pin **INP**, $t_{DOFF}=t_{PDOFF}$.
- In case of a DESAT Event, $t_{DOFF}=t_{OFFDESAT2}$.
- In case of an OCP event, $t_{DOFF}=t_{OFFOCP2}$.
- In case of an Event Class A on the primary side: $t_{DOFF}=t_{OFFCLA}$.
- In case of an Event Class B on the secondary side: $t_{DOFF}=t_{OFFCLB2}$.

When the turn-off command is processed by the logic, signal **DACL** is deactivated (i.e. active clamping is enabled). Signal **TON** and **TOFF** are decreased with the slew rate t_{SLEW} fixed by hardware. Once the voltage at pin **TOFF** has reached the value defined by bit field **SCTRL.GPOFS** (or **SSTTOF.GPS** in the case of a safe turn-off), the turn-off sequence is interrupted. Time t_{TTOFF} is defined as the moment when the device starts turning off signal **TOFF**, and the moment where the turn-off sequence is resumed. Depending on the event that triggered the turn-off sequence, t_{TTOFF} is given by either bit field **SRTTOF.RTVAL** or **SSTTOF.STVAL**. Once the TTOFF time has elapsed, a hard commutation takes place, and signals **TON** and **TOFF** are driven to V_{EE2} .

Note: Once a turn-off sequence is started, it is completed to the end with the same delay parameters.

At the moment when the hard commutation takes place, signal **DACL** remains deactivated for time t_{ACL} defined by bit field **SACLT.AT**. When this time is elapsed, signal **DACL** is reactivated (i.e. active clamping is disabled).

In case **SACLT.AT** is set to 0_H , **DACL** is constantly activated (constant High level). In case **SACLT.AT** is set to FF_H , **DACL** is constantly at Low level.

The Gate Monitoring function (time-out mechanism) is started at each turn-on and turn-off sequence. See **Chapter 3.4.2** for more details.

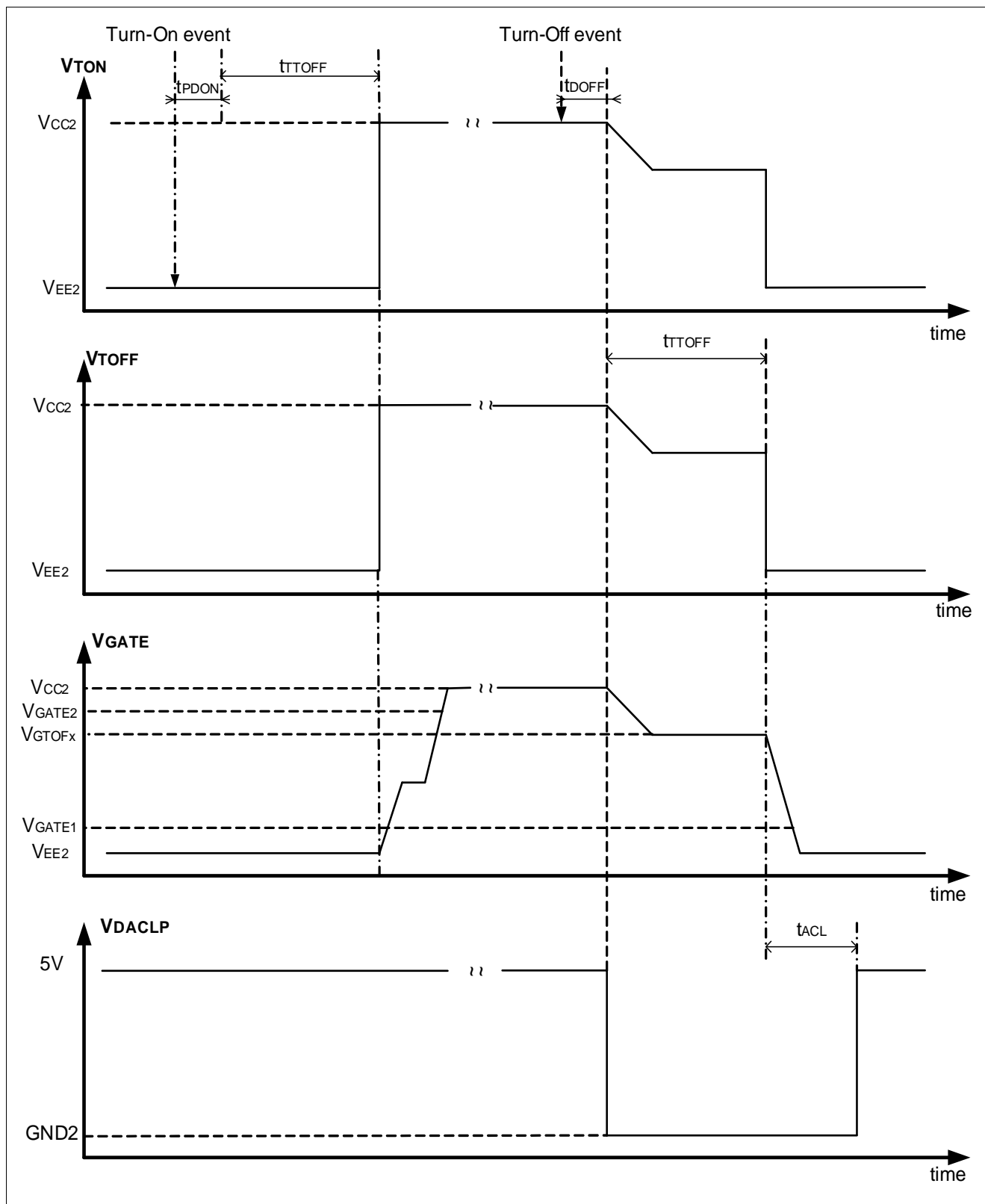


Figure 2-15 Idealized Switching Sequence

2.4.7 Fault Notifications

The device provides two kinds of fault notification mechanisms:

- Pins **NFLTA**, **NFLTB** and **NRST/RDY** allow for fast error notification to the main microcontroller. All signals are active low.
- Error bits can be read by SPI.

The activation of signal **NRST/RDY** is associated with Reset Events (see [Chapter 2.4.9](#)). The activation of signal **NFLTA** is associated with Class A Events. The activation of signal **NFLTB** is associated with Class B Events. In general the activation of signal **NFLTA** or **NFLTB** is linked to a state transition of the state machine.

If an Event Class A occurs that leads to a state transition (from OPM4 to OPM3 or OPM6 to OPM5), signal **NFLTA** is activated. In case an Event Class A occurs that does not lead to a state transition, **NFLTA** is not activated (exception: tristate events). However, the corresponding error bit in register **PER** or **SER** is set.

Tristate events are handled in a special way. Tristate events can be generated either by the output stage monitoring (when enabled) or by a High Level at pin **OSD**.

In case bit **SCFG.OSMD** is set, the OSM is completely disabled and therefore can not generate any tristate events (and consequently it can not generate Events Class A).

In case bit **SCFG.OSDAD** is set, a transition to High Level of pin **OSD** does not generate any state transition. As a result, no Event Class A is generated. However, bit **SER.OSTER** is set and the output stage is in tristate for the duration for which pin **OSD** is at High Level.

Additionally, signal **NFLTA** can be activated directly by the status bits on the primary side. This allows to have signal **NFLTA** activated in any OPM mode in case of tristate events. If **PCFG.OSTAEN** is set, **NFLTA** is activated at the transition of bit **PER.OSTER** from 0_B to 1_B. If **PCFG.OSMAEN** is set, **NFLTA** is activated at the transition of bit **PSTAT2.OSTC** from 0_B to 1_B. In case both bits **PCFG.OSTAEN** and **PCFG.OSMAEN** are cleared, **NFLTA** is only activated in case of a state transition of the state machine.

If an Event Class B occurs that leads to a state transition (to OPM1), signal **NFLTB** is activated. In case an Event Class B occurs that does not lead to a state transition, **NFLTB** is not activated. However, the corresponding error bit in register **PER** or **SER** is set.

[Table 2-12](#) describes how failure notifications are cleared:

Table 2-12 Failure Notification Clearing

| | NFLTA / B signals | Primary Sticky Bits | Secondary Sticky Bits |
|---------------------------------------|----------------------------|----------------------------|------------------------------|
| PCTRL.CLRP set | De-assertion | Cleared | - |
| PCTRL.CLRS set ¹⁾ | - | - | Cleared |
| EN Invalid to Valid transition | De-assertion ²⁾ | - | - |

1) If the device is in OPM1, setting bit **SCTRL.CLRS** leads to a transition to OPM0

2) Only in OPM3 and OPM5. In other Operating Modes, no de-assertion is done.

The level issued by the device on pins **NFLTA** and **NFLTB** is given by bits **PSTAT2.FLTA** and **PSTAT2.FLTB**. The levels read by the device at those pins is given by bits **PPIN.NFLTAL** and **PPIN.NFLTBL**.

2.4.8 EN Signal Pin

The **EN** signal allows the logic on the primary side to have a direct control on the state of the device. A valid signal has to be provided on this pin. A valid to invalid transition of the signal on pin **EN** generates an Event Class A.

Functional Description

Pin **EN** should be driven actively by the external circuit. In case this pin is floating, an internal weak pull-down resistor ensures that the signal is low.

*Note: It should be noted that even if the signal at pin **EN** is valid, the device can still be in disabled state. This may happen for example if another error is being detected*

A valid **EN** signal is defined as a digital High level. When **EN** is at Low level, the signal is considered as not valid and the device is in Disabled State. In case of a High-to-Low transition, an Event Class A is generated.

An Invalid to Valid transition of signal **EN** deactivates signals **NFLTA** and **NFLT B** (when the device is in OPM3 or OPM5 only).

The levels read by the device at pin **EN** is given by bits **PPIN.ENL**. The validity status of **EN** signal is given by bit **PSTAT2.ENVAL**.

2.4.9 Reset Events

A reset event sets the device and its internal logic in the default configuration. All user-defined settings are overwritten with the default values. The list of reset events and their effect is summarized in **Table 2-13**.

Table 2-13 Reset Events Summary

| Reset Event | Primary | Secondary | Notification (primary) | Notification (secondary) |
|---|---------|------------|--|--|
| NRST/RDY Input signal active (driven externally) | Reset | Soft Reset | <ul style="list-style-type: none"> • NRST/RDY Low (during event). • Bit PER.RST1 and PER.RST1 set. • Bit PER.CER1 is not set. • Event Class B (NFLT B activated) at the end of the reset event. | <ul style="list-style-type: none"> • Bit SER.CER2 set (in case of lifesign lost). • Output Stage issues a PWM OFF command. • OSD pin functionality operational. |
| UVLO1 Event | Reset | Soft Reset | <ul style="list-style-type: none"> • NRST/RDY Low (driven by device during event). • Bit PER.RST1 set (once V_{CC1} valid again). • Bit PER.CER1 is not set. • Event Class B (NFLT B activated) at the end of the reset event. | <ul style="list-style-type: none"> • Bit SER.CER2 set (in case of lifesign lost). • Output Stage issues a PWM OFF command. • OSD pin functionality operational. |
| OSC1 not starting at power-up | Reset | Soft Reset | <ul style="list-style-type: none"> • NRST/RDY Low (driven by device during event). • Bit PER.RST1 set (once OSC1 valid again). • Bit PER.CER1 is not set. • Event Class B (NFLT B activated) at the end of the reset event. | <ul style="list-style-type: none"> • Bit SER.CER2 set (in case of lifesign lost). • Output Stage issues a PWM OFF command. • OSD pin functionality operational. |

Functional Description
Table 2-13 Reset Events Summary

| Reset Event | Primary | Secondary | Notification (primary) | Notification (secondary) |
|-----------------------------------|---------|------------|--|--|
| IREF1 shorted to ground or open | Reset | Soft Reset | <ul style="list-style-type: none"> • NRST/RDY Low (driven by device during event). • Bit PER.RST1 set (once IREF1 valid again). • Bit PER.CER1 is not set. • Event Class B (NFLT B activated) at the end of the reset event. | <ul style="list-style-type: none"> • Bit SER.CER2 set (in case of lifesign lost). • Output Stage issues a PWM OFF command. • OSD pin functionality operational. |
| Memory Error on Primary | Reset | Soft Reset | <ul style="list-style-type: none"> • NRST/RDY Low (driven by device during event). • Bit PER.RST1 set (when failure condition is removed). • Bit PER.CER1 is not set. • Event Class B (NFLT B activated) at the end of the reset event. | <ul style="list-style-type: none"> • Bit SER.CER2 set (in case of lifesign lost). • Output Stage issues a PWM OFF command. • OSD pin functionality operational. |
| UVLO2 Event | - | Hard Reset | <ul style="list-style-type: none"> • Event Class B (NFLT B activated, bit PER.CER1 set). • Bit PSTAT.SRDY cleared for the duration of the failure. | <ul style="list-style-type: none"> • Signal NUV2 at Low level (if $V_{CC2} < V_{UVLO2}$). • Bit SER.RST2 (once V_{CC2} valid again). • Output Stage issues a PWM OFF command. • OSD pin functionality operational for: $V_{CC2} > V_{RST2}$. |
| OSC2 not starting at power-up | - | Hard Reset | <ul style="list-style-type: none"> • Event Class B (NFLT B activated, bit PER.CER1 set) • Bit PSTAT.SRDY cleared | <ul style="list-style-type: none"> • Output Stage issues a PWM OFF command. • OSD pin functionality operational. |
| OSC2 misfunction during operation | - | Soft Reset | <ul style="list-style-type: none"> • Event Class B (NFLT B activated, bit PER.CER1 set) • Bit PSTAT.SRDY cleared for the duration of the failure. | <ul style="list-style-type: none"> • Output Stage issues a PWM OFF command. • OSD pin functionality operational. |
| IREF2 open | - | Hard Reset | <ul style="list-style-type: none"> • Event Class B (NFLT B activated, bit PER.CER1 not) • Bit PSTAT.SRDY cleared | None. |

Table 2-13 Reset Events Summary

| Reset Event | Primary | Secondary | Notification (primary) | Notification (secondary) |
|---------------------------|---------|------------|--|---|
| VREG shorted to ground | - | Undefined | <ul style="list-style-type: none"> Event Class B (NFLTB activated, bit PER.CER1 set) Bit PSTAT.SRDY cleared. | <ul style="list-style-type: none"> Signal NUV2 at Low Level. Output Stage issues a PWM OFF command. |
| Memory Error on Secondary | - | Hard Reset | <ul style="list-style-type: none"> Event Class B (NFLTB activated, bit PER.CER1 set). Bit PSTAT.SRDY cleared. | <ul style="list-style-type: none"> Output Stage issues a PWM OFF command. OSD pin functionality operational. |

All reset events set the device in Mode OPM0. In a soft reset, the logic works further, but the registers use the default values.

In case of a reset condition on the primary side, the behavior of the pin of the device is defined in [Table 2-14](#).

Table 2-14 Pin behavior (primary side) in case of reset condition

| Pin | Output Level | Comments |
|----------|--------------|----------|
| SDO | Low | |
| NFLTB | Low | |
| NFLTA | High | |
| NRST/RDY | Low (GND1) | |

In case of a hard reset condition on the secondary side, the behavior of the pin of the device is defined in [Table 2-15](#).

Table 2-15 Pin behavior (secondary side) in case of reset condition

| Pin | Output Level | Comments |
|-------|-------------------|--------------------------------------|
| TON | Low (V_{EE2}) | Passive Clamping |
| TOFF | Low (V_{EE2}) | Passive Clamping |
| DESAT | Low (GND2) | Clamped. |
| GATE | Low (V_{EE2}) | Passive Clamping |
| DACLP | High (5V) | Active clamping disabled by default. |
| NUV2 | Low (GND2) | |

2.4.10 Operation in Configuration Mode

This section describes the mechanisms to configure the device.

2.4.10.1 Static Configuration Parameters

Static parameters can be configured when the device is in Mode OPM2 by writing the appropriate register.

Once Mode OPM2 is left with the SPI Command EXIT_CM0DE, the configuration parameters are frozen on both primary and secondary chips. This means in particular that write accesses to the corresponding registers are invalidated. This prevents static configurations to be modified during runtime. Besides, the configuration

parameters on the primary and secondary side are protected with a memory protection mechanism. In case the values are not consistent, a Reset Event and / or an Event Class B is generated.

2.4.10.1.1 Configuration of the SPI Parity Check

The SPI interface supports by default an odd parity check. The Parity Check mechanism (active at the reception of an SPI word) can be disabled by setting bit **PCFG.PAREN** to 0_B. Setting bit **PAREN** to 1_B enables the Parity Check.

Parity Bit Generation for the transmitter can not be disabled.

2.4.10.1.2 Configuration of NFLTA Activation in case of Tristate Event

Signal **NFLTA** is normally activated by a state transition of the internal state machine. However, it can be also configured to be activated in relation with the primary bits **PER.OSTER** or **PSTAT2.OSTC**. This is configured thanks to bits **PCFG.OSTAEN** and **PCFG.OSMAEN**.

2.4.10.1.3 Configuration of the V_{BE} Compensation

The V_{BE} compensation of signal **TON** and **TOFF** can be activated or deactivated by writing bit **SCFG.VBEC**. See [Chapter 2.4.6](#) for more details.

2.4.10.1.4 Deactivation of Output Stage Monitoring

The OSM function can be disabled by setting bit **SCFG.OSMD**.

2.4.10.1.5 Deactivation of Events Class A due to pin OSD

By setting bit **SCFG.OSDAD**, Event Class A are not issued in case of a Tristate event generated by pin **OSD**. Other actions such as tristating the output stage or setting bit **SER.OSTER** are performed normally.

2.4.10.1.6 Clamping of DESAT pin

By setting bit **SCFG.DSTCEN**, the DESAT signal is clamped to V_{GND2} while the output stage of the device issues a PWM OFF command and during blanking time periods. By clearing bit **SCFG.DSTCEN**, the DESAT clamping is only activated during blanking time periods.

2.4.10.1.7 Activation of the Pulse Suppressor

The pulse suppressor function associated with the TTOFF function can be activated by setting bit **SCFG.PSEN**. When activated, **SRTTOF.RTVAL** shall be programmed with a minimum value (see [Page 108](#)).

2.4.10.1.8 Configuration of the Verification Mode Time Out Duration

The duration of the time out in verification mode is selectable via bit **SCFG.TOSEN**.

2.4.10.1.9 Configuration of the TTOFF Delays

The TTOFF delays for Regular and Safe Turn-Off sequences can be programmed separately by writing registers **SRTOFF** or **SSTOFF**. The delay for Regular Turn-Off can also be configured using the Timing Calibration Feature. Programming 0_H as a delay value disables the TTOFF for the concerned Turn-Off Sequence. Hard turn-off are performed instead. In case the TTOFF function is wished, a minimum value for the delay has to be programmed (see [Page 108](#) and [Page 109](#)).

When safe two level turn-off is used (non zero delay) in normal operating mode (OPM4), the programmed safe turn-off delay value shall be higher than the programmed regular two level turn off delay.

2.4.10.1.10 Configuration of the Safe TTOFF Plateau Level

The plateau level for safe two level turn off sequences can be programmed with bit field **SSTOFF.GPS**. The plateau level value for safe turn-off sequences shall be lower than the one selected for regular turn-off sequences.

2.4.10.1.11 Configuration of the DESAT Blanking Time

The blanking time for the DESAT protection can be configured by writing bit field **SDSAT.DSATBT**. In case this function is used, a minimum value for the delay has to be programmed (see [Page 106](#)).

Note: The programmed OCP blanking time shall be smaller than the programmed DESAT blanking time.

2.4.10.1.12 Configuration of the OCP Blanking Time

The blanking time for the OCP protection can be configured by writing bit field **SOC.PCPBT**. Programming 0_H deactivates the blanking time feature. The programmed blanking time shall not exceed a maximum value (see [Page 107](#)).

Note: The programmed OCP blanking time shall be smaller than the programmed DESAT blanking time.

2.4.10.1.13 Configuration of **DACL** Activation Time

The **DACL** activation time after hard commutation can be programmed by writing bit field **SACLT.AT**. In case value 0_H is programmed, the device delivers at **DACL** a constant High level. In case an activation time is required, a minimum value for the delay has to be programmed (see [Page 112](#)). In case value FF_H is programmed, the device delivers a constant Low level at **DACL**.

2.4.10.2 Dynamic Configuration

The TTOFF plateau level in regular turn-off can be modified during runtime by writing bit field **PCTRL2.GPOF**. The value of this bit field is periodically transferred to the secondary side. The last valid received value by the primary side is available at bit field **PSTAT.GPOFS**. The value currently used by the secondary chip is available at bit field **SCTRL.GPOFS**.

The TTOFF plateau for safe turn-off can only be configured statically with bit field **SSTOFF.GPS**.

This dynamic configuration of the plateau level allows to compensate for temperature variations of the I-V characteristic of the IGBT. In overcurrent conditions, the maximum current flowing through the IGBT when the plateau is reached can be limited more accurately.

Similarly, The WTOLevel can be configured by writing bit field **PCTRL.GPON**.

The plateau value stored in the device at the beginning of the corresponding switching sequence is latched and active until the next switching sequence.

2.4.10.3 Delay Calibration

In order to compensate for timing errors due to part-to-part variations, a dedicated Timing Calibration Feature (TCF) has been implemented. The TCF works in such a way that the PWM input signal is used to start and stop a counter clocked by the Start-Stop Oscillator of the Output Stage. As a result, the following delays and timing can be configured that way:

- TTOFF delay for Regular Turn-Off.

The TCF allows to compensate for part to part variations of the frequency of the Start-Stop oscillator. This results in better accuracy for application critical timing. Device specific variations, e.g. temperature related, are not compensated though.

The TCF can be activated or deactivated in Configuration Mode by writing bit field **SSCR.VFS2**. The device shall then be set in OPM6 and the PWM signal applied. Details about the TCF operation are given in [Chapter 3.5.9](#).

3 Protection and Diagnostics

This section can describes the safety relevant functions implemented in the 1EDI2001AS.

3.1 Supervision Overview

The 1EDI2001AS driver provides extended supervision functions, in order to achieve ASIL requirements on system level. [Table 3-1](#) gives an overview of the implemented functions.

Table 3-1 Safety Related Functions

| Protection Feature | Description | Category | Comments |
|-------------------------------------|---|----------|---|
| DESAT | Monitoring of the collector-emitter voltage of the IGBT in ON state. | A | See Chapter 3.2.1 |
| OCP | Monitoring of the current on the IGBT's auxiliary emitter path. | A | See Chapter 3.2.2 |
| External Enable | Fast deactivation via an external Enable signal on the primary. | A | See Chapter 3.2.3 |
| Output Stage Monitoring | Monitoring of TON and TOFF signals. | A | See Chapter 3.2.4 |
| Power Supply Monitoring | Under Voltage Lock-Out function on V_{CC1} , V_{CC2} and V_{EE2} ; Over Voltage Lock-Out on V_{EE2} and V_{CC2} . | B | See Chapter 3.3.1 |
| Internal Supervision | Monitoring of the key internal functions of the chip. | B | See Chapter 3.3.2 |
| STP | Shoot Through Protection. | C | See Chapter 3.4.1 |
| Gate Monitoring | Monitoring of the GATE voltage during a switching sequence. | C | See Chapter 3.4.2 |
| Temperature Monitoring | Over temperature warning for the driver. | C | See Chapter 3.4.3 |
| SPI Error Detection | SPI Error Detection. | C | See Chapter 3.4.4 |
| Active Short Circuit Support | V_{CC2} not valid error notification | C | See Chapter 3.4.5 |
| WTO | Weak Turn-On Functionality | D | See Chapter 3.5.2 |
| DESAT Supervision | Supervision of the DESAT function during application life time. | D | See Chapter 3.5.3 , Chapter 3.5.4 and Chapter 3.5.5 |
| OCP Supervision | Supervision of the OCP function during application life time. | C & D | See Chapter 3.5.6 , Chapter 3.5.7 and Chapter 3.2.2 |
| Power Supply Monitoring Supervision | Supervision of the OVLO / UVLO function during application life time. | D | See Chapter 3.5.8 |
| Internal Clock Supervision | Plausibility check of the frequency of the internal oscillator. | D | See Chapter 3.5.9 |

Table 3-1 Safety Related Functions (cont'd)

| Protection Feature | Description | Category | Comments |
|------------------------|---|----------|-----------------------------------|
| TTOFF | Two Level Turn-Off | E | See Chapter 2.4.6 |
| SPI Communication | SPI Communication (using register PRW). | E | See Chapter 4.1 |
| Overvoltage robustness | Robustness against transient overvoltage on power supply. | E | See Chapter 5.2 |

From the conceptual point of view, the protection functions can be clustered into five main categories.

- Category A corresponds to the functions where the device “decides on its own”, after the detection of an Event Class A, to change the state of the output stage and to disable itself. A dedicated action from the user is needed to reactivate the device (fast reactivation).
- Category B corresponds to the functions where the device “decides on its own”, after the detection of an Event Class B, to change the state of the output stage and to disable itself. A complete reinitialization from the user is needed to reactivate the device (slow reactivation).
- Category C corresponds to the functions that only issue a notification in case an error is detected.
- Category D are intrusive supervision functions, aimed at being started when the application is not running.
- Category E corresponds to implemented functions or capabilities supported by the device whose use can enhance the overall safety coverage of the application.

3.2 Protection Functions: Category A

3.2.1 Desaturation Protection

The integrated desaturation (DESAT) functionality is summarized in [Table 3-2](#):

Table 3-2 DESAT Protection Overview

| Parameter | Short Description |
|---------------------------------|--|
| Function | Monitoring of the V_{CE} voltage of the IGBT. |
| Periodicity | Continuous while device issues a PWM ON command. |
| Action in case of failure event | <ol style="list-style-type: none"> 1. Emergency (Safe) Turn-off Sequence. 2. Error Flag SER.DESATER is set. 3. Assertion of signal NFLTA. |
| Programmability | Yes (blanking time). |
| In-System Testability | Yes (see also Chapter 3.5.3 and Chapter 3.5.4). |

The DESAT function aims at protecting the IGBT in case of short circuit. The voltage drop V_{CE} over the IGBT is monitored via the **DESAT** pin while the device issues a PWM ON command. The voltage at pin **DESAT** is externally filtered by an external RC filter, and decoupled by an external diode (see [Figure 3-1](#)). The DESAT voltage is compared to an internal reference voltage. The result of this comparison is available by reading bit **SSTAT2.DSATC**.

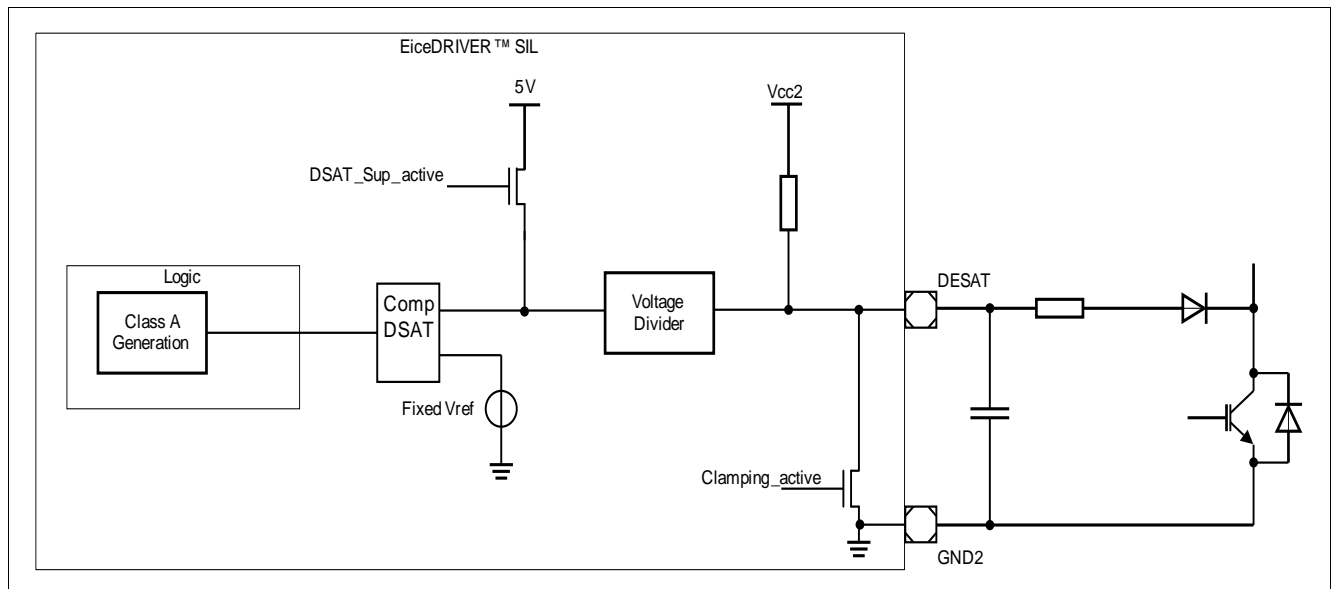


Figure 3-1 DESAT Function: Diagram of Principle

At the beginning of a turn-on sequence, the voltage at pin **DESAT** is forced to Low level for the duration the blanking time defined by register **SDESAT**. Once the blanking time has elapsed, the voltage at pin **DESAT** is released and is compared to an internal reference voltage. Depending on the value of the decoupling capacitance, an additional “analog” blanking time will be added corresponding to the charging of the capacitance through the internal pull-up resistance ([Figure 3-2](#)).

In case the measured voltage is higher than the internal threshold, an Emergency (Safe) Turn-Off sequence is initiated, bit **SER.DESATER** is set and a fault notification is issued on pin **NFLTA** (in case of an OPM transition the state machine - see [Chapter 2.4.7](#)).

The DESAT function is not active while the output stage is in PWM OFF state.

The blanking time needs to be chosen carefully, since the DESAT protection may be *de facto* inhibited if the PWM ON-time is too short compared to the chosen blanking time.

At turn-off, the DESAT signal is pulled down for the duration of the TTOFF plateau time, and extended by the blanking time once the hard turn off sequence is initiated.

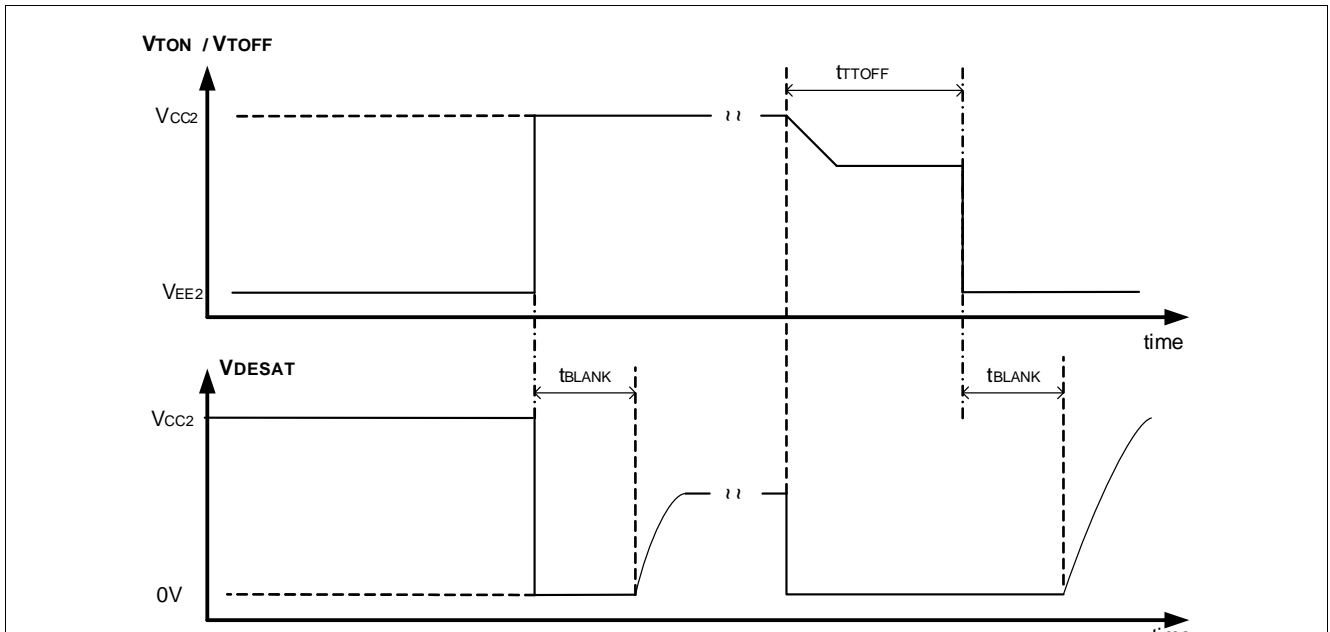


Figure 3-2 DESAT Operation

Note: . In case the **DESAT** pin is open, the pull-up resistance ensures that a DESAT event is generated at the next PWM turn-on command.

DESAT Clamping during turn-off

The internal pull-up resistance may lead to the unwanted charging of the DC-link capacitance via the DESAT pin. In order to overcome this, the DESAT function needs to be activated by clearing bit **SCFG.DSTCEN**. When this bit is set, pin **DESAT** is internally clamped to GND2 when a PWM off command is issued by the device.

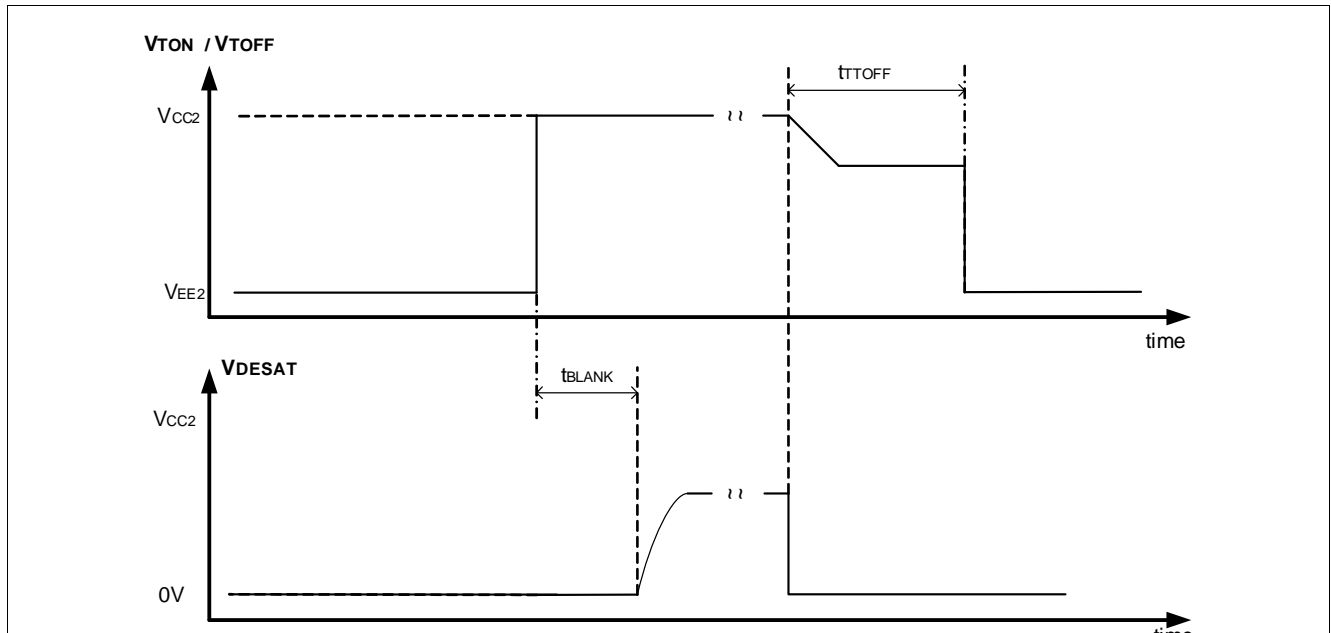


Figure 3-3 DESAT Operation with DESAT clamping enabled

3.2.2 Overcurrent Protection

The integrated Over Current Protection (OCP) functionality is summarized in [Table 3-3](#):

Table 3-3 OCP Function Overview

| Parameter | Short Description |
|---------------------------------|--|
| Function | Monitoring of the voltage drop over an external resistor located on the auxiliary emitter path of the IGBT. |
| Periodicity | Continuous while device issues a PWM ON command. |
| Action in case of failure event | <ol style="list-style-type: none"> 1. Emergency (Safe) Turn-off Sequence. 2. Error Flag SER.OPPER is set. 3. Assertion of signal NFLTA. |
| Programmability | No |
| In-System Testability | Yes (see Chapter 3.5.6). |

The integrated Over Current Protection (OCP) function aims at protecting the IGBT in case of overcurrent and short-circuit conditions. The voltage drop over a sense resistor located on the auxiliary emitter path of the IGBT is monitored via the **OCP** while the device issues a PWM ON command. The voltage at pin **OCP** is externally filtered by an (optional) RC filter and compared (using several internal voltage comparators) to the internal reference thresholds V_{OCPD1} and V_{OCPD2} (see [Figure 3-4](#)). The result of these comparisons is available by reading bits **SSTAT2.OCPC1** and **SSTAT2.OCPC2**.

*Note: Bits **SSTAT2.OCPC1** and **OCPC2** are blanked by the selected blanking time.*

At the beginning of a turn-on sequence, the internal evaluation of the voltage at pin **OCP** is inhibited for the duration the blanking time defined by register **SOCP**. Once the blanking time has elapsed, the voltage at pin **OCP** is compared to an internal reference voltage.

In case the measured voltage at pin **OCF** is higher than the internal threshold V_{OCFD1} , an Emergency (Safe) Turn-off sequence is initiated, bit **SER.OCFER** is set and a fault notification is issued on pin **NFLTA** (in case of an OPM transition the state machine - see [Chapter 2.4.7](#)). In case the measured voltage at pin **OCF** is higher than the internal threshold V_{OCFD2} , the sticky bit **SSTAT.OCPCD** is set. This allows to verify during application run time the signal integrity of the sense path. The OCP function is not active while the output stage is in PWM OFF state.

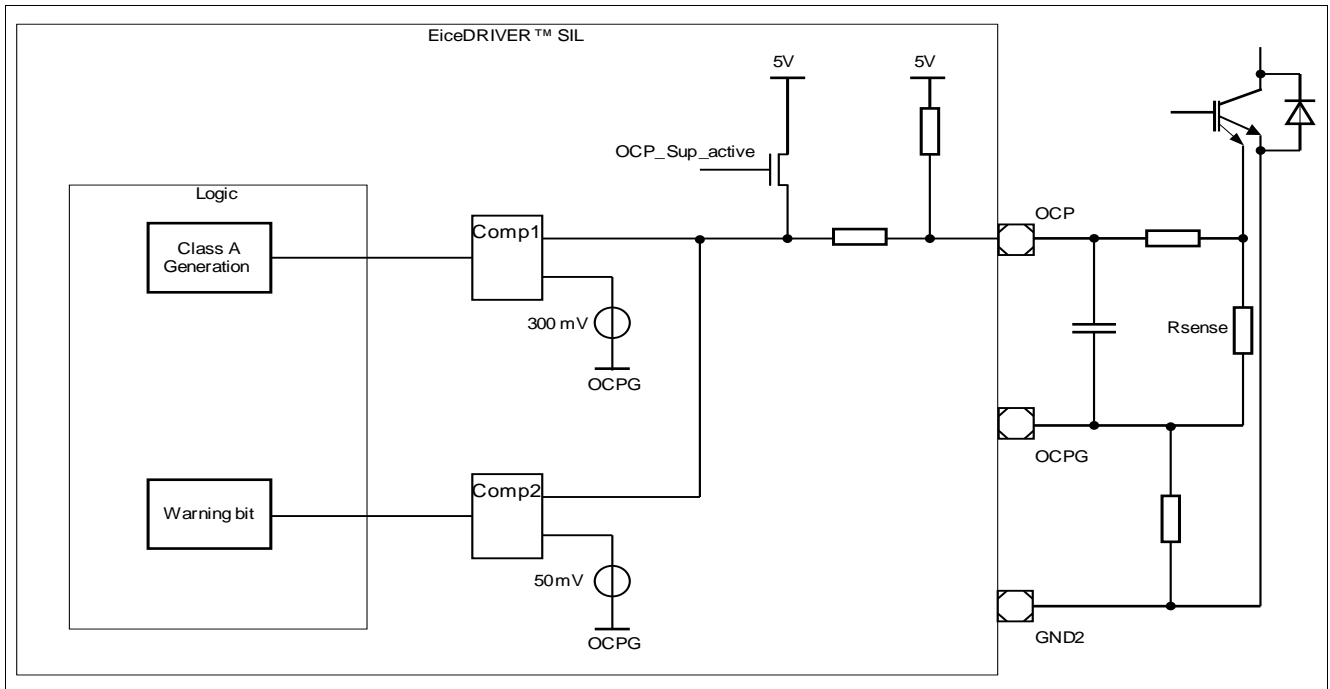


Figure 3-4 OCP Function: Principle of Operation

Note: Both DESAT and OCP protection mechanisms can be used simultaneously.

*Note: In case the **OCF** pin is open, the pull-up resistance ensures that an OCP event is generated.*

3.2.3 External Enable

The External Enable functionality is summarized in [Table 3-4](#):

Table 3-4 External Enable Function Overview

| Parameter | Short Description |
|---------------------------------|--|
| Function | External Enable. |
| Periodicity | Invalid signal on EN pin. |
| Action in case of failure event | <ol style="list-style-type: none"> 1. Emergency (Regular) Turn-off Sequence. 2. Error Flag PER.ENER is set. 3. Assertion of signal NFLTA. |
| Programmability | No. |
| In-System Testability | Yes. |

The functionality of the signal at pin [EN](#) is given in [Chapter 2.4.8](#). In case of a Valid-to-Invalid signal transition, an error is detected. In this case, an Emergency (Regular) turn-off sequence is initiated, bit [PER.ENER](#) is set and a fault notification is issued on pin [NFLTA](#) (in case of an OPM transition the state machine - see [Chapter 2.4.7](#)). The current validity state of the signal at pin [EN](#) can be read on bit [PSTAT2.ENVAL](#).

This function can be tested by generating an invalid signal on pin [EN](#) and verifying that the actions done by the device correspond to the expected behavior.

3.2.4 Output Stage Monitoring

The Output Stage Monitoring functionality is summarized in [Table 3-5](#):

Table 3-5 Output Stage Monitoring Overview

| Parameter | Short Description |
|---------------------------------|---|
| Function | Monitoring of signals TON and TOFF . |
| Periodicity | Continuous. |
| Action in case of failure event | <ol style="list-style-type: none"> 1. Tristate Output Stage (bit SSTAT.HZ set) 2. Bit SCTRL.OSTC and error Flag SER.OSTER are set. 3. Assertion of signal NFLTA. |
| Programmability | Yes (can be disabled). |
| In-System Testability | Yes. |

Signals **TON** and **TOFF** are normally connected to an external booster ([Figure 5-1](#)). In case the inputs of the booster can not be driven (e.g. short circuit), the resulting high currents may lead to the destruction of the 1EDI2001AS and / or of the booster. This failure case is avoided thanks to the Output Stage Monitoring function.

When levels at **TON** and **TOFF** differ from the expected levels, the output stage is tristated and bit **SSTAT.HZ** is set. A transition of bit **SSTAT.HZ** from 0_B to 1_B generates an Event Class A: bit **SCTRL.OSTC** and error flag **SER.OSTER** are set, signal **NFLTA** is asserted (see [Chapter 2.4.7](#)).

The monitoring is continuous, but is inhibited for the inhibition time t_{OSM} after commutation. At turn-on, time t_{OSM} is counted from the beginning of the turn-on sequence. At turn-off, time t_{OSM} is counted from the moment where the hard switching action takes place (after the TTOFF plateau). Signal **TON** is compared against V_{OSMON} . Signal **TOFF** is compared against V_{OSMOF} .

*Note: Bit **SCTRL.OSTC** is cleared either by setting bit **PCTRL.CLRS** or by a falling edge of signal **OSD**.*

In OPM5 and OPM6, Output Stage Monitoring for **TON** is disabled.

Output Stage Monitoring is disabled when the device is already in tristate (for example, when pin **OSD** is at High Level). The Output Stage returns from tristate to normal conditions when bit **SSTAT.HZ** is cleared. Clearing bit **SSTAT.HZ** reactivates the OSM (after the duration of the blanking time).

*Note: The OSM can be permanently disabled by setting bit **SCFG.OSMD**, for both **TON** and **TOFF**.*

The OSM can be tested on system level by (for example) pulling the IGBT gate signal high while the device issues a PWM Low command. This can be done for example in combination with the ASC function of Infineon's 1EBN100XAE "EiceDRIVER™ Boost" booster stage. It can then be verified that the reaction of the device corresponds to the expected behavior.

3.3 Protection Functions: Category B

3.3.1 Power Supply Voltage Monitoring

The Power Supply Voltage Monitoring functionality is summarized in [Table 3-6](#):

Table 3-6 Power Supply Voltage Monitoring Overview

| Parameter | Short Description |
|---------------------------------|---|
| Function | Monitoring of V_{CC1} , V_{CC2} , V_{EE2} . |
| Periodicity | Continuous. |
| Action in case of failure event | <ol style="list-style-type: none"> Emergency (Regular) Turn-off Sequence. Error Flag PER.RST1 (UVLO1) or SER.UVLO2ER or OVLO2ER or UVLO3ER or OVLO3ER is set. Assertion of signal NRST/RDY (UVLO1 only) or NFLTb. |
| Programmability | No. |
| In-System Testability | Yes (see Chapter 3.5.8). |

In order to ensure a correct switching of the IGBT, the device supports an undervoltage lockout (UVLO) function for V_{CC1} , V_{CC2} , V_{EE2} , and an overvoltage lockout (OVLO) function for V_{CC2} and V_{EE2} ([Figure 3-5](#)).

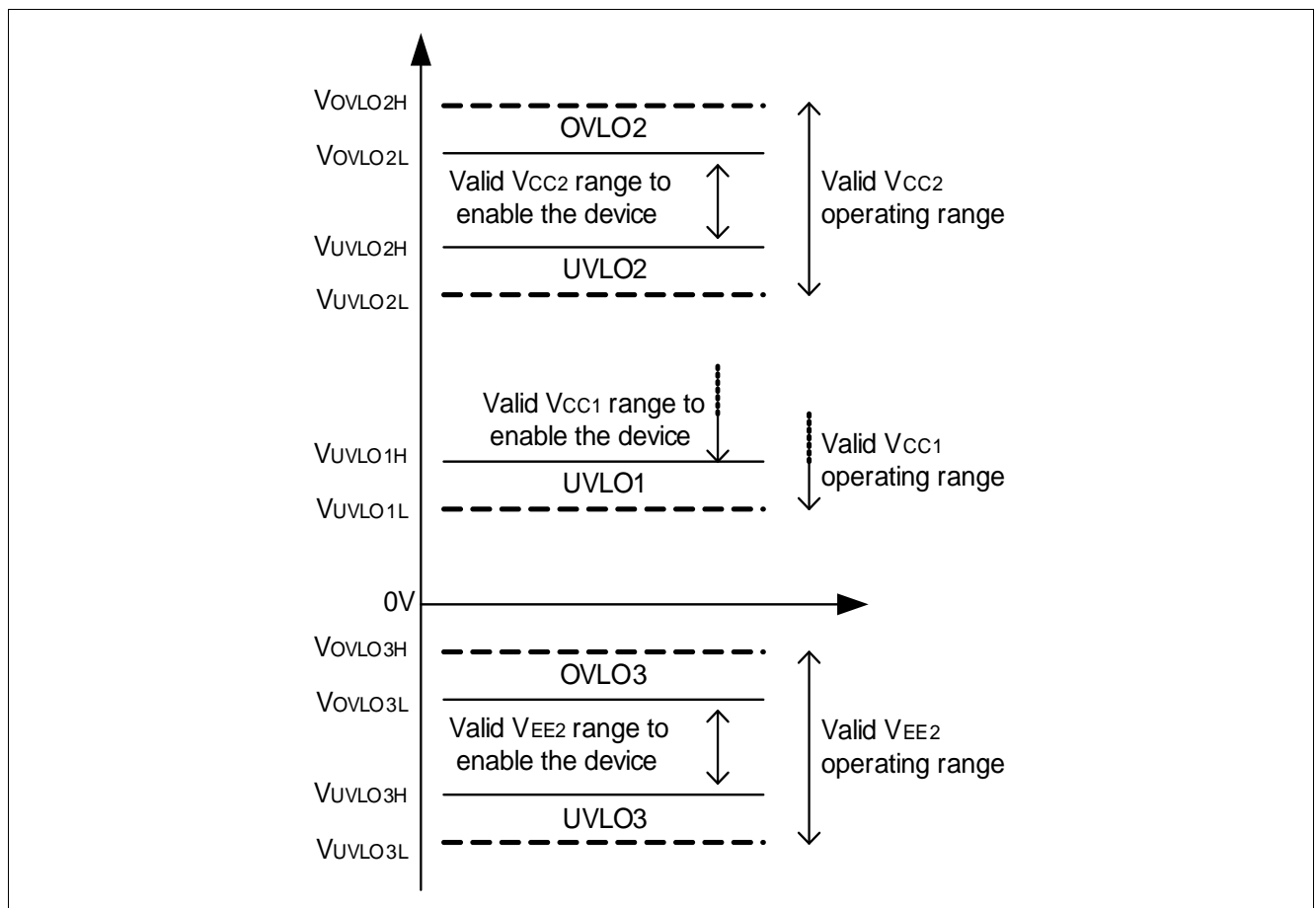


Figure 3-5 Power Supply Supervision Function

The V_{CC1} voltage is compared (using an internal voltage comparator) to an internal reference threshold. If the power supply voltage V_{CC1} of the primary chip drops below V_{UVLO1L} , an error is detected. In this case, an emergency (Regular) turn-off sequence is initiated and signal **NRST/RDY** goes low. In case V_{CC1} reaches afterwards a level higher than V_{UVLO1H} , then the error condition is removed and signal **NRST/RDY** is deasserted. Besides, bit **PER.RST1** is set.

The V_{CC2} voltage is compared (using an internal voltage comparator) to an internal reference threshold. If the power supply voltage V_{CC2} of the secondary chip drops below V_{UVLO2L} , an error is detected. In this case, an emergency (Regular) turn-off sequence is initiated, bit **SER.UVLO2ER** is set and signal **NFLTB** is activated (in case of an OPM transition the state machine - see [Chapter 2.4.7](#)). In case V_{CC2} reaches afterwards a level higher than V_{UVLO2H} , then the error condition is removed and the device can be reenabled.

The V_{CC2} voltage is compared (using an internal voltage comparator) to an internal reference threshold. If the power supply voltage V_{CC2} of the secondary chip goes above V_{OVLO2H} , an error is detected. In this case, an emergency (Regular) turn-off sequence is initiated, bit **SER.OVLO2ER** is set and signal **NFLTB** is activated (in case of an OPM transition the state machine - see [Chapter 2.4.7](#)). In case V_{CC2} reaches afterwards a level below V_{OVLO2L} , then the error condition is removed and the device can be reenabled.

The V_{EE2} voltage is compared (using an internal voltage comparator) to an internal reference threshold. If the power supply voltage V_{EE2} of the secondary chip drops below V_{UVLO3L} , an error is detected. In this case, an emergency (Regular) turn-off sequence is initiated, bit **SER.UVLO3ER** is set and signal **NFLTB** is activated (in case of an OPM transition the state machine - see [Chapter 2.4.7](#)). In case V_{EE2} reaches afterwards a level higher than V_{UVLO3H} , then the error condition is removed and the device can be reenabled.

The V_{EE2} voltage is compared (using an internal voltage comparator) to an internal reference threshold. If the power supply voltage V_{EE2} of the secondary chip goes above V_{OVLO3H} , an error is detected. In this case, an emergency (Regular) turn-off sequence is initiated, bit **SER.OVLO3ER** is set and signal **NFLTB** is activated (in case of an OPM transition the state machine - see [Chapter 2.4.7](#)). In case V_{EE2} reaches afterwards a level below V_{OVLO3L} , then the error condition is removed and the device can be reenabled. **NFLTB**

The current status of the error detection of OVLO2, UVLO3 and OVLO3 mechanism is available by reading bit **SSTAT2.UVLO2M**, **OVLO2M**, **UVLO3M** or **OVLO3M** respectively.

Note: In case V_{CC2} goes below the voltage V_{RST2} , the secondary chip is kept in reset state.

3.3.2 Internal Supervision

The Internal Supervision functionality is summarized in [Table 3-7](#):

Table 3-7 System Supervision Overview

| Parameter | Short Description |
|---------------------------------|---|
| Function | Monitoring of the key internal functions of the chip. |
| Periodicity | Continuous. |
| Action in case of failure event | See below |
| Programmability | No. |
| In-System Testability | No. |

The primary and secondary chips are equipped with internal verification mechanisms ensuring that the key functions of the device are operating correctly. The internal blocks which are supervised are listed below:

- Lifesign watchdog: mutual verification of the response of both chips (both primary and secondary).
- Oscillators (both primary and secondary, including open / short detection on signals **IREF1** and **IREF2**).
- Memory error (both primary and secondary).

3.3.2.1 Lifesign watchdog

The primary and the secondary chips monitor each other by the mean of a lifesign signal. The periodicity of the lifesign is typically t_{LS} . Each chip expects a lifesign from its counterpart within a given time window. In case two consecutive lifesign errors are detected by a chip, an Event Class B is generated. Depending on which side has detected the error, either bit **PER.CER1** or **SER.CER2** is set.

*Note: Bits **PER.CER1** and **SER.CER2** indicate a loss of communication event. The current status of the internal communication is indicated by bit **PSTAT.SRDY**.*

3.3.2.2 Oscillator Monitoring

The main oscillators on the primary and on the secondary side are monitored continuously. Two distinct mechanisms are used for this purpose:

- Lifesign Watchdog allows to detect significant deviations from the nominal frequency (both primary and secondary, see above).
- Open / short detection on pin **IREF1**.
- Open detection on pin **IREF2**.

In case a failure is detected on pin **IREF1**, the primary chip is kept in reset state for the duration of the failure and signal **NRST/RDY** is asserted. This leads to the detection of a lifesign error by the secondary chip, generating thus an Event Class B.

In case a failure is detected on pin **IREF2**, an Emergency (regular) Turn-Off sequence is initiated. The secondary chip is kept in reset state for the duration of the failure. This leads to the detection of a lifesign error by the primary chip, generating thus an Event Class B.

3.3.2.3 Memory Supervision

The configuration parameters of the device, stored in the registers, are protected with a parity bit protection mechanism. Both primary and secondary chips are protected (refer to **Chapter 4**).

In case a failure is detected on the primary chip, it is kept in reset state, and both signal **NRST/RDY** and **NFLTb** are asserted. The secondary side initiates an Emergency (Regular) Turn-Off sequence.

In case a memory failure is detected by the secondary chip, an Emergency (Regular) Turn-Off sequence is initiated. The secondary chip is kept in reset state for the duration of the failure. This leads to the detection of a lifesign error by the primary chip, generating thus an Event Class B.

3.4 Protection Functions: Category C

3.4.1 Shoot Through Protection function

The Shoot Through Protection (STP) functionality is summarized in [Table 3-8](#):

Table 3-8 STP Overview

| Parameter | Short Description |
|---------------------------------|---|
| Function | Prevents both High-Side and Low-Side Switches to be activated simultaneously. |
| Periodicity | Continuous. |
| Action in case of failure event | 1. The signal at pin INP is inhibited. 2. Error Flag PER.STPER is set. |
| Programmability | No. |
| In-System Testability | Yes. |

With the implemented STP function, a low-side (resp. high-side) device is able to monitor the status of its high-side (resp. low-side) counterpart. The input pin **INSTP** provides an input for the PWM signal of the driver's counterpart ([Figure 3-6](#)).

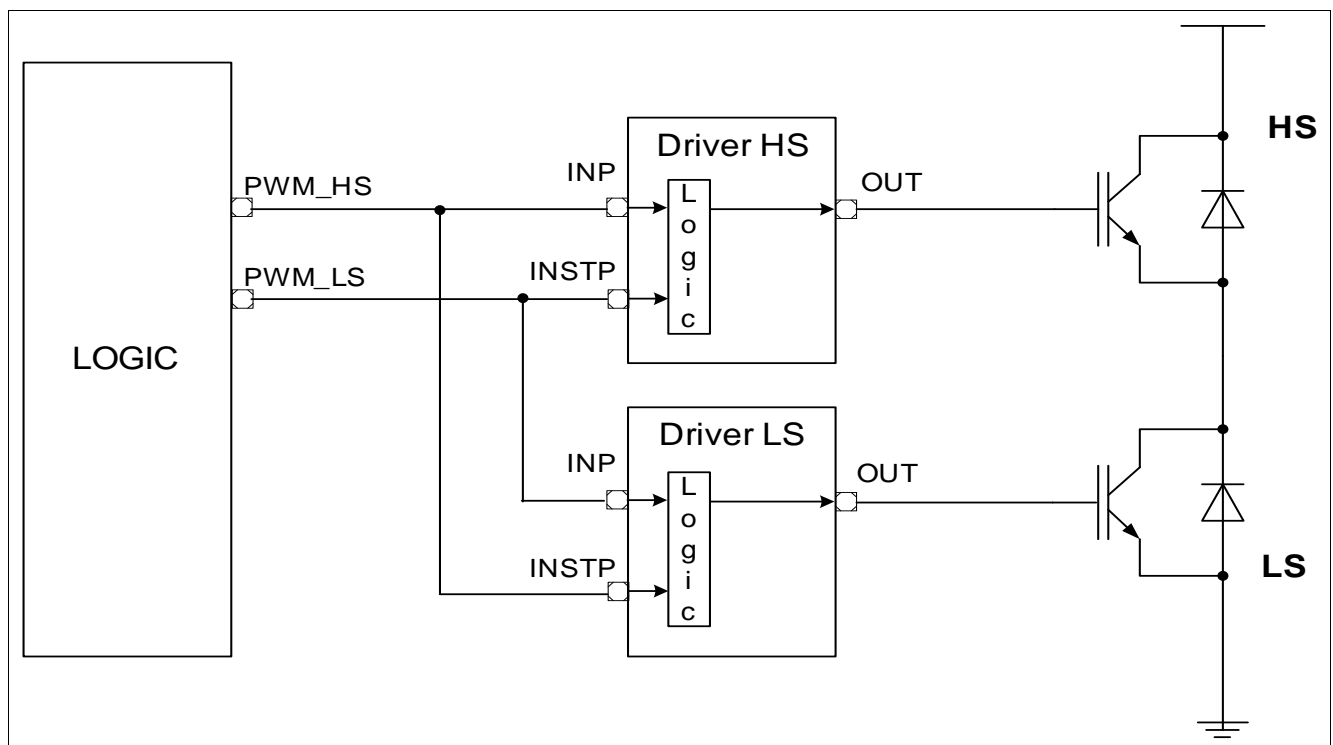


Figure 3-6 Shoot Through Protection: Principle of Operation

In case one of the driver is in ON state, the driver's counterpart PWM input is inhibited, preventing it to turn-on (See [Chapter 2.4.3](#)). A minimum dead time is defined by hardware. Conceptually, the STP aims at providing an additional "line of defense" for the system in case erroneous PWM commands are issued by the primary logic. In normal operation, dead time management shall be performed at the microcontroller level.

In case a PWM ON command is received on pin **INP** during the inhibition time, a failure event is detected. In this case, the high level at pin **INP** is ignored and bit **PER.STPER** is set.

Note: Internal filter ensures that STPER is not set for glitches smaller than approximately 50ns.

The STP can be tested by applying non valid INSTP and INP and by checking bit **PSTAT2.STP**.

The STP can not be disabled. However, setting pin **INSTP** to V_{GND1} deactivates de facto the function.

3.4.2 Gate Monitoring

The Gate Monitoring functionality is summarized in **Table 3-9**:

Table 3-9 Gate Monitoring Overview

| Parameter | Short Description |
|---------------------------------|---|
| Function | Monitors the waveform at pin GATE . |
| Periodicity | Timeout detection at every PWM command transition. Exact timing measurement on request. |
| Action in case of failure event | Flag PER.GER is set. |
| Programmability | No |
| In-System Testability | Yes |

The goal of this function is to allow a plausibility check on the IGBT gate voltage signal waveform during a switching sequence, for example in order to track degradations of the IGBT gate resistances.

The Gate Monitoring consists in two functions: Gate Timeout and Gate Timing Capture.

Gate Timeout

The Gate Timeout mechanism is active for both turn-on and turn-off sequence. At the beginning of a turn-on sequence, an internal 8-bit timer (in the clock domain OSC2) is cleared and starts counting up. When the gate voltage reaches V_{GATE2} , the timer stops. In case the timer overflows, flag **PER.GER** is set.

A similar mechanism is initiated at every turn-off sequence (regular or safe). When a **hard** transition occurs, an internal timer is cleared starts counting up. When the gate voltage reaches the value V_{GATE1} , the timer stops. In case the timer overflows, flag **PER.GER** is set.

The Gate Timeout mechanism is always active, except in OPM5 and OPM6. In OPM5 and OPM6, the Gate Timeout mechanism is disabled during turn-on sequences. It works however normally for turn-off sequences

Gate Timing Capture

This function is armed when an SPI command sets bit **PCTRL.GTCT**. This sets both bits **SGM1.GTCT1** and **SGM2.GTCT2** which indicates that the function is armed. At the next turn-on, respectively turn-off, sequence, a timing measurement is performed. At the beginning of a turn-on sequence, bit field **SGM2.VTOM2** is cleared and the device starts incrementing an internal counter (in the clock domain of SSOSC2). When signal **GATE** reaches voltage V_{GATE2} , the value of the timer is stored in bit field **SGM2.VTOM2** and bit **SGM2.GTCT2** is cleared. In case the timer overflows, value FF_H is stored.

Similarly, at the **hard** transition of a turn-off sequence, bit field **SGM1.VTOM1** is cleared and the device starts incrementing an internal counter (in the clock domain of SSOSC2). When signal **GATE** reaches voltage V_{GATE1} , the value of the timer is stored in bit field **SGM1.VTOM1** and bit **SGM1.GTCT1** is cleared. In case the timer overflows, value FF_H is stored.

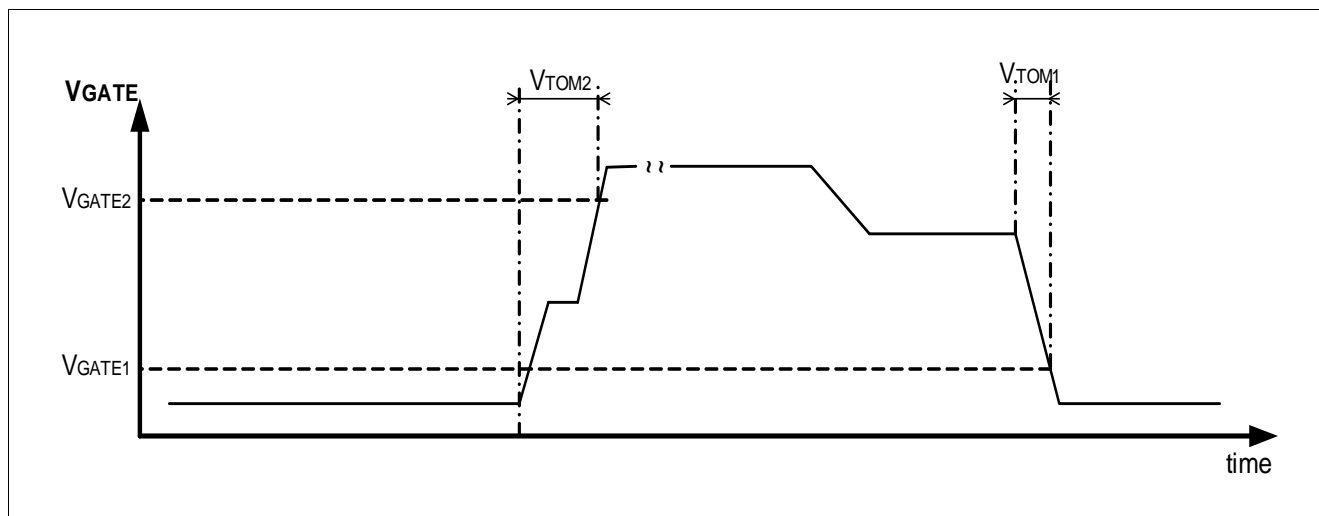


Figure 3-7 Gate Monitoring Function: Timing Definition

The Gate Monitoring can be tested on system level by (for example) pulling the IGBT gate signal high while the device issues a PWM Low command. This can be done for example in combination with the ASC function of Infineon's 1EBN100XAE "EiceDRIVER™ Boost" booster stage. It can then be verified that the reaction of the device corresponds to the expected behavior.

3.4.3 Temperature Monitoring

The Temperature Monitoring functionality is summarized in [Table 3-10](#):

Table 3-10 Temperature Monitoring Overview

| Parameter | Short Description |
|---------------------------------|--------------------------------------|
| Function | Warning in case of over-temperature. |
| Periodicity | Continuous. |
| Action in case of failure event | Flag PER.OTER is set. |
| Programmability | No |
| In-System Testability | No |

The device is equipped with an internal temperature sensor. In case the value measured by the internal sensor temperature exceeds a given threshold, bit **PER.OTER** is set.

3.4.4 SPI Error Detection

The SPI Error Detection mechanisms are summarized in [Table 3-11](#):

Table 3-11 SPI Error Detection Overview

| Parameter | Short Description |
|---------------------------------|---|
| Function | Non valid SPI command detection and notification. |
| Periodicity | Continuous. |
| Action in case of failure event | Flag PER.SPIER is set. |

Table 3-11 SPI Error Detection Overview (cont'd)

| Parameter | Short Description |
|-----------------------|-------------------------------|
| Programmability | Yes (parity can be disabled). |
| In-System Testability | Yes. |

For more details, see [Chapter 2.4.4.4](#).

The SPI Error Detection Mechanism can be tested by inserting on purpose a dedicated error and by verifying that the device's reaction is conform to specification.

3.4.5 Active Short Circuit Support

The Active Short Circuit Support Function is summarized in [Table 3-12](#):

Table 3-12 Active Short Circuit Support Overview

| Parameter | Short Description |
|---------------------------------|---|
| Function | Notification in case V_{CC2} is below the UVLO2 threshold or internal digital supply not valid. |
| Periodicity | Continuous. |
| Action in case of failure event | Signal NUV2 activated. |
| Programmability | No. |
| In-System Testability | Yes. |

This feature is aimed at being used in combination with a booster device supporting a direct turn-on input (pin ASC, see [Figure 3-8](#)). Any time the voltage V_{CC2} goes below threshold V_{UVLO2L} , or the internal digital voltage supply is not valid, the open drain pin **NUV2** drives a low level for the duration of the event.

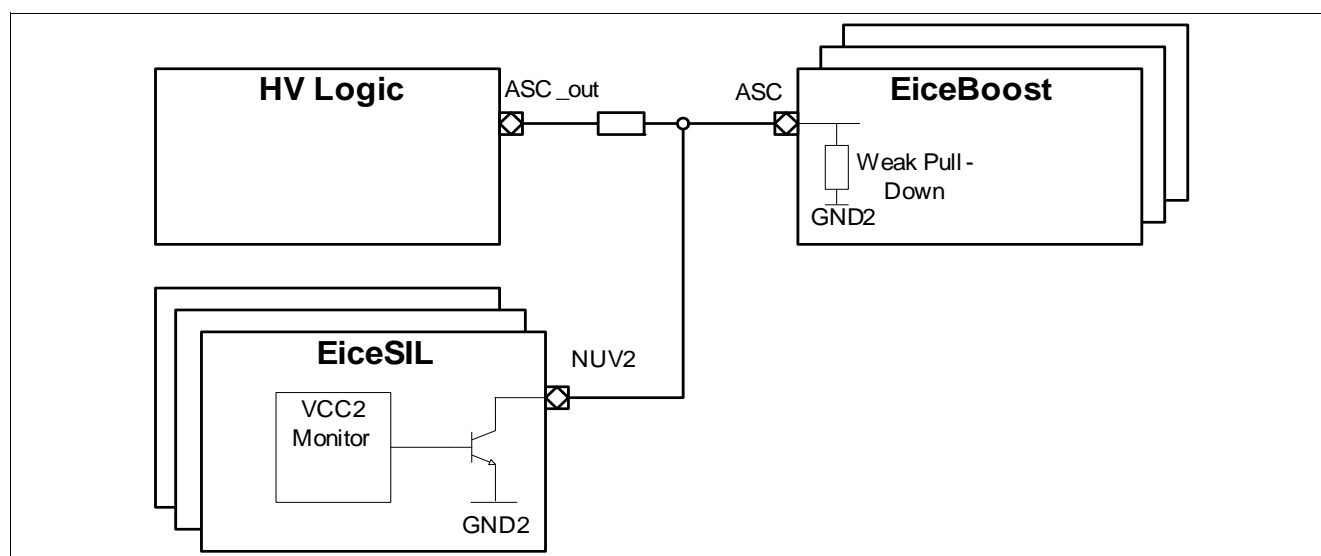


Figure 3-8 ASC Strategy Support

The **NUV2** pin functionality can be tested on system level by creating the conditions of its activation and verifying that the reaction of the device corresponds to the expected behavior.

3.5 Protection Functions: Category D

3.5.1 Operation in Verification Mode and Weak Active Mode

Verification Mode and Weak Active Mode are used to start intrusive test functions on device and system level, in order to verify during life time safety relevant functions. The following functions are supported in Verification and Weak Active Mode:

- Weak Turn-On
- DESAT Supervision Level 1
- DESAT Supervision Level 2
- DESAT Supervision Level 3
- OCP Supervision Level 1
- OCP Supervision Level 3
- UVLOx and OVLOx Supervision Level 1
- Internal Clock Supervision
- Timing Calibration Feature

Intrusive test functions can only be started once a correct sequence of SPI commands has been received after reset. The implementation of the device ensures that no intrusive function can be started when the device is normally active.

A time-out function ensures that the device quits OPM5 or OPM6 to OPM1 after a hardware defined time.

The verification functions are triggered by setting the corresponding bit fields in registers **PSCR** or **SSCR** in OPM2. The settings are then activated in OPM5. Only one verification function should be activated at the time.

In OPM5 and OPM6, Gate Monitoring for High level and Output Stage Monitoring on pin **TON** are disabled

*Note: In OPM5 and OPM6 mode, it is recommended to have bit field **SSTOF.STVAL** programmed to 0_H.*

3.5.2 Weak Turn On

The Weak-Turn On (WTO) corresponds to the operation when Mode OPM6 is active.

The purpose of the Weak Turn-On functionality is to perform a “probe” test of the IGBT, by switching it on with a reduced gate voltage, in order to limit the current through it in case of overcurrent conditions. This allows to avoid high currents when the system has no memory of the previous state.

In Mode OPM6, when the driver initiates a turn-on sequence after the reception of a PWM command, the ON voltage at signal **TON** is defined by bit field **SCTRL.GPONS**. **Figure 3-9** shows an idealized weak turn-on sequence.

The device allows for external booster voltage compensation at the IGBT gate. When bit **SCFG2.VBEC** is cleared, the voltage at **TON** at the plateau corresponds to the programmed value. When bit **SCFG2.VBEC** is set, an additional V_{BE} (base emitter junction voltage of an internal pn diode) is subtracted to the programmed voltage at **TON** in order to compensate for the V_{BE} of an external booster.

Note: When using WTO, it is recommended to have the selected TTOFF (if active) plateau at a smaller voltage than the WTO voltage.

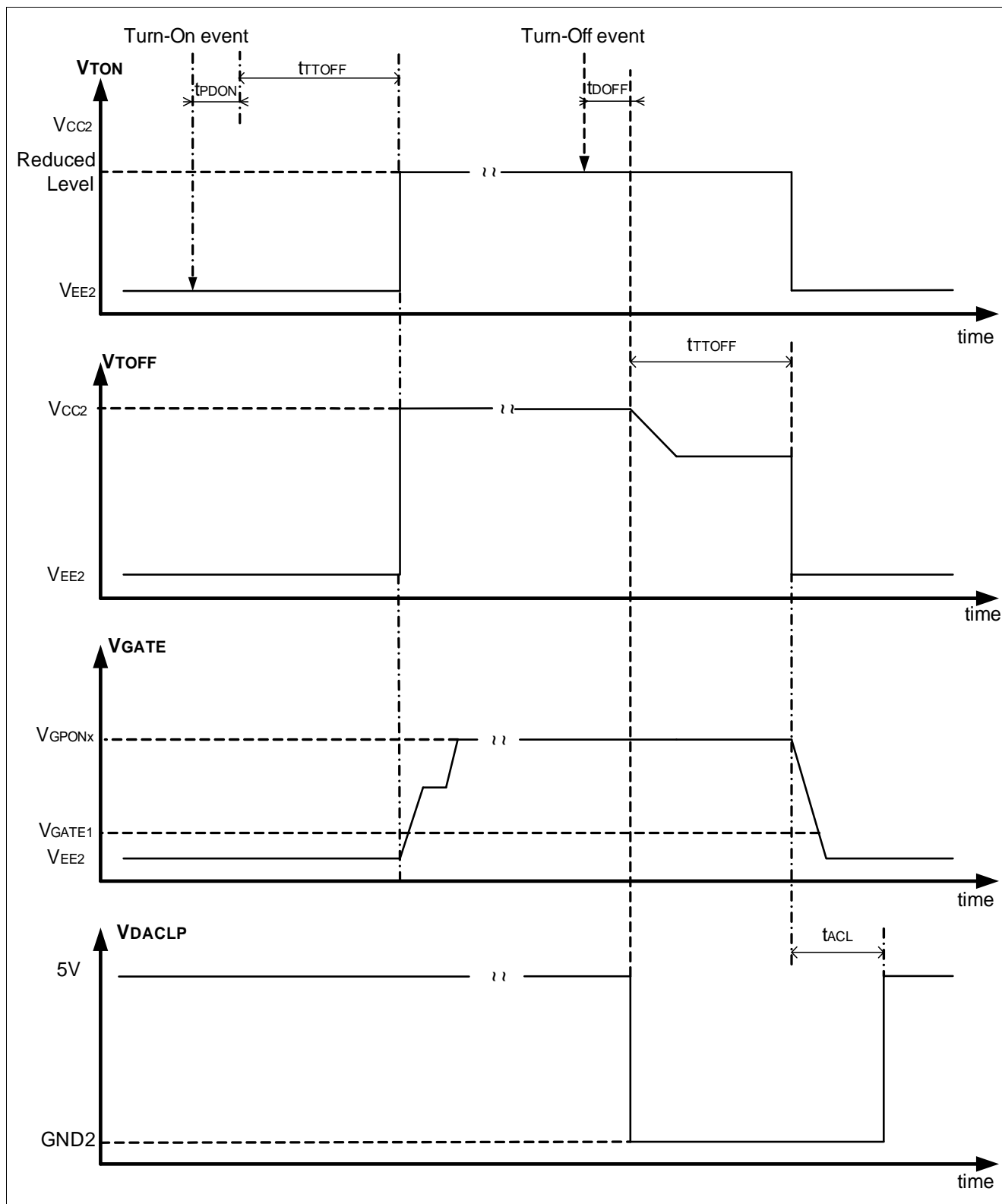


Figure 3-9 Idealized Weak Turn-On Sequence

3.5.3 DESAT Supervision Level 1

The DESAT Supervision Level 1 functionality is summarized in [Table 3-13](#):

Table 3-13 DESAT Supervision Level 1 Overview

| Parameter | Short Description |
|---------------------------------|---|
| Function | Supervision of the DESAT functionality. |
| Periodicity | On request. |
| Action in case of failure event | N.a. |
| Programmability | No |
| In-System Testability | No |

The purpose of the DESAT Supervision Level 1 function is to verify that the DESAT feature is operational over the whole life time of the application. Since the DESAT supervision is intrusive, it is intended to be executed when the device is in Mode OPM5 and OPM6 (e.g. after power-up during the initialization phase). This mechanism aims at generating artificially a DESAT error, verifying that it is recognized by the device and that an error notification is correctly issued to the primary logic.

When this function is triggered, the driver enters a special mode where the signal input of the comparator is internally pulled up above the threshold voltage (see [Figure 3-1](#)). The DESAT function works normally otherwise. When the device enters OPM6 and turns on, after the blanking time has elapsed, a DESAT error is generated, with the corresponding actions being triggered by the device.

The **INP** signal is issued at the output stage (weak turn-on).

3.5.4 DESAT Supervision Level 2

The DESAT Supervision Level 2 functionality is summarized in [Table 3-14](#):

Table 3-14 DESAT Supervision Level 2 Overview

| Parameter | Short Description |
|---------------------------------|---|
| Function | Supervision of the DESAT functionality. |
| Periodicity | On request. |
| Action in case of failure event | N.a. |
| Programmability | No |
| In-System Testability | No |

The purpose of the DESAT Supervision Level 2 function is to verify that the DESAT feature is operational over the whole life time of the application. Since the DESAT supervision is intrusive, it is intended to be executed when the device is in Mode OPM5 and OPM6 (e.g. after power-up during the initialization phase). This mechanism aims at generating artificially a DESAT error, verifying that it is recognized by the device and that an error notification is correctly issued to the primary logic.

When this function is triggered, the driver enters a special mode where, as soon as the device is in OPM6 and a PWM turn-on command is received, no action is executed on the output stage. However, the DESAT logic works normally. It means that after the blanking time has elapsed, the voltage on pin DESAT should exceed the DESAT threshold level, leading to a DESAT error, with the corresponding actions being triggered by the driver.

The **INP** signal is not issued at the output stage.

3.5.5 DESAT Supervision Level 3

The DESAT Supervision Level 3 functionality is summarized in [Table 3-15](#):

Table 3-15 DESAT Supervision Level 3 Overview

| Parameter | Short Description |
|---------------------------------|---|
| Function | Supervision of the DESAT functionality. |
| Periodicity | On request. |
| Action in case of failure event | N.a. |
| Programmability | No |
| In-System Testability | No |

The purpose of the DESAT Supervision Level 3 function is to verify that the DESAT feature is operational over the whole life time of the application. Since the DESAT supervision is intrusive, it is intended to be executed when the device is in Mode OPM5 and OPM6 (e.g. after power-up during the initialization phase). This mechanism aims at generating artificially a DESAT error, verifying that it is recognized by the device and that an error notification is correctly issued to the primary logic.

When this function is triggered, the driver enters a special mode where the signal input of the comparator is internally pulled up above the threshold voltage (see [Figure 3-1](#)). When the device enters OPM6, independently from the PWM signal, a DESAT error is generated, with the corresponding actions being triggered by the device.

The **INP** signal is not issued at the output stage.

*Note: When using DESAT supervision Level 3, bit field **SSTOF.STVAL** must be programmed to 0_H*

3.5.6 OCP Supervision Level 1

The OCP Supervision functionality is summarized in [Table 3-16](#):

Table 3-16 OCP Supervision Level 1 Overview

| Parameter | Short Description |
|---------------------------------|---------------------------------------|
| Function | Supervision of the OCP functionality. |
| Periodicity | On Request. |
| Action in case of failure event | N.a. |
| Programmability | No |
| In-System Testability | No |

The purpose of the OCP Supervision Level 1 function is to verify that the OCP feature is operational over the whole life time of the application. Since the OCP supervision is intrusive, it is intended to be executed when the device is in Mode OPM5 and OPM6 (e.g. after power-up during the initialization phase). The main goal of this mechanism is to generate artificially an OCP error, to verify that it is recognized by the driver and that an error notification is correctly issued to the primary logic.

When this function is triggered, the driver enters a special mode where here the signal input of both comparators is internally pulled up above their respective threshold voltages (see [Figure 3-4](#)). The OCP function works normally otherwise. When the device enters OPM6 and turns on, after the blanking time has elapsed, an OCP error is generated, with the corresponding actions being triggered by the device.

The **INP** signal is issued at the output stage (weak turn-on).

3.5.7 OCP Supervision Level 3

The OCP Supervision functionality is summarized in [Table 3-17](#):

Table 3-17 OCP Supervision Level 3 Overview

| Parameter | Short Description |
|---------------------------------|---------------------------------------|
| Function | Supervision of the OCP functionality. |
| Periodicity | On Request. |
| Action in case of failure event | N.a. |
| Programmability | No |
| In-System Testability | No |

The purpose of the OCP Supervision Level 3 function is to verify that the OCP feature is operational over the whole life time of the application. Since the OCP supervision is intrusive, it is intended to be executed when the device is in Mode OPM5 and OPM6 (e.g. after power-up during the initialization phase). The main goal of this mechanism is to generate artificially an OCP error, to verify that it is recognized by the driver and that an error notification is correctly issued to the primary logic.

When this function is triggered, the driver enters a special mode where here the signal input of both comparators is internally pulled up above their respective threshold voltages (see [Figure 3-4](#)). When the device enters OPM6, independently from the PWM command, an OCP error is generated, with the corresponding actions being triggered by the device.

The **INP** signal is not issued at the output stage.

*Note: When using OCP supervision Level 3, bit field **SSTOF.STVAL** must be programmed to 0_H.*

3.5.8 Power Supply Monitoring Supervision

The Power Supply Monitoring Supervision monitoring functionality is summarized in [Table 3-18](#):

Table 3-18 Power Supply Monitoring Supervision Overview

| Parameter | Short Description |
|-------------------------|--|
| Function | Supervision of the Power Supply Monitoring Mechanisms. |
| Periodicity | On Request. |
| Action in case of event | N.a. |
| Programmability | No |
| In-System Testability | No |

The purpose of this supervision function is to verify that the Power Supply Monitoring functions (UVLO2, OVLO2, UVLO3, OVLO3) are operational over the whole life time of the application. Since this supervision is intrusive, it is intended to be executed when the device is in Mode OPM5 (e.g. after power-up during the initialization phase). The main goal of this mechanism is to generate artificially a power supply monitoring error, in order to verify that it is recognized by the driver and that an error notification is correctly issued to the primary logic.

When this function is triggered, the supervision mechanism of the power supply addressed by the command is activated. The internal threshold of the comparator delivers a “dummy” error, with the corresponding actions being triggered by the driver.

The supervision of UVLO1 is not supported by the device.

3.5.9 Internal Clock Supervision

The Primary Clock Supervision functionality is summarized in [Table 3-19](#):

Table 3-19 Primary Clock Supervision Overview

| Parameter | Short Description |
|-------------------------|--|
| Function | Supervision of the frequency of OSC1 and SSOSC2. |
| Periodicity | On Request. |
| Action in case of event | N.a. |
| Programmability | No |
| In-System Testability | No |

The clock supervision function consists on the primary clock supervision and the TCF feature.

Primary Clock Supervision

The purpose of this supervision function is to verify the frequency deviation of the primary clock. This function works in such a way that the PWM input signal is used to start and stop a counter clocked by OSC1. The function is activated when the device is in OPM5 or OPM6. The counter is incremented for the duration of the High level at pin **INP**. At a High-to-Low transition at pin INP, the counter is stopped, and its content is transferred to bit field **PCS.CS1**. A plausibility check can therefore be made by the logic. In case of a long **INP** pulse, the counter does not overflow but stays at the maximum value until cleared. **PCS.CS1** is cleared by setting bit **PCTRL.CLRP**.

The **INP** signal is not issued at the output stage.

Note: OSC2 is indirectly monitored by the Life Sign mechanism.

Timing Calibration Feature

The purpose of this supervision function is to measure the frequency of oscillator SSOC2. The PWM input signal is used to start and stop a counter clocked by SSOSC2. The function is activated when the device is in OPM6 (only). The counter is incremented for the duration of the High level at pin **INP**. At a High-to-Low transition at pin INP, the counter is stopped, and its content is transferred to bit field **SCS.CS2**. A plausibility check can therefore be made by the logic. In case of a long **INP** pulse, the counter does not overflow but stays at the maximum value until cleared. **SCS.CS2** is cleared by a reset event only.

The **INP** signal is not issued at the output stage.

4 Register Description

This chapter describes the internal registers of the device. [Table 4-1](#) provides an overview of the implemented registers. The abbreviations shown in [Table 4-2](#) are used in the whole section.

Table 4-1 Register Overview

| Register Short Name | Register Long Name | Offset Address | Wakeup Value | Reset Value |
|--|--|-----------------|--------------|-------------------|
| Register Description, Primary Register Description | | | | |
| PID | Primary ID Register | 00 _H | n.a. | xxxx _H |
| PSTAT | Primary Status Register | 01 _H | n.a. | 087D _H |
| PSTAT2 | Primary Second Status Register | 02 _H | n.a. | 0010 _H |
| PER | Primary Error Register | 03 _H | n.a. | 1C00 _H |
| PCFG | Primary Configuration Register | 04 _H | n.a. | 0004 _H |
| PCTRL | Primary Control Register | 06 _H | n.a. | 0001 _H |
| PCTRL2 | Primary Second Control Register | 07 _H | n.a. | 003D _H |
| PSCR | Primary Supervision Function Control Register | 08 _H | n.a. | 0001 _H |
| PRW | Primary Read/Write Register | 09 _H | n.a. | 0001 _H |
| PPIN | Primary Pin Status Register | 0A _H | n.a. | xxxx _H |
| PCS | Primary Clock Supervision Register | 0B _H | n.a. | 0001 _H |
| Register Description, Secondary Registers Description | | | | |
| SID | Secondary ID Register | 10 _H | n.a. | xxxx _H |
| SSTAT | Secondary Status Register | 11 _H | n.a. | 0001 _H |
| SSTAT2 | Secondary Second Status Register | 12 _H | n.a. | xxxx _H |
| SER | Secondary Error Register | 13 _H | n.a. | 8011 _H |
| SCFG | Secondary Configuration Register | 14 _H | n.a. | 0190 _H |
| SCTRL | Secondary Control Register | 16 _H | n.a. | 00F1 _H |
| SSCR | Secondary Supervision Function Control Register | 17 _H | n.a. | 0001 _H |
| SDESAT | Secondary DESAT Blanking Time Register | 18 _H | n.a. | 2000 _H |
| SOCP | Secondary OCP Blanking Time Register | 19 _H | n.a. | 0001 _H |
| SRTTOF | Secondary Regular TTOFF Configuration Register | 1A _H | n.a. | 0001 _H |
| SSTTOF | Secondary Safe TTOFF Configuration Register | 1B _H | n.a. | 2000 _H |
| SGM1 | Secondary First Gate Monitoring Register | 1C _H | n.a. | FF01 _H |
| SGM2 | Secondary Second Gate Monitoring Register | 1D _H | n.a. | FF01 _H |
| SACLT | Secondary Active Clamping Configuration Register | 1E _H | n.a. | 2600 _H |
| SCS | Secondary Clock Supervision Register | 1F _H | n.a. | 0001 _H |

The registers are addressed wordwise.

Table 4-2 Bit Access Terminology

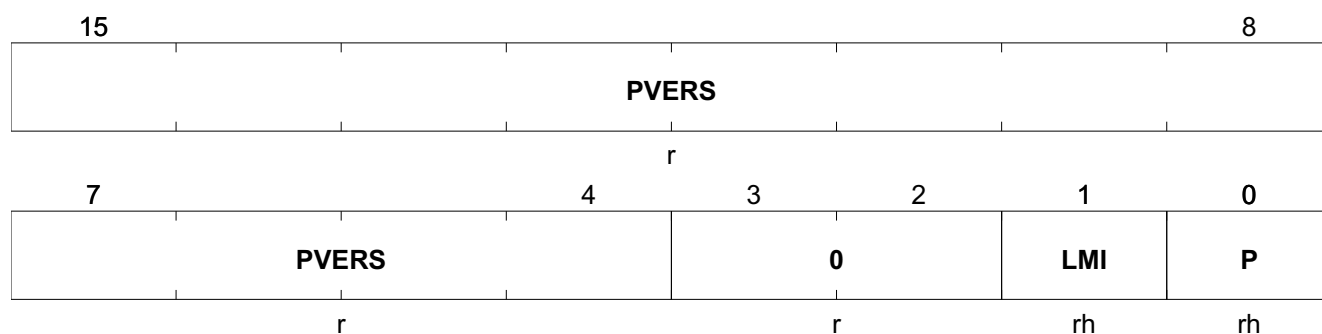
| Mode | Symbol | Description |
|------------------------------|--------|--|
| Basic Access Types | | |
| read/write | rw | This bit or bit field can be written or read. |
| read | r | This bit or bit field is read only. |
| write | w | This bit or bit field is write only (read as 0 _H). |
| read/write hardware affected | rwh | As rw, but bit or bit field can also be modified by hardware. |
| read hardware affected | rh | As r, but bit or bit field can also be modified by hardware. |
| sticky | s | Bits with this attribute are “sticky” in one direction. If their reset value is once overwritten they can be switched again into their reset state only by a reset operation. Software and internal logic (except reset-like functions) cannot switch this type of bit into its reset state by writing directly the register. The sticky attribute can be combined to other functions (e.g. ‘rh’). |
| Reserved / not implemented | 0 | Bit fields named ‘0’ indicate not implemented functions. They have the following behavior: <ul style="list-style-type: none"> • Reading these bit fields returns 0_H. • Writing these bit fields has no effect. These bit fields are reserved. When writing, software should always set such bit fields to 0 _H in order to preserve compatibility with future products. |
| Reserved / not defined | Res | Certain bit fields or bit combinations in a bit field can be marked as ‘Reserved’, indicating that the behavior of the device is undefined for that combination of bits. Setting the register to such an undefined value may lead to unpredictable results. When writing, software must always set such bit fields to legal values. |

4.1 Primary Register Description

Primary ID Register

This register contains the identification number of the primary chip version.

| PID | Offset | Wakeup Value | Reset Value |
|---------------------|-----------------|--------------|-------------------|
| Primary ID Register | 00 _H | n.a. | xxxx _H |



| Field | Bits | Type | Description |
|-------|------|------|--|
| PVERS | 15:4 | r | Primary Chip Identification This bit field defines the version of the primary chip. This bit field is hard-wired: 4A3 _H : AD Step. |
| 0 | 3:2 | r | Reserved Read as 0 _B . |
| LMI | 1 | rh | Last Message Invalid Notification This bit indicates if the last received SPI Message was correctly processed by the device. 0 _B : Previous Message was processed correctly. 1 _B : Previous Message was discarded. |
| P | 0 | rh | Parity Bit Odd Parity Bit. |

Primary Status Register

This register contains information on the status of the device.

| PSTAT Primary Status Register | | | | Offset 01 _H | Wakeup Value n.a. | Reset Value 087D _H |
|----------------------------------|------|-------|----|---------------------------|----------------------|----------------------------------|
| 15 | 12 | 11 | 10 | 9 | 8 | |
| 0 | | | | ERR | 0 | GPONS |
| r | | | | rh | r | rh |
| 7 | 6 | 5 | 2 | 1 | 0 | |
| ACT | SRDY | GPOFS | | LMI | P | |
| rh | rh | rh | | rh | rh | rh |

| Field | Bits | Type | Description |
|-------|-------|------|--|
| 0 | 15:12 | r | Reserved Read as 0 _B . |
| ERR | 11 | rh | Error Status This bit is the OR combination of all bits of register PER . 0 _B : No error is detected. 1 _B : An error is detected. |
| 0 | 10 | r | Reserved Read as 0 _B . |
| GPONS | 9:8 | rh | Gate Turn-On Plateau Level Configuration Status This bit field indicates the latest turn-on plateau level configuration request (WTO) received by the primary side via the SPI interface. Coding is identical to bit field PCTRL.GPON . |
| ACT | 7 | rh | Active State Status This bit indicates if the device is in Active State (OPM4). 0 _B : The device is not in Active State. 1 _B : The device is in Active State. |
| SRDY | 6 | rh | Secondary Ready Status This bit indicates if the secondary chip is ready for operation. 0 _B : Secondary chip is not ready. 1 _B : Secondary chip is ready. |
| GPOFS | 5:2 | rh | Gate Turn-Off Plateau Level Configuration Status (regular turn-off) This bit field indicates the latest turn-off plateau level configuration request (regular TTOFF) received by the primary side via the SPI interface. Coding is identical to bit field PCTRL2.GPOF . |

Register Description

| Field | Bits | Type | Description |
|-------|------|------|--|
| LMI | 1 | rh | Last Message Invalid Notification This bit indicates if the last received SPI Message was correctly processed by the device. 0 _B : Previous Message was processed correctly. 1 _B : Previous Message was discarded. |
| P | 0 | rh | Parity Bit Odd Parity Bit. |

Register Description

Primary Second Status Register

This register contains information on the status of the device.

PSTAT2

Primary Second Status Register

Offset
02_H

Wakeup Value
n.a.

Reset Value
0010_H

| | | | | | |
|-----|------|------|-------|-----|----|
| 15 | 12 | 11 | 10 | 9 | 8 |
| 0 | OSTC | STP | OT | HZ | |
| r | rh | rh | rh | rh | rh |
| 7 | 5 | 4 | 3 | 2 | 1 |
| OPM | FLTB | FLTA | ENVAL | LMI | P |
| rh | rhs | rhs | rh | rh | rh |

| Field | Bits | Type | Description |
|-------|-------|------|---|
| 0 | 15:12 | r | Reserved Read as 0 _B . |
| OSTC | 11 | rh | Output Stage Tristate Control This bit is set in case an OSM event. <i>Note: This bit is a mirror of bit SCTRL.OSTC</i> |
| STP | 10 | rh | Shoot Through Protection Status This bit is set in case the shoot through protection inhibition time (i.e. would inhibit a PWM rising edge). 0 _B : STP inhibition is not active. 1 _B : STP inhibition is active. |
| OT | 9 | rh | Over Temperature Status This bit is set in case an overtemperature condition is detected. 0 _B : The device is in normal operation. 1 _B : The device is in overtemperature condition. <i>Note: This bit is a mirror of bit SSTAT.OT</i> |
| HZ | 8 | rh | Tristate Output Stage Status This bit is set in case the output stage is in tristate. 0 _B : The output stage is in normal operation. 1 _B : The output stage is tristated. <i>Note: This bit is a mirror of bit SSTAT.HZ</i> |

Register Description

| Field | Bits | Type | Description |
|-------|------|------|---|
| OPM | 7:5 | rh | Operating Mode This bit field indicates which operating mode is active. 000 _B : Mode OPM0 is active. 001 _B : Mode OPM1 is active. 010 _B : Mode OPM2 is active. 011 _B : Mode OPM3 is active. 100 _B : Mode OPM4 is active. 101 _B : Mode OPM5 is active. 110 _B : Mode OPM6 is active. 111 _B : Reserved. <i>Note: This bit field is a mirror of bit field SSTAT.OPM</i> |
| FLTB | 4 | rhs | NFLTB Driver Request This bit indicates what output state is driven by the device at pin NFLTB . 0 _B : NFLTB is tristated. 1 _B : A Low Level is issued at NFLTB . This bit is sticky. |
| FLTA | 3 | rhs | NFLTA Driver Request This bit indicates what output state is driven by the device at pin NFLTA . 0 _B : NFLTA is tristated. 1 _B : A Low Level issued at NFLTA . This bit is sticky. |
| ENVAL | 2 | rh | EN Valid Status This bit indicates if the signal received on pin EN is valid. 0 _B : A non-valid signal is detected. 1 _B : A valid signal is detected. |
| LMI | 1 | rh | Last Message Invalid Notification This bit indicates if the last received SPI Message was correctly processed by the device. 0 _B : Previous Message was processed correctly. 1 _B : Previous Message was discarded. |
| P | 0 | rh | Parity Bit Odd Parity Bit. |

Primary Error Register

This register provides information on the error status of the device.

| PER Primary Error Register | | | | Offset 03 _H | Wakeup Value n.a. | Reset Value 1C00 _H | |
|-------------------------------|-----|---------|------|---------------------------|----------------------|----------------------------------|----|
| 15 | 13 | 12 | 11 | 10 | 9 | 8 | |
| 0 | | RSTE1 | RST1 | ENER | STPER | SPIER | |
| r | | rhs | rhs | rhs | rhs | rhs | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| VMTO | GER | OVLO3ER | OTER | OSTER | CER1 | LMI | P |
| rh | rh | rh | rh | rh | rhs | rh | rh |

| Field | Bits | Type | Description |
|-------|-------|------|---|
| 0 | 15:13 | r | Reserved Read as 0 _B . |
| RSTE1 | 12 | rhs | External Hard Reset Primary Flag This bit indicates if a reset event has been detected on the primary chip due to the activation of pin NRST/RDY . 0 _B : No external hard reset event has been detected. 1 _B : An externally hard reset event has been detected. This bit is sticky. |
| RST1 | 11 | rhs | Reset Primary Flag This bit indicates if a reset event has been detected on the primary chip. 0 _B : No reset event has been detected. 1 _B : A reset event has been detected. This bit is sticky. |
| ENER | 10 | rhs | EN Signal Invalid Flag This bit indicates if an invalid-to-valid transition on signal EN has been detected. 0 _B : No event has been detected. 1 _B : An event has been detected. This bit is sticky. <i>Note: This bit can not be cleared while an error condition is active (bit PSTAT2.ENVAL cleared).</i> |

Register Description

| Field | Bits | Type | Description |
|---------|------|------|--|
| STPER | 9 | rhs | Shoot Through Protection Error Flag This bit indicates if a shoot through protection error event has been detected. 0 _B : No event has been detected. 1 _B : An event has been detected. This bit is sticky. <i>Note: This bit can not be cleared while an error condition is active (bit PSTAT2.STP set).</i> |
| SPIER | 8 | rhs | SPI Error Flag This indicates if an SPI error event has been detected. 0 _B : No error event has been detected. 1 _B : An error event has been detected. This bit is sticky. |
| VMTO | 7 | rh | Verif. Mode Time-Out Flag This bit indicates if a verification mode time-out event has been detected. 0 _B : No time-out event has been detected. 1 _B : A time-out event has been detected. <i>Note: This bit is a mirror of bit SER.VMTO.</i> |
| GER | 6 | rh | GATE Monitoring Error Flag This bit indicates if a GATE monitoring timer overflow occurred during a switching sequence. 0 _B : No error event has been detected. 1 _B : An error event has been detected. <i>Note: This bit is a mirror of bit SER.GER.</i> |
| OVLO3ER | 5 | rh | OVLO3 Error Flag This bit indicates if an Overvoltage Lockout event on V _{EE2} has been detected. 0 _B : No error event has been detected. 1 _B : An error event has been detected. <i>Note: This bit is a mirror of bit SER.OVLO3ER.</i> |
| OTER | 4 | rh | Overtemperature Error Flag This bit indicates if an overtemperature condition has been detected. 0 _B : No event has been detected. 1 _B : An event has been detected. <i>Note: This bit is a mirror of bit SER.OTER.</i> |
| OSTER | 3 | rh | Output Stage Tristate Event Flag This bit indicates if the output stage has been tristated. 0 _B : No tristate event has been detected. 1 _B : A tristate event has been detected. <i>Note: This bit is a mirror of bit SER.OSTER.</i> |

Register Description

| Field | Bits | Type | Description |
|-------|------|------|---|
| CER1 | 2 | rhs | Communication Error Primary Flag This indicates if a loss of communication event ¹⁾ with the secondary chip has been detected by the primary chip. 0 _B : No event has been detected. 1 _B : An event has been detected. This bit is sticky. <i>Note: This bit can not be cleared while an error condition is active (bit PSTAT2.SRDY cleared).</i> |
| LMI | 1 | rh | Last Message Invalid Notification This bit indicates if the last received SPI Message was correctly processed by the device. 0 _B : Previous Message was processed correctly. 1 _B : Previous Message was discarded. |
| P | 0 | rh | Parity Bit Odd Parity Bit. |

1) This bit is not set after a reset event

Primary Configuration Register

This register is used to select the configuration of the device.

| PCFG | Offset | Wakeup Value | Reset Value |
|--------------------------------|-----------------|--------------|-------------------|
| Primary Configuration Register | 04 _H | n.a. | 0004 _H |

| | | | | | | | | |
|----|--------|--------|-----|-------|-----|----|---|---|
| 15 | | | | | | | | 8 |
| 0 | | | | | | | | |
| r | | | | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | |
| 0 | OSMAEN | OSTAEN | Res | PAREN | LMI | P | | |
| r | rw | rw | rw | rw | rh | rh | | |

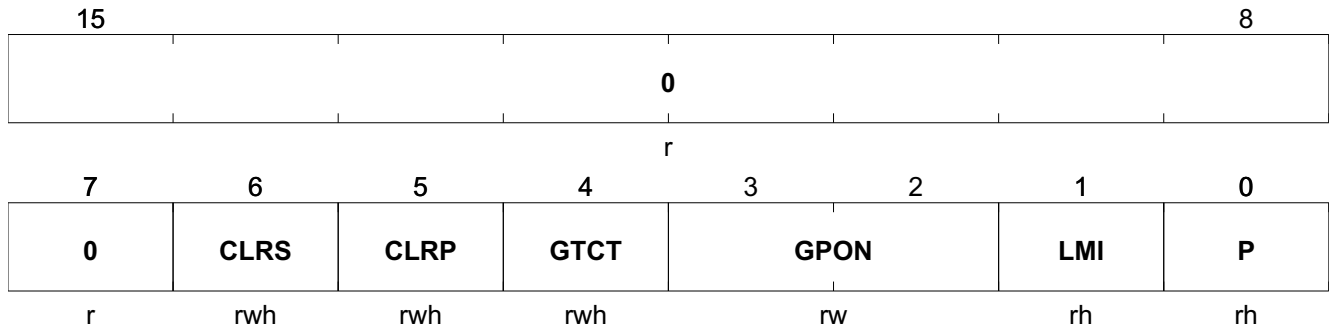
| Field | Bits | Type | Description |
|--------|------|------|---|
| 0 | 15:6 | r | Reserved Read as 0 _B . |
| OSMAEN | 5 | rw | NFLTA Activation on OSM Event Enable Bit This bit enables the activation of signal NFLTA in case of a transition from 0 _B to 1 _B of bit PSTAT2.OSTC . 0 _B : NFLTA activation is disabled. 1 _B : NFLTA activation is enabled |
| OSTAEN | 4 | rw | NFLTA Activation on Tristate Event Enable Bit This bit enables the activation of signal NFLTA in case of a transition from 0 _B to 1 _B of bit PER.OSTER . 0 _B : NFLTA activation is disabled. 1 _B : NFLTA activation is enabled |
| Res | 3 | rw | Reserved This bit is reserved. It should be written with 0 _H . |
| PAREN | 2 | rw | Parity Enable Bit This bit indicates if the SPI parity error detection is active (reception only). 0 _B : Parity Check is disabled. 1 _B : Parity Check is enabled. |
| LMI | 1 | rh | Last Message Invalid Notification This bit indicates if the last received SPI Message was correctly processed by the device. 0 _B : Previous Message was processed correctly. 1 _B : Previous Message was discarded. |
| P | 0 | rh | Parity Bit Odd Parity Bit. |

Register Description

Primary Control Register

This register is used to control the device during run-time.

| PCTRL | Offset | Wakeup Value | Reset Value |
|--------------------------|-----------------|--------------|-------------------|
| Primary Control Register | 06 _H | n.a. | 0001 _H |



| Field | Bits | Type | Description |
|-------|------|------|--|
| 0 | 15:7 | r | Reserved Read as 0 _B . |
| CLRS | 6 | rwh | Clear Secondary Request Bit This bit is used to clear the sticky bits on the secondary side. 0 _B : No action. 1 _B : Clear sticky bits. This bit is automatically cleared by hardware. |
| CLRP | 5 | rwh | Clear Primary Request Bit This bit is used to clear the sticky bits on the primary side. 0 _B : No action. 1 _B : Clear sticky bits and deassert signals NFLTA and NFLTb . This bit is automatically cleared by hardware. |
| GTCT | 4 | rwh | Gate Timing Capture Trigger Bit This bit is used to trigger the timing capture mechanism measurements of the Gate Monitoring function. 0 _B : No action. 1 _B : Timing capture triggered. This bit is automatically cleared by hardware |
| GPON | 3:2 | rw | Gate Turn-On Plateau Level Configuration This bit field is used to configure the voltage of the plateau during Weak Turn-On. 0 _H : V _{GPON0} selected. 1 _H : V _{GPON1} selected. 2 _H : V _{GPON2} selected. 3 _H : Reserved (WTO) . |

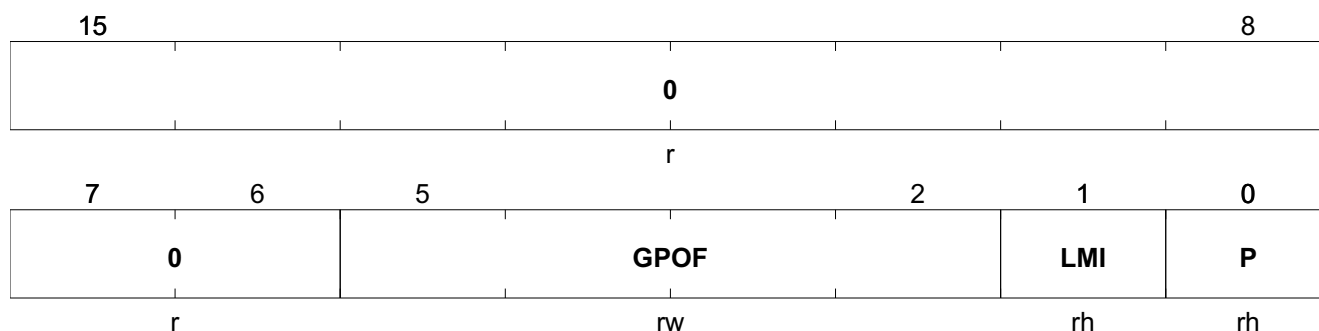
Register Description

| Field | Bits | Type | Description |
|-------|------|------|--|
| LMI | 1 | rh | Last Message Invalid Notification This bit indicates if the last received SPI Message was correctly processed by the device. 0 _B : Previous Message was processed correctly. 1 _B : Previous Message was discarded. |
| P | 0 | rh | Parity Bit Odd Parity Bit. |

Primary Second Control Register

This register is used to control the device during run-time.

| | | | |
|--|-----------------------|---------------------|-------------------------|
| PCTRL2 | Offset | Wakeup Value | Reset Value |
| Primary Second Control Register | 07_H | n.a. | 003D_H |

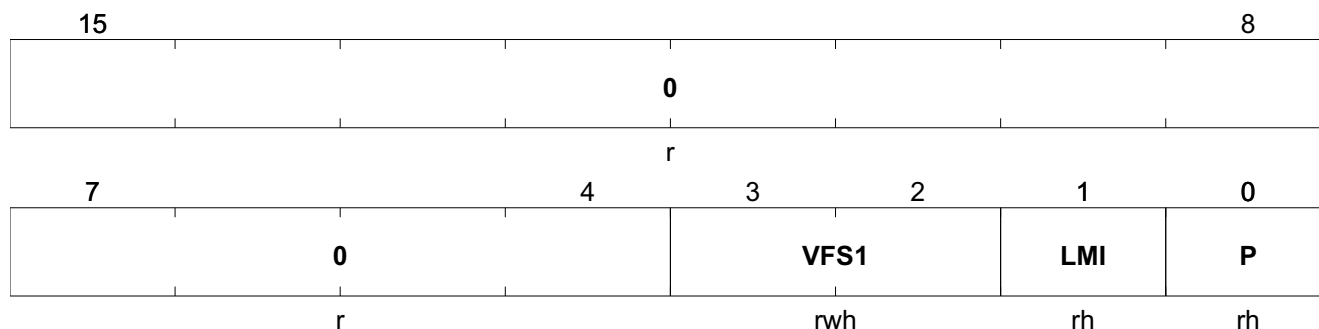


| Field | Bits | Type | Description |
|-------|------|------|--|
| 0 | 15:6 | r | Reserved Read as 0 _B . |
| GPOF | 5:2 | rw | Gate Turn-Off Plateau Level Configuration (regular turn-off) This bit field is used to configure the Two-Level Turn-Off plateau voltage (regular turn-off). 0000 _B : V _{GPOF0} selected. 0001 _B : V _{GPOF1} selected. ... 1110 _B : V _{GPOF14} selected. 1111 _B : V _{GPOF15} selected. |
| LMI | 1 | rh | Last Message Invalid Notification This bit indicates if the last received SPI Message was correctly processed by the device. 0 _B : Previous Message was processed correctly. 1 _B : Previous Message was discarded. |
| P | 0 | rh | Parity Bit Odd Parity Bit. |

Primary Supervision Function Control Register

This register is used to trigger the verification functions on the primary side.

| | | | |
|--|-----------------------|---------------------|-------------------------|
| PSCR | Offset | Wakeup Value | Reset Value |
| Primary Supervision Function Control Register | 08_H | n.a. | 0001_H |

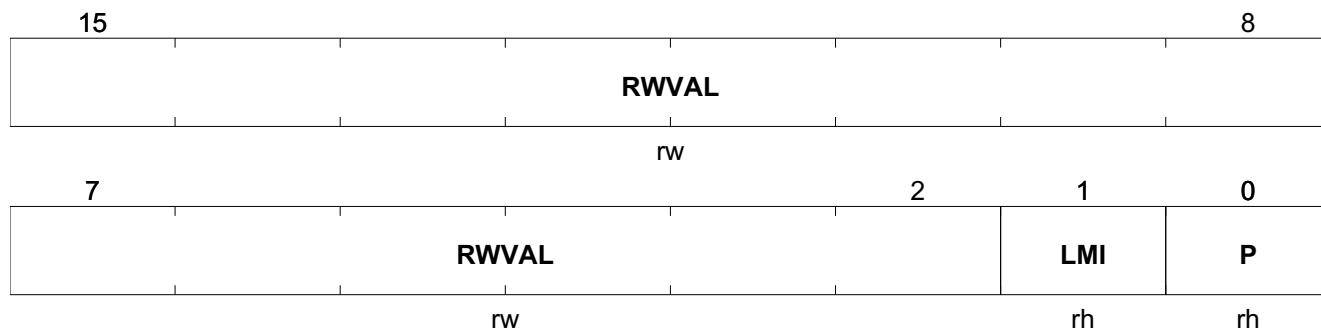


| Field | Bits | Type | Description |
|-------|------|------|---|
| 0 | 15:4 | r | Reserved Read as 0 _B . |
| VFS1 | 3:2 | rwh | Primary Verification Function Selection This bit field is used to activate the primary verification functions. 00 _B : No function activated. 01 _B : Reserved. 10 _B : Primary Clock Supervision active. 11 _B : Reserved. <i>Note: The selection defined by this bit field is only effective when the device enters Mode OPM5. This bit field is automatically cleared when entering OPM1.</i> |
| LMI | 1 | rh | Last Message Invalid Notification This bit indicates if the last received SPI Message was correctly processed by the device. 0 _B : Previous Message was processed correctly. 1 _B : Previous Message was discarded. |
| P | 0 | rh | Parity Bit Odd Parity Bit. |

Register Description
Primary Read/Write Register

This register provides a readable and writable address space for data integrity test during runtime. This register is not associated with any hardware functionality.

| PRW | Offset | Wakeup Value | Reset Value |
|-----------------------------|-----------------|--------------|-------------------|
| Primary Read/Write Register | 09 _H | n.a. | 0001 _H |



| Field | Bits | Type | Description |
|-------|------|------|--|
| RWVAL | 15:2 | rw | Read/Write value This bit field is "don't care" for the device. |
| LMI | 1 | rh | Last Message Invalid Flag This bit indicates if the last received SPI Message was correctly processed by the device. 0 _B : Previous Message processed correctly. 1 _B : Previous Message not processed. |
| P | 0 | rh | Parity Bit Odd Parity Bit. |

Primary Pin Status Register

This register provides status information on the I/Os of the primary chip.

| PPIN | Offset | Wakeup Value | Reset Value |
|--|-----------------|--------------|-------------------|
| Primary Pin Status Register | 0A _H | n.a. | xxxx _H |
| <div> <div>15</div> <div>9</div> <div>8</div> <div>0</div> <div>Res</div> </div> | | | |
| <div> <div>7</div> <div>6</div> <div>5</div> <div>4</div> <div>3</div> <div>2</div> <div>1</div> <div>0</div> <div>Res</div> <div>NFLTBL</div> <div>NFLTAL</div> <div>ENL</div> <div>INSTPL</div> <div>INPL</div> <div>LMI</div> <div>P</div> </div> | | | |
| <div> <div>rh</div> <div>rh</div> <div>rh</div> <div>rh</div> <div>rh</div> <div>rh</div> <div>rh</div> <div>rh</div> </div> | | | |

| Field | Bits | Type | Description |
|--------|------|------|--|
| 0 | 15:9 | r | Reserved Read as 0 _B . |
| Res | 8:7 | rh | Reserved This bit field is reserved. |
| NFLTBL | 6 | rh | Pin NFLTB Level This bit indicates the logical level read on pin NFLTB . 0 _B : Low-level is detected. 1 _B : High-level is detected. |
| NFLTAL | 5 | rh | Pin NFLTA Level This bit indicates the logical level read on pin NFLTA . 0 _B : Low-level is detected. 1 _B : High-level is detected. |
| ENL | 4 | rh | Pin EN Level This bit indicates the logical level read on pin EN . 0 _B : Low-level is detected. 1 _B : High-level is detected. |
| INSTPL | 3 | rh | Pin INSTP Level This bit indicates the logical level read on pin INSTP . 0 _B : Low-level is detected. 1 _B : High-level is detected. |
| INPL | 2 | rh | Pin INP Level This bit indicates the logical level read on pin INP . 0 _B : Low-level is detected. 1 _B : High-level is detected. |
| LMI | 1 | rh | Last Message Invalid Notification This bit indicates if the last received SPI Message was correctly processed by the device. 0 _B : Previous Message was processed correctly. 1 _B : Previous Message was discarded. |

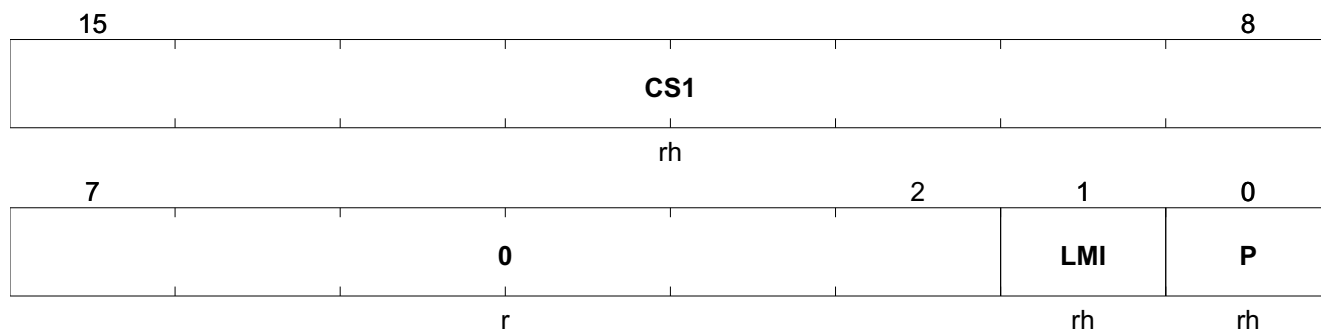
Register Description

| Field | Bits | Type | Description |
|--------------|-------------|-------------|--------------------------------------|
| P | 0 | rh | Parity Bit Odd Parity Bit. |

Primary Clock Supervision Register

This register shows the result of the Primary Clock Supervision function.

| PCS | Offset | Wakeup Value | Reset Value |
|------------------------------------|-----------------|--------------|-------------------|
| Primary Clock Supervision Register | 0B _H | n.a. | 0001 _H |



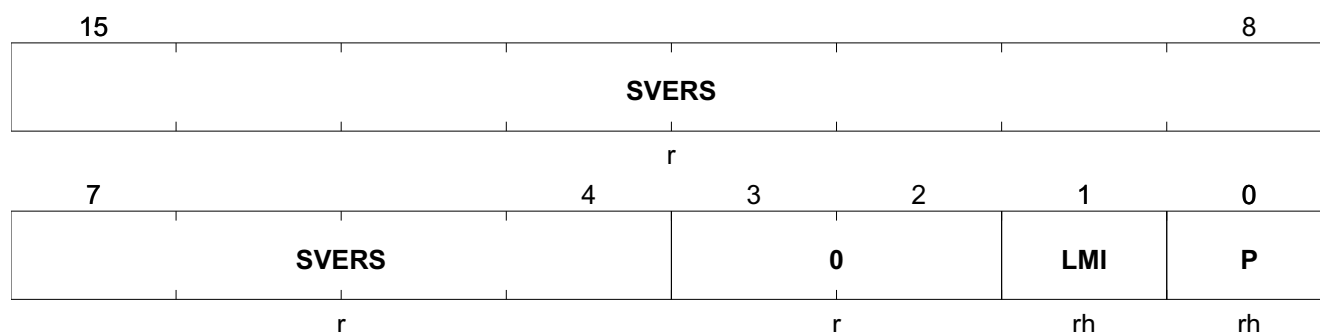
| Field | Bits | Type | Description |
|-------|------|------|--|
| CS1 | 15:8 | rh | Primary Clock Supervision This bit field is written by hardware by the Primary Clock Supervision function and gives the number of measured OSC1 clock cycles. <i>Note: This bit field can be cleared by setting bit PCTRL.CLRP.</i> |
| 0 | 7:2 | r | Reserved Read as 0 _B . |
| LMI | 1 | rh | Last Message Invalid Notification This bit indicates if the last received SPI Message was correctly processed by the device. 0 _B : Previous Message was processed correctly. 1 _B : Previous Message was discarded. |
| P | 0 | rh | Parity Bit Odd Parity Bit. |

4.2 Secondary Registers Description

Secondary ID Register

This register contains the identification number of secondary chip version.

| SID | Offset | Wakeup Value | Reset Value |
|-----------------------|-----------------|--------------|-------------------|
| Secondary ID Register | 10 _H | n.a. | xxxx _H |



| Field | Bits | Type | Description |
|-------|------|------|--|
| SVERS | 15:4 | r | Secondary Chip Identification This bit field defines the version of the secondary chip. This bit field is hard-wired: 8B2 _H : AD Step. |
| 0 | 3:2 | r | Reserved Read as 0 _B . |
| LMI | 1 | rh | Last Message Invalid Notification This bit indicates if the last received SPI Message was correctly processed by the device. 0 _B : Previous Message was processed correctly. 1 _B : Previous Message was discarded. |
| P | 0 | rh | Parity Bit Odd Parity Bit. |

Secondary Status Register

This register contains information on the status of the device.

SSTAT
Secondary Status Register
Offset
11_H
Wakeup Value
n.a.
Reset Value
0001_H

| | | | | | | | |
|-----|------|------|-------|-----|-----|----|---|
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| Res | OT | HZ | OCPCD | DBG | OPM | | |
| | rh | rh | rhs | rh | rh | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| OPM | FLTB | FLTA | PWM | 0 | LMI | P | |
| rh | rh | rh | rh | r | rh | rh | |

| Field | Bits | Type | Description |
|-------|-------|------|---|
| Res | 15:14 | rh | Reserved This bit field is reserved. |
| OT | 13 | rh | Overttemperature Status This bit indicates if an overtemperature condition is detected. 0 _B : No overtemperature condition is detected. 1 _B : Overttemperature condition is detected. |
| HZ | 12 | rh | Output Stage Status This bit indicates the state of the output stage. 0 _B : The output stage is operating normally. 1 _B : The output stage is tristated. |
| OCPCD | 11 | rhs | OCPCD Current Detection Flag This bit indicates if the voltage at pin OCPCD has been above the internal threshold V _{OCPCD2} . 0 _B : OCPCD voltage has not been above internal threshold. 1 _B : OCPCD voltage has been above internal threshold. This bit is sticky. |
| DBG | 10 | rh | Debug Mode Active Bit This bit indicates if the Debug Mode is active. 0 _B : Debug Mode is not active. 1 _B : Debug Mode is active. |
| OPM | 9:7 | rh | Operating Mode This bit field indicates in which operating mode is active. The coding is identical to PSTAT2 . |
| FLTB | 6 | rh | Event Class B Status This bit indicates if the conditions leading to an Event Class B are detected. 0 _B : Event conditions are not met. 1 _B : Event conditions are met. |

Register Description

| Field | Bits | Type | Description |
|-------|------|------|--|
| FLTA | 5 | rh | Event Class A Error This bit indicates if the conditions leading to an Event Class A are detected. 0 _B : Event conditions are not met. 1 _B : Event conditions are met. |
| PWM | 4 | rh | PWM Command Status This bit indicates the status of the PWM command received from the primary side. 0 _B : PWM OFF command is detected. 1 _B : PWM ON command is detected. |
| 0 | 3:2 | r | Reserved Read as 0 _B . |
| LMI | 1 | rh | Last Message Invalid Notification This bit indicates if the last received SPI Message was correctly processed by the device. 0 _B : Previous Message was processed correctly. 1 _B : Previous Message was discarded. |
| P | 0 | rh | Parity Bit Odd Parity Bit. |

Register Description

Secondary Second Status Register

This register contains information on the status of the device.

SSTAT2

Secondary Second Status Register

Offset
12_H

Wakeup Value
n.a.

Reset Value
xxxx_H

| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|-------|--------|------|-------|--------|--------|--------|--------|
| Res | DACLPL | GC2 | GC1 | OVLO3M | UVLO3M | OVLO2M | UVLO2M |
| rh | rh | rh | rh | rh | rh | rh | rh |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| OCPC2 | OCPC1 | OSDL | DSATC | 0 | | LMI | P |
| rh | rh | rh | rh | r | | rh | rh |

| Field | Bits | Type | Description |
|--------|------|------|---|
| Res | 15 | rh | Reserved This bit is reserved. |
| DACLPL | 14 | rh | DACLPL Level This bit indicates the level read at pin DACLPL . 0 _B : DACLPL level is Low. 1 _B : DACLPL level is High. |
| GC2 | 13 | rh | Gate Second Comparator Status This bit shows the output of the second comparator of the Gate Monitoring function. 0 _B : GATE voltage is below V _{GATE2} . 1 _B : GATE voltage is above V _{GATE2} . |
| GC1 | 12 | rh | Gate First Comparator Status This bit indicates the output of the first comparator of the Gate Monitoring function. 0 _B : GATE voltage is below V _{GATE1} . 1 _B : GATE voltage is above V _{GATE1} . |
| OVLO3M | 11 | rh | OVLO3 Comparator Status This bit indicates the result of the OVLO3 monitoring function. 0 _B : No failure condition is detected. 1 _B : A failure condition is detected. |
| UVLO3M | 10 | rh | UVLO3 Monitoring Result This bit indicates the result of the UVLO3 monitoring function. 0 _B : No failure condition is detected. 1 _B : A failure condition is detected. |

Register Description

| Field | Bits | Type | Description |
|--------|------|------|--|
| OVLO2M | 9 | rh | OVLO2 Monitoring Result This bit indicates the result of the OVLO2 monitoring function. 0_B : No failure condition is detected. 1_B : A failure condition is detected. |
| UVLO2M | 8 | rh | UVLO2 Monitoring Result This bit indicates the result of the UVLO2 monitoring function. 0_B : No failure condition is detected. 1_B : One failure condition is detected. |
| OCPC2 | 7 | rh | OCP Second Comparator Result This bit indicates the (blanked) output of the second comparator of the OCP function. 0_B : OC P voltage is below V_{OCPD2} . 1_B : OC P voltage is above V_{OCPD2} . |
| OCPC1 | 6 | rh | OCP First Comparator Result This bit indicates the (blanked) output of the first comparator of the OCP function. 0_B : OC P voltage is below V_{OCPD1} . 1_B : OC P voltage is above V_{OCPD1} . |
| OSDL | 5 | rh | OSD Level This bit indicates the level read at pin OSD . 0_B : OSD level is Low. 1_B : OSD level is High. |
| DSATC | 4 | rh | DESAT Comparator Result This bit indicates the output of the comparator of the DESAT function. 0_B : DESAT voltage is below V_{DESAT} . 1_B : DESAT voltage is above V_{DESAT} . |
| 0 | 3:2 | r | Reserved Read as 0_B . |
| LMI | 1 | rh | Last Message Invalid Notification This bit indicates if the last received SPI Message was correctly processed by the device. 0_B : Previous Message was processed correctly. 1_B : Previous Message was discarded. |
| P | 0 | rh | Parity Bit Odd Parity Bit. |

Register Description

Secondary Error Register

This register provides information on the error status of the device.

| SER Secondary Error Register | | | | Offset 13 _H | Wakeup Value n.a. | Reset Value 8011 _H | |
|---------------------------------|-------|---------|---------|---------------------------|----------------------|----------------------------------|-----|
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| RST2 | OCPER | DESATER | UVLO2ER | OVLO2ER | UVLO3ER | VMTO | GER |
| rhs | rhs | rhs | rhs | rhs | rhs | rhs | rhs |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| OVLO3ER | OTER | OSTER | CER2 | 0 | | LMI | P |
| rhs | rhs | rhs | rhs | r | | rh | rh |

| Field | Bits | Type | Description |
|---------|------|------|--|
| RST2 | 15 | rhs | Hard Reset Secondary Flag This bit indicates if a hard reset event has been detected on the secondary chip (due to a V_{CC2} power-up). 0 _B : No hard reset event has been detected. 1 _B : A hard reset event has been detected. This bit is sticky. |
| OCPER | 14 | rhs | OCP Error Flag This bit indicates if an OCP event has been detected. 0 _B : No event has been detected. 1 _B : An event has been detected. This bit is sticky. <i>Note: This bit can not be cleared while an error condition is active (bit SSTAT2.OCP1 set).</i> |
| DESATER | 13 | rhs | DESAT Error Flag This bit indicates if a DESAT event has been detected. 0 _B : No event has been detected. 1 _B : An event has been detected. This bit is sticky. |
| UVLO2ER | 12 | rhs | UVLO2 Error Flag This bit indicates if an Undervoltage Lockout event (on V_{CC2}) has been detected. 0 _B : No event has been detected. 1 _B : An event has been detected. This bit is sticky. <i>Note: This bit can not be cleared while an error condition is active (bit SSTAT2.UVLO2M set).</i> |

Register Description

| Field | Bits | Type | Description |
|---------|------|------|---|
| OVLO2ER | 11 | rhs | OVLO2 Error Flag This bit indicates if an Overvoltage Lockout event (on V_{CC2}) has been detected. 0_B : No event has been detected. 1_B : An event has been detected. This bit is sticky. <i>Note: This bit can not be cleared while an error condition is active (bit SSTAT2.OVLO2M set).</i> |
| UVLO3ER | 10 | rhs | UVLO3 Error Flag This bit indicates if an Undervoltage Lockout event (on V_{EE2}) has been detected. 0_B : No event has been detected. 1_B : An event has been detected. This bit is sticky. <i>Note: This bit can not be cleared while an error condition is active (bit SSTAT2.UVLO3M set).</i> |
| VMTO | 9 | rhs | Verif. Mode Time-Out Flag This bit indicates if time-out event in Verification Mode has been detected. 0_B : No event has been detected. 1_B : An event has been detected. This bit is sticky. |
| GER | 8 | rhs | Gate Monitoring Error Flag This bit indicates in a Gate Monitoring error event has been detected. 0_B : No event has been detected. 1_B : An event has been detected. This bit is sticky. |
| OVLO3ER | 7 | rhs | OVLO3 Error Flag This bit indicates if an Overvoltage Lockout event (on V_{EE2}) has been detected. 0_B : No event has been detected. 1_B : An event has been detected. This bit is sticky. <i>Note: This bit can not be cleared while an error condition is active (bit SSTAT2.OVLO3M set).</i> |
| OTER | 6 | rhs | Overtemperature Error Flag This bit indicates if an overtemperature event has been detected. 0_B : No event has been detected. 1_B : An event has been detected. This bit is sticky. <i>Note: This bit can not be cleared if bit SSTAT.OT is set.</i> |

Register Description

| Field | Bits | Type | Description |
|-------|------|------|--|
| OSTER | 5 | rhs | Output Stage Tristate Event Flag This bit indicates if an output stage tristate event has been detected. 0 _B : No event has been detected. 1 _B : An event has been detected. This bit is sticky. <i>Note: This bit can not be cleared if bit SSTAT.HZ is set.</i> |
| CER2 | 4 | rhs | Communication Error Secondary Flag This indicates if a loss of communication event with the primary chip has been detected by the secondary chip. 0 _B : No event has been detected. 1 _B : An event has been detected. This bit is sticky. |
| 0 | 3:2 | r | Reserved Read as 0 _B . |
| LMI | 1 | rh | Last Message Invalid Notification This bit indicates if the last received SPI Message was correctly processed by the device. 0 _B : Previous Message was processed correctly. 1 _B : Previous Message was discarded. |
| P | 0 | rh | Parity Bit Odd Parity Bit. |

Secondary Configuration Register

This register is used to select the configuration of the device.

| SCFG Secondary Configuration Register | | | | Offset 14 _H | Wakeup Value n.a. | Reset Value 0190 _H |
|--|------|-----|------|---------------------------|----------------------|----------------------------------|
| 15 | | 11 | | 10 | 9 | 8 |
| 0 | | | | TOSEN | PSEN | DSTCEN |
| r | | rw | | rw | rw | rw |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 |
| OSDAD | OSMD | Res | VBEC | 0 | LMI | P |
| rw | rw | rwh | rw | r | rh | rh |

| Field | Bits | Type | Description |
|--------|-------|------|---|
| 0 | 15:11 | r | Reserved Read as 0 _B . |
| TOSEN | 10 | rw | Verification Mode Time Out Duration Selection This bit selects the duration of the verification mode time out. 0 _B : Regular time-out value (typ. 15 ms). 1 _B : Slow time-out value (typ. 60 ms). |
| PSEN | 9 | rw | Pulse Suppressor Enable Bit This bit enables the internal pulse suppressor. 0 _B : Pulse suppressor is disabled. 1 _B : Pulse suppressor is enabled. |
| DSTCEN | 8 | rw | DESAT Clamping Enable Bit This bit enables the internal clamping (to GND2) of the DESAT pin during PWM OFF commands. 0 _B : DESAT clamping is disabled. 1 _B : DESAT clamping is enabled. |
| OSDAD | 7 | rw | OSD Event Class A Disable Bit This bit disables the generation of an Event Class A in case of an OSD pin Tristate event. 0 _B : Event Class A is enabled. 1 _B : Event Class A is disabled. |
| OSMD | 6 | rw | Output Stage Monitoring Disable Bit This bit disables the internal Output Stage Monitoring mechanism. 0 _B : OSM is working normally. 1 _B : OSM is disabled. |
| Res | 5 | rwh | Reserved This bit field is reserved. It should be written with 0 _H . |

Register Description

| Field | Bits | Type | Description |
|-------|------|------|--|
| VBEC | 4 | rw | V_{BE} Compensation This bit enables the V _{BE} compensation of the TTOFF and WTO plateau levels. 0 _B : V _{BE} Compensation disabled. 1 _B : V _{BE} Compensation enabled. |
| 0 | 3:2 | r | Reserved Read as 0 _B . |
| LMI | 1 | rh | Last Message Invalid Notification This bit indicates if the last received SPI Message was correctly processed by the device. 0 _B : Previous Message was processed correctly. 1 _B : Previous Message was discarded. |
| P | 0 | rh | Parity Bit Odd Parity Bit. |

Register Description

Secondary Control Register

This register is used to control the device during run-time.

SCTRL

Secondary Control Register

Offset
16_H

Wakeup Value
n.a.

Reset Value
00F1_H

| | | | | | | |
|----|-------|------|------|----|-------|----|
| 15 | 13 | 12 | 11 | 10 | 9 | 8 |
| 0 | | OSTC | CLRS | 0 | GPONS | |
| r | | rhs | rh | rh | | rh |
| 7 | | 4 | 3 | 2 | 1 | 0 |
| | GPOFS | | 0 | | LMI | P |
| | rh | | r | | rh | rh |

| Field | Bits | Type | Description |
|-------|-------|------|--|
| 0 | 15:13 | r | Reserved Read as 0 _B . |
| OSTC | 12 | rhs | Output Stage Tristate Control This bit is used by the hardware to control the state of the output stage. This bit is set in case of an OSM event. It is cleared by either a falling edge on pin OSD or when bit PCTRL.CLRS is set. |
| CLRS | 11 | rh | Clear Secondary Request Bit This bit is set by writing PCTRL.CLRS . |
| 0 | 10 | rh | Reserved Read as 0 _B . |
| GPONS | 9:8 | rh | Gate Turn-On Plateau Level Configuration This bit field indicates the current configuration of the plateau level for WTO. Coding is identical to PCTRL.GPON . <i>Note: This bit field is a mirror of PSTAT.GPONS.</i> |
| GPOFS | 7:4 | rh | Gate Turn-Off Plateau Level Configuration (regular turn-off) This bit field indicates the current configuration of the TTOFF plateau level (for regular turn-off). Coding is identical to PCTRL2.GPOF . <i>Note: This bit field is a mirror of PSTAT.GPOFS.</i> |
| 0 | 3:2 | r | Reserved Read as 0 _B . |
| LMI | 1 | rh | Last Message Invalid Notification This bit indicates if the last received SPI Message was correctly processed by the device. 0 _B : Previous Message was processed correctly. 1 _B : Previous Message was discarded. |

Register Description

| Field | Bits | Type | Description |
|-------|------|------|--------------------------------------|
| P | 0 | rh | Parity Bit Odd Parity Bit. |

Register Description

Secondary Supervision Function Control Register

This register is used to trigger the verification functions on the secondary side.

| SSCR | Offset | Wakeup Value | Reset Value |
|---|-----------------|--------------|-------------------|
| Secondary Supervision Function Control Register | 17 _H | n.a. | 0001 _H |

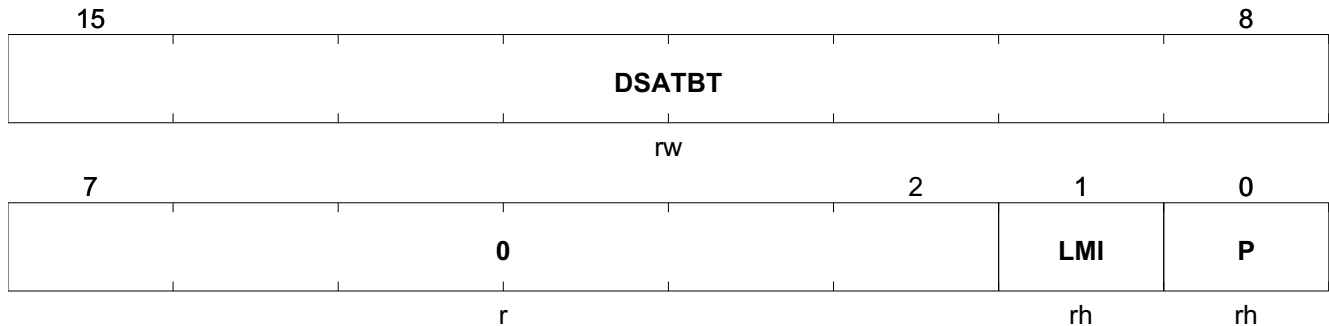
| | | | | | | | | | | | | | | | | | | | |
|------|--|--|--|--|--|--|--|--|--|---|--|-----|--|----|--|--|--|--|---|
| 15 | | | | | | | | | | | | | | | | | | | 8 |
| 0 | | | | | | | | | | | | | | | | | | | |
| r | | | | | | | | | | | | | | | | | | | |
| 7 | | | | | | | | | | | | | | | | | | | 0 |
| VFS2 | | | | | | | | | | 0 | | LMI | | P | | | | | |
| rwh | | | | | | | | | | r | | rh | | rh | | | | | |

| Field | Bits | Type | Description |
|-------|------|------|--|
| 0 | 15:8 | r | Reserved Read as 0 _B . |
| VFS2 | 7:4 | rwh | Secondary Verification Function Selection This bit field is used to activate the secondary verification function. 0000 _B : No function activated. 0001 _B : DESAT Supervision Level 1 active. 0010 _B : DESAT Supervision Level 2 active. 0011 _B : OCP Supervision Level 1 active. 0100 _B : UVLO2 Supervision active. 0101 _B : OVLO2 Supervision active. 0110 _B : UVLO3 Supervision active. 0111 _B : OVLO3 Supervision active. 1000 _B : TCF function active. 1001 _B : DESAT Supervision Level 3 active. 1010 _B : OCP Supervision Level 3 active. All other bit combinations are reserved. <i>Note: The selection defined by this bit field is only effective when the device enters Mode OPM5. This bit field is automatically cleared when entering OPM1.</i> |
| 0 | 3:2 | r | Reserved Read as 0 _B . |
| LMI | 1 | rh | Last Message Invalid Notification This bit indicates if the last received SPI Message was correctly processed by the device. 0 _B : Previous Message was processed correctly. 1 _B : Previous Message was discarded. |
| P | 0 | rh | Parity Bit Odd Parity Bit. |

Secondary DESAT Blanking Time Register

This register configures the blanking time of the DESAT function.

| SDESAT | Offset | Wakeup Value | Reset Value |
|--|-----------------|--------------|-------------------|
| Secondary DESAT Blanking Time Register | 18 _H | n.a. | 2000 _H |

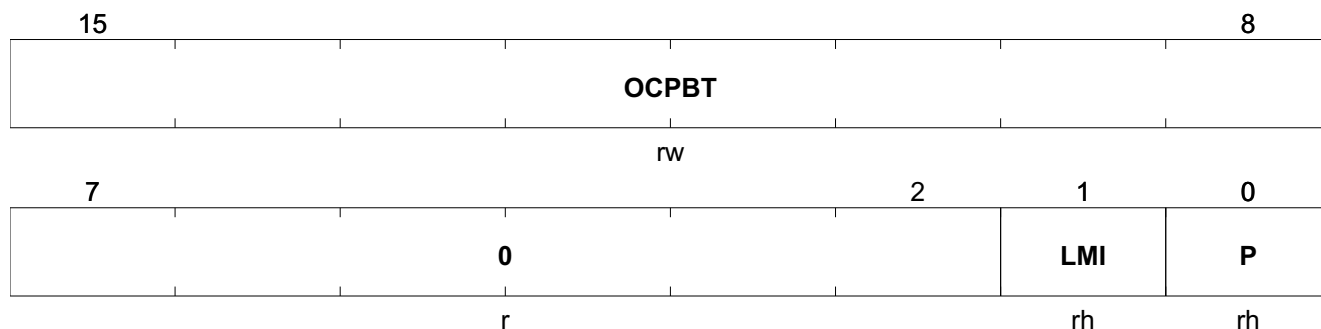


| Field | Bits | Type | Description |
|--------|------|------|--|
| DSATBT | 15:8 | rw | DESAT Blanking Time Value. This bit field defines the blanking time of the DESAT function (in OSC2 clock cycles). If the DESAT function is used, a value of at least A _H shall be programmed. |
| 0 | 7:2 | r | Reserved Read as 0 _B . |
| LMI | 1 | rh | Last Message Invalid Notification This bit indicates if the last received SPI Message was correctly processed by the device. 0 _B : Previous Message was processed correctly. 1 _B : Previous Message was discarded. |
| P | 0 | rh | Parity Bit Odd Parity Bit. |

Secondary OCP Blanking Time Register

This register configures the blanking time of the OCP function.

| SOCP | Offset | Wakeup Value | Reset Value |
|--------------------------------------|-----------------|--------------|-------------------|
| Secondary OCP Blanking Time Register | 19 _H | n.a. | 0001 _H |



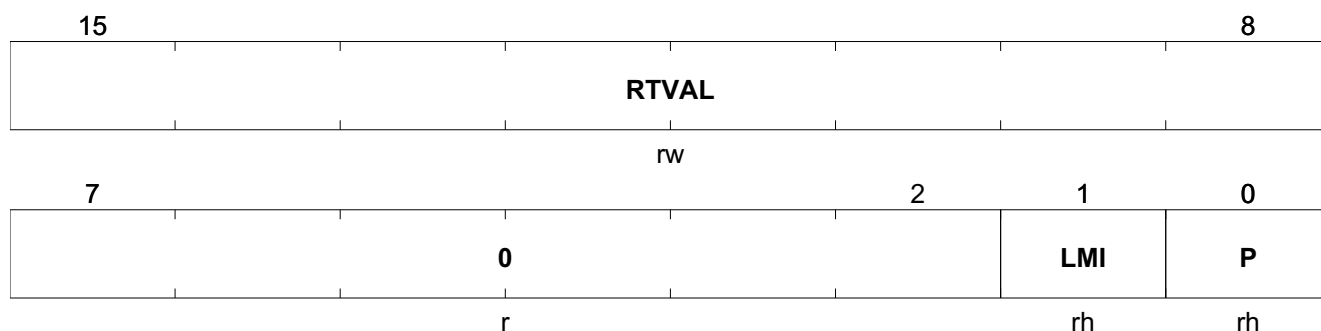
| Field | Bits | Type | Description |
|-------|------|------|---|
| OCPBT | 15:8 | rw | OCP Blanking Time Value. This bit field defines the blanking time of the OCP function (in OSC2 clock cycles). Writing 0 _H to this field deactivates the digital blanking time generation. This field shall not be programmed with values above 2F _H . |
| 0 | 7:2 | r | Reserved Read as 0 _B . |
| LMI | 1 | rh | Last Message Invalid Notification This bit indicates if the last received SPI Message was correctly processed by the device. 0 _B : Previous Message was processed correctly. 1 _B : Previous Message was discarded. |
| P | 0 | rh | Parity Bit Odd Parity Bit. |

Register Description

Secondary Regular TTOFF Configuration Register

This register shows the configuration of the TTOFF function for regular turn-off.

| SRTTOF | Offset | Wakeup Value | Reset Value |
|--|-----------------|--------------|-------------------|
| Secondary Regular TTOFF Configuration Register | 1A _H | n.a. | 0001 _H |



| Field | Bits | Type | Description |
|-------|------|------|--|
| RTVAL | 15:8 | rw | TTOFF Delay Value (regular turn-off). This bit field defines the TTOFF delay for a regular turn-off (in SSOSC2 clock cycles). Writing 00 _H to this field deactivates the TTOFF function for regular turn-off. If used, a minimal value of at least 2 _H has to be programmed. |
| 0 | 7:2 | r | Reserved Read as 0 _B . |
| LMI | 1 | rh | Last Message Invalid Notification This bit indicates if the last received SPI Message was correctly processed by the device. 0 _B : Previous Message was processed correctly. 1 _B : Previous Message was discarded. |
| P | 0 | rh | Parity Bit Odd Parity Bit. |

Register Description

Secondary Safe TTOFF Configuration Register

This register shows the configuration of the TTOFF function for safe turn-off.

| SSTOF | Offset | Wakeup Value | Reset Value |
|---|-----------------|--------------|-------------------|
| Secondary Safe TTOFF Configuration Register | 1B _H | n.a. | 2000 _H |

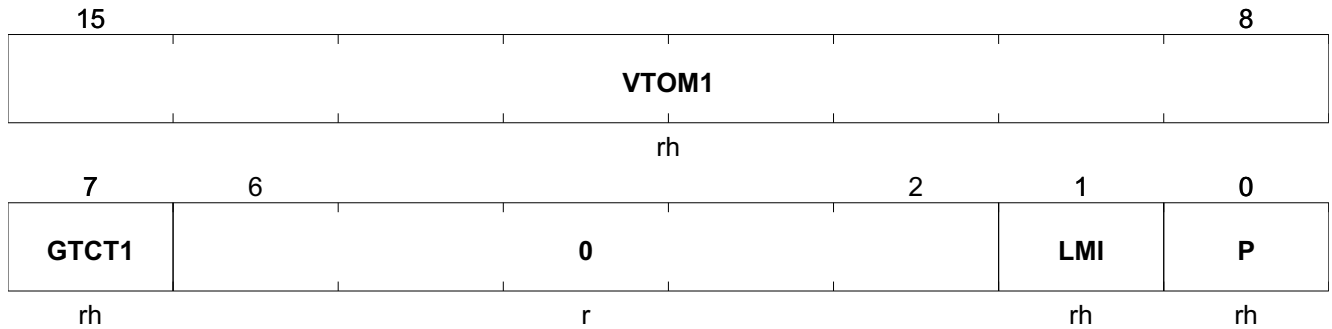
| | | | | | | | | |
|-------|--|--|---|---|---|-----|--|----|
| 15 | | | | | | | | 8 |
| STVAL | | | | | | | | |
| rw | | | | | | | | |
| 7 | | | 4 | 3 | 2 | 1 | | 0 |
| GPS | | | | 0 | | LMI | | P |
| rw | | | | r | | rh | | rh |

| Field | Bits | Type | Description |
|-------|------|------|---|
| STVAL | 15:8 | rw | TTOFF Delay Value (safe turn-off). This bit field defines the TTOFF delay for a safe turn-off (in OSC2 clock cycles). Writing 00 _H to this field deactivates the TTOFF function for regular turn-off. if used, a minimal value of at least A _H has to be programmed. <i>Note:</i> 1. In OPM5 and OPM6, it is recommended to have this bit field programmed to 0 _H . 2. In OPM4, when safe two level turn off is used, bit field STVAL shall be programmed with a higher value than field SRTTOF.RTVAL . 3. |
| GPS | 7:4 | rw | TTOFF Plateau voltage (safe turn-off) This bit field defines the TTOFF plateau voltage for safe turn-off sequences. Coding is identical to PCTRL2.GPOF . <i>Note:</i> In OPM4, bit field GPS shall be programmed with a value smaller or equal than field PCTRL2.GPOF . |
| 0 | 3:2 | r | Reserved Read as 0 _B . |
| LMI | 1 | rh | Last Message Invalid Notification This bit indicates if the last received SPI Message was correctly processed by the device. 0 _B : Previous Message was processed correctly. 1 _B : Previous Message was discarded. |
| P | 0 | rh | Parity Bit Odd Parity Bit. |

Secondary First Gate Monitoring Register

This register captures the value of the counter monitoring during the switching sequence.

| | | | |
|---|-----------------------|---------------------|-------------------------|
| SGM1 | Offset | Wakeup Value | Reset Value |
| Secondary First Gate Monitoring Register | 1C_H | n.a. | FF01_H |

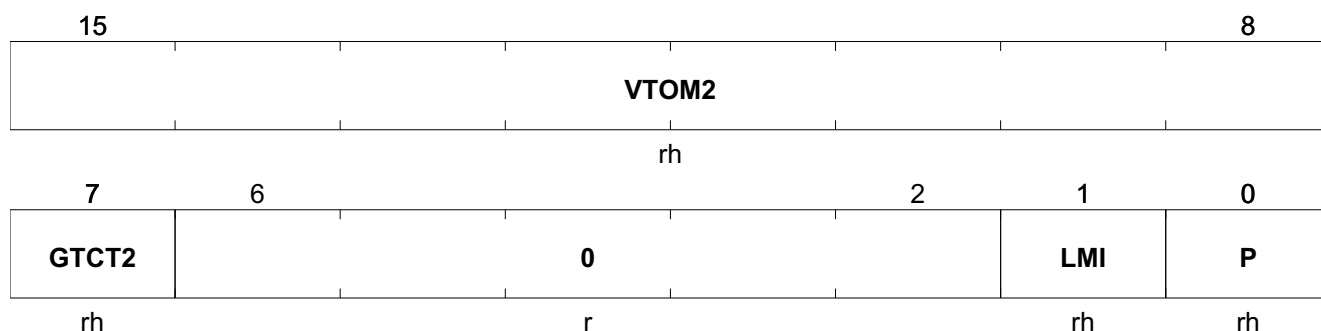


| Field | Bits | Type | Description |
|-------|------|------|---|
| VTOM1 | 15:8 | rh | Turn-Off Counter Value This bit field is used to capture the timing of signal GATE during turn-off sequences. It is cleared at the beginning of the timing measurement. |
| GTCT1 | 7 | rh | Gate Timing Capture Trigger 1 This bit indicates the state of the timing capture mechanism. When it is set, the mechanism is armed. This bit is cleared at the end of the timing measurement. <i>Note: In case a new request occurs while the mechanism is already armed, then this bit is cleared and the mechanism disarmed.</i> |
| 0 | 6:2 | r | Reserved Read as 0 _B . |
| LMI | 1 | rh | Last Message Invalid Notification This bit indicates if the last received SPI Message was correctly processed by the device. 0 _B : Previous Message was processed correctly. 1 _B : Previous Message was discarded. |
| P | 0 | rh | Parity Bit Odd Parity Bit. |

Secondary Second Gate Monitoring Register

This register captures the value of the counter monitoring during the switching sequence.

| | | | |
|--|-----------------------|---------------------|-------------------------|
| SGM2 | Offset | Wakeup Value | Reset Value |
| Secondary Second Gate Monitoring Register | 1D_H | n.a. | FF01_H |

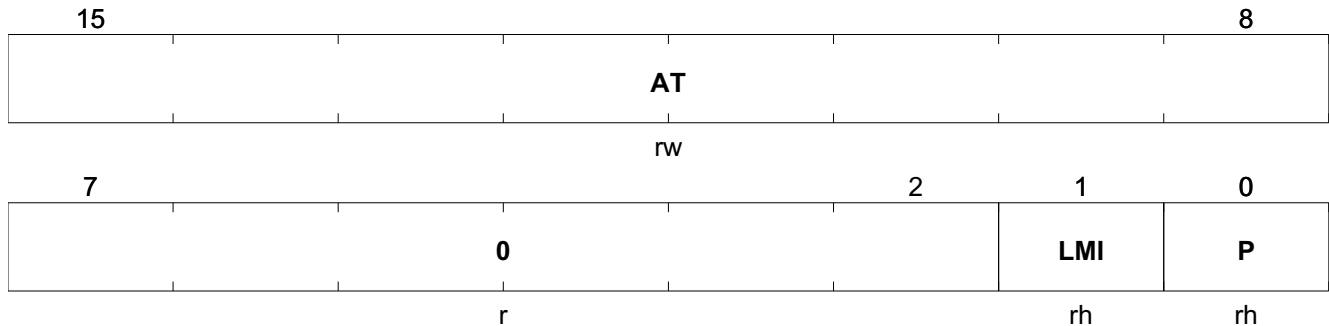


| Field | Bits | Type | Description |
|-------|------|------|---|
| VTOM2 | 15:8 | rh | Turn-On Counter Value This bit field is used to capture the timing of signal GATE during turn-on sequences. It is cleared at the beginning of the timing measurement. |
| GTCT2 | 7 | rh | Gate Timing Capture Trigger 2 This bit indicates the state of the timing capture mechanism. When it is set, the mechanism is armed. This bit is cleared at the end of the timing measurement. <i>Note: In case a new request occurs while the mechanism is already armed, then this bit is cleared and the mechanism disarmed.</i> |
| 0 | 6:2 | r | Reserved Read as 0 _B . |
| LMI | 1 | rh | Last Message Invalid Notification This bit indicates if the last received SPI Message was correctly processed by the device. 0 _B : Previous Message was processed correctly. 1 _B : Previous Message was discarded. |
| P | 0 | rh | Parity Bit Odd Parity Bit. |

Secondary DACLP Activation Configuration Register

This register defines the activation time of signal **DACLP**.

| | | | |
|---|-----------------------|---------------------|-------------------------|
| SACLT | Offset | Wakeup Value | Reset Value |
| Secondary Active Clamping Configuration Register | 1E_H | n.a. | 2600_H |

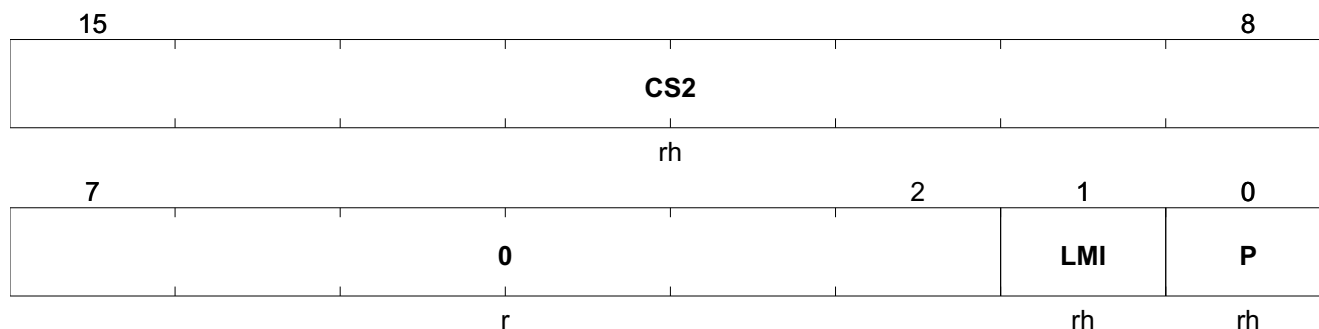


| Field | Bits | Type | Description |
|-------|------|------|---|
| AT | 15:8 | rw | Activation time This bit field defines the activation time for signal DACLP (In SSOSC2 clock cycles). 00 _H : DACLP is at constant High Level. 01 _H ...09 _H : Reserved. 0A _H ...FE _H : DACLP activation time. FF _H : DACLP is at constant Low Level. |
| 0 | 7:2 | r | Reserved Read as 0 _B . |
| LMI | 1 | rh | Last Message Invalid Notification This bit indicates if the last received SPI Message was correctly processed by the device. 0 _B : Previous Message was processed correctly. 1 _B : Previous Message was discarded. |
| P | 0 | rh | Parity Bit Odd Parity Bit. |

Secondary Clock Supervision Register

This register is for internal purpose only.

| SCS | Offset | Wakeup Value | Reset Value |
|--------------------------------------|-----------------|--------------|-------------------|
| Secondary Clock Supervision Register | 1F _H | n.a. | 0001 _H |



| Field | Bits | Type | Description |
|-------|------|------|--|
| CS2 | 15:8 | rh | Secondary Clock Supervision This bit field is written by hardware by the TCF function and gives the number of measured Start Stop Oscillator clock cycles. |
| 0 | 7:2 | r | Reserved Read as 0 _B . |
| LMI | 1 | rh | Last Message Invalid Notification This bit indicates if the last received SPI Message was correctly processed by the device. 0 _B : Previous Message was processed correctly. 1 _B : Previous Message was discarded. |
| P | 0 | rh | Parity Bit Odd Parity Bit. |

4.3 Read / Write Address Ranges

Table 4-3 summarizes which register is accessible with a READ command for a given operating mode.

Table 4-3 Read Access Validity

| | OPM1 | OPM2 | OPM3 | OPM4 | OPM5 | OPM6 |
|---------------|------|------|------|-----------------|------|-----------------|
| PID | X | X | X | X | X | X |
| PSTAT | X | X | X | X | X | X |
| PSTAT2 | X | X | X | X | X | X |
| PER | X | X | X | X | X | X |
| PCFG | X | X | X | X | X | X |
| PCTRL | X | X | X | X | X | X |
| PCTRL2 | X | X | X | X | X | X |
| PSCR | X | X | X | X | X | X |
| PRW | X | X | X | X | X | X |
| PPIN | X | X | X | X | X | X |
| PCS | X | X | X | X | X | X |
| SID | X | X | X | X ¹⁾ | X | X ¹⁾ |
| SSTAT | X | X | X | X ¹⁾ | X | X ¹⁾ |
| SSTAT2 | X | X | X | X ¹⁾ | X | X ¹⁾ |
| SER | X | X | X | X ¹⁾ | X | X ¹⁾ |
| SCFG | X | X | X | X ¹⁾ | X | X ¹⁾ |
| SCTRL | X | X | X | X ¹⁾ | X | X ¹⁾ |
| SSCR | X | X | X | X ¹⁾ | X | X ¹⁾ |
| SDESAT | X | X | X | X ¹⁾ | X | X ¹⁾ |
| SOCP | X | X | X | X ¹⁾ | X | X ¹⁾ |
| SRTTOF | X | X | X | X ¹⁾ | X | X ¹⁾ |
| SSTTOF | X | X | X | X ¹⁾ | X | X ¹⁾ |
| SGM1 | X | X | X | X ¹⁾ | X | X ¹⁾ |
| SGM2 | X | X | X | X ¹⁾ | X | X ¹⁾ |
| SACLT | X | X | X | X ¹⁾ | X | X ¹⁾ |
| SCS | X | X | X | X ¹⁾ | X | X ¹⁾ |

1) Increased latency time

Table 4-4 summarizes which register is accessible with a WRITEL command for a given operating mode.

Table 4-4 Write Access Validity

| | OPM1 | OPM2 | OPM3 | OPM4 | OPM5 | OPM6 |
|---------------|------|------|------|------|------|------|
| PID | | | | | | |
| PSTAT | | | | | | |
| PSTAT2 | | | | | | |
| PER | | | | | | |
| PCFG | | X | | | | |
| PCTRL | X | X | X | X | X | X |
| PCTRL2 | X | X | X | X | X | X |
| PSCR | | X | | | | |
| PRW | X | X | X | X | X | X |
| PPIN | | | | | | |
| PCS | | | | | | |
| SID | | | | | | |
| SSTAT | | | | | | |
| SSTAT2 | | | | | | |
| SER | | | | | | |
| SCFG | | X | | | | |
| SCTRL | | | | | | |
| SSCR | | X | | | | |
| SDESAT | | X | | | | |
| SOCP | | X | | | | |
| SRTTOF | | X | | | | |
| SSTTOF | | X | | | | |
| SGM1 | | | | | | |
| SGM2 | | | | | | |
| SACLT | | X | | | | |
| SCS | | | | | | |

5 Specification

5.1 Typical Application Circuit

Table 5-1 Component Values

| Parameter | Symbol | Values | | | Unit | Note / Test Condition |
|---|-------------|---------|--------------------|------|------------------|--|
| | | Min. | Typ. | Max. | | |
| Decoupling Capacitance (Between VEE2 and GND2) | C_d | 2 x 0.5 | 11 | - | μF | 10 μF capacitance next to the power supply source (e.g. flyback converter). 1 μF close to the device. It is strongly recommended to have at least two capacitances close to the device (e.g. 2 x 500nF). |
| Decoupling Capacitance (Between VCC2 and GND2) | C_d | - | 11 | - | μF | 10 μF capacitance next to the power supply source (e.g. flyback converter). 1 μF close to the device. |
| Decoupling Capacitance (Between VCC1 and GND1) | C_d | - | 11 | - | μF | 10 μF capacitance next to the power supply source (e.g. flyback converter). 1 μF close to the device. |
| Series Resistance | R_{s1} | 0 | 1 | - | $\text{k}\Omega$ | |
| Pull-up Resistance | R_{pu1} | - | 10 | - | $\text{k}\Omega$ | |
| Filter Resistance | R_1 | - | 1 | - | $\text{k}\Omega$ | |
| Filter Capacitance | C_1 | - | 47 | - | pF | |
| Reference Resistance | R_{ref1} | - | 26.7 ¹⁾ | - | $\text{k}\Omega$ | high accuracy, as close as possible to the device |
| Reference Capacitance | C_{ref1} | - | 100 | - | pF | As close as possible to the device. |
| Pull-up Resistance | R_{pu2} | - | 10 | - | $\text{k}\Omega$ | |
| Reference Resistance | R_{ref2} | - | 23.7 | - | $\text{k}\Omega$ | high accuracy, as close as possible to the device |
| Reference Capacitance | C_{ref2} | - | 100 | - | pF | As close as possible to the device. |
| DESAT filter Resistance | R_{desat} | 1 | 3 | - | $\text{k}\Omega$ | Depends on required response time. |
| DESAT filter Capacitance | C_{desat} | - | n/a | - | nF | Depends on required response time. |
| DESAT Diode | D_{desat} | - | n/a | - | - | HV diode. |
| OSD Filter Resistance | R_{osd} | - | 1 | - | $\text{k}\Omega$ | |
| OSD Filter Capacitance | C_{osd} | - | 47 | - | pF | |
| Sense Resistance | R_{sense} | - | n/a | - | Ω | Depends on IGBT specification. |

Table 5-1 Component Values (cont'd)

| Parameter | Symbol | Values | | | Unit | Note / Test Condition |
|--------------------------------|--------------------------|--------|------|------|------------|-------------------------------------|
| | | Min. | Typ. | Max. | | |
| OCF filter Resistance | R_{ocp} | - | n/a | - | Ω | Depends on required response time. |
| OCF filter Capacitance | C_{ocp} | - | n/a | - | nF | Depends on required response time. |
| OCPG resistance | R_{ocpg} | 0 | - | 100 | Ω | |
| DACL filter Resistance | R_{dacp} | - | 1 | - | k Ω | |
| DACL filter Capacitance | C_{dacp} | - | 470 | - | pF | |
| NUV2 Filter Resistance | R_2 | - | n/a | - | Ω | Depends on required response time. |
| NUV2 Filter Capacitance | C_2 | - | - | 100 | pF | |
| Active Clamping Resistance | R_{acl1} | - | n/a | - | Ω | Depends on application requirements |
| Active Clamping Resistance | R_{acl2} | - | n/a | - | k Ω | Depends on application requirements |
| Active Clamping Capacitance | C_{acli} | - | n/a | - | nF | Depends on application requirements |
| TVS Diode | D_{tvsac1}, D_{tvsac2} | - | n/a | - | - | Depends on application requirements |
| Active Clamping Diode | D_{acl} | - | n/a | - | - | Depends on application requirements |
| ACLI Clamping Diode | D_{acl2} | - | n/a | - | - | Depends on application requirements |
| VREG Capacitance | C_{vreg} | | 1 | | μ F | As close as possible to the device. |
| GATE Resistance | R_{gon} | 0.5 | - | - | Ω | |
| GATE Resistance | R_{goff} | 0.5 | - | - | Ω | |
| GATE Clamping Diode | D_{gcl1} | - | n/a | - | - | ²⁾ |
| GATE Clamping Diode | D_{gcl2} | - | n/a | - | - | E.g. Schottky Diode. ²⁾ |
| GATE Series Resistance | R_{gate} | 0 | 10 | - | Ω | Optional component. |
| VEE2 Clamping Diode | D_{gcl3} | - | n/a | - | - | E.g. Schottky Diode. ²⁾ |

1) 26.1 kOhm can also be used

2) Characteristics of this components are application specific.

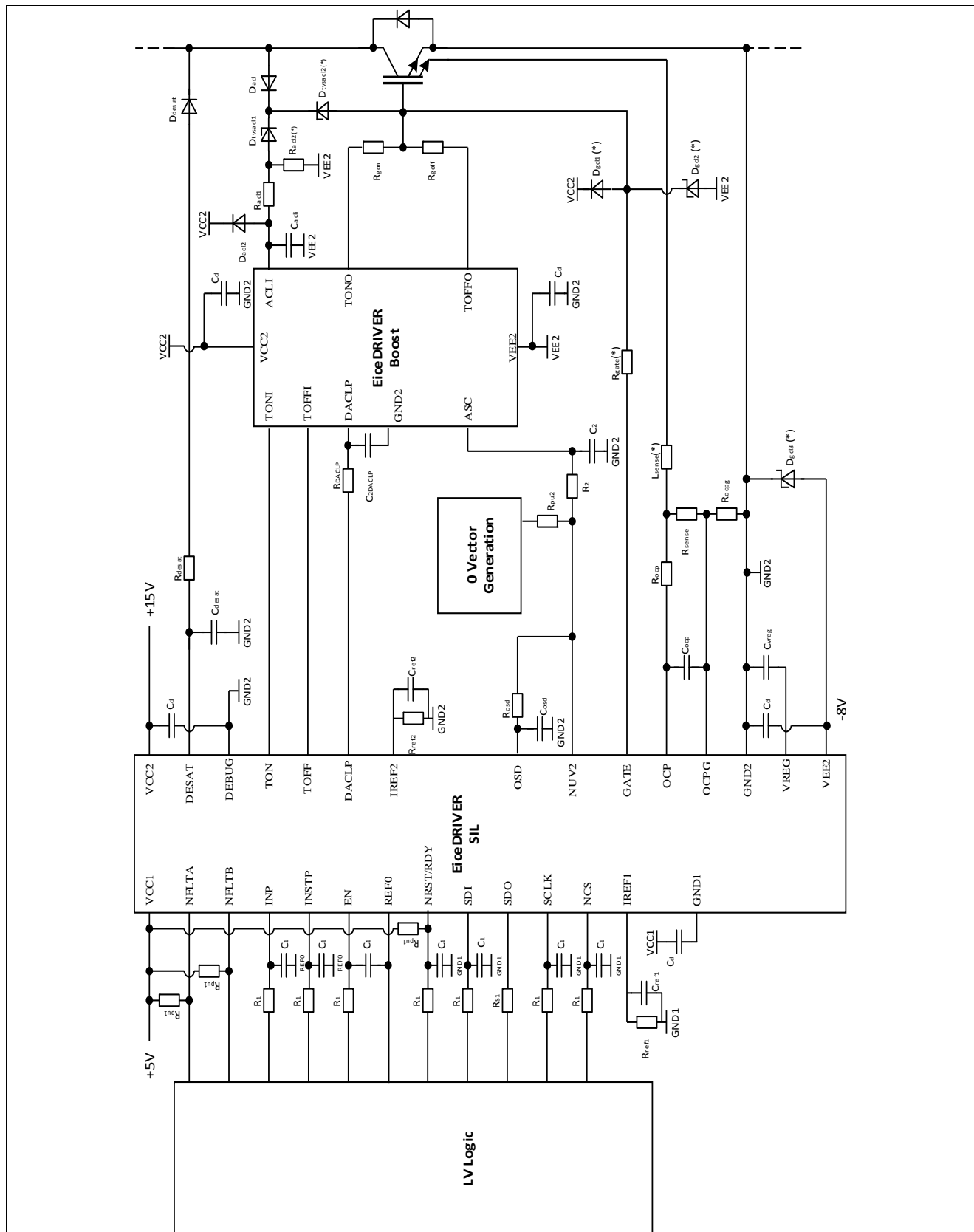


Figure 5-1 Typical Application Example

Note: Components marked with (*) are optional.

5.2 Absolute Maximum Ratings

Stress above the maximum values listed here may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Table 5-2 Absolute Maximum Ratings¹⁾

| Parameter | Symbol | Values | | | Unit | Note / Test Condition |
|---|----------------------|-----------------------|------|-----------------------|------|---|
| | | Min. | Typ. | Max. | | |
| Junction temperature | T _{JUNC} | -40 | - | 150 | °C | |
| Storage temperature | T _{STO} | -55 | - | 150 | °C | |
| Positive power supply (primary) | V _{CC1} | -0.3 | - | 6.0 | V | Referenced to GND1 |
| Positive power supply (secondary) | V _{CC2} | -0.3 | - | 28 | V | Referenced to GND2 |
| Negative power supply | V _{EE2} | -13 | - | 0.3 | V | Referenced to GND2 |
| Power supply voltage difference (secondary) V _{CC2} -V _{EE2} | V _{DS2} | - | - | 40 | V | |
| Voltage on any I/O pin on primary side except INP , INSTP , EN | V _{IN1} | -0.3 | - | 6.0 | V | Referenced to GND1 |
| Voltage on INP , INSTP , EN pins | V _{INR1} | -0.3 | - | 6.0 | V | Referenced to REF0 |
| Voltage difference between REF0 and GND1 | V _{DG1} | -5 | - | 5 | V | |
| Voltage difference between OCPG and GND2 | V _{OCPG2} | -0.3 | - | 0.3 | V | |
| Output current on push-pull I/O on primary side | I _{OUTPP1} | - | - | 20 | mA | |
| Output current on push-pull I/O on secondary side | I _{OUTPP2} | - | - | 5 | mA | |
| Output current on open drain I/O on primary side | I _{OUTOD1} | - | - | 20 | mA | |
| Output current on pin OSD , NUV2 | I _{OUTOD2} | - | - | 5 | mA | |
| Voltage on 5 V pin on secondary side. | V _{IN52} | -0.3 | - | 6.5 | V | Referenced to GND2 |
| Voltage on 15 V pin on secondary side. | V _{IN152} | V _{EE2} -0.3 | - | V _{CC2} +0.3 | V | Referenced to GND2 , except DESAT |
| Voltage on DESAT pin. | V _{INDESAT} | -0.3 | - | 20 | V | Referenced to GND2 |
| ESD Immunity | V _{ESD} | - | - | 2 | kV | HBM ²⁾ |
| | | - | - | 750 | V | CDM ³⁾ , pins 1, 16, 17, 36 |
| | | - | - | 500 | V | CDM ³⁾ , all other pins |
| MSL Level | MSL | n.a. | 3 | n.a. | | |

1) Not subject to production test. Absolute maximum Ratings are verified by design / characterization.

2) According to EIA/JESD22-A114-B.

3) According to JESD22-C101-C.

5.3 Operating range

The following operating conditions must not be exceeded in order to ensure correct operation of the 1EDI2001AS. All parameters specified in the following sections refer to these operating conditions, unless otherwise noticed.

Table 5-3 Operating Conditions

| Parameter | Symbol | Values | | | Unit | Note / Test Condition |
|-----------------------------------|---------------|--------|------|------|-------------|---|
| | | Min. | Typ. | Max. | | |
| Ambient temperature | T_{amb} | -40 | - | 125 | °C | |
| Positive power supply (primary) | V_{CC1} | 4.65 | 5.0 | 5.5 | V | Referenced to GND1 ¹⁾ |
| Positive power supply (secondary) | V_{CC2} | 13.0 | 15.0 | 18.0 | V | Referenced to GND2 ²⁾ |
| Negative power supply | V_{EE2} | -10.0 | -8.0 | -5.0 | V | Referenced to GND2 ³⁾ |
| PWM switching frequency | f_{sw} | - | - | 30 | kHz | ⁴⁾ |
| Common Mode Transient Immunity | dV_{ISO}/dt | -50 | - | 50 | kV/ μ s | At 500 V ⁵⁾ |

1) Deterministic and correct operation of the device is ensured down to V_{UVLO1L} .

2) Deterministic and correct operation of the device is ensured down to V_{UVLO2L} and up to 28V.

3) Deterministic and correct operation of the device is ensured up to 0.3V.

4) Maximum junction temperature of the device must not be exceeded.

5) Not subject to production test. This parameter is verified by design / characterization.

5.4 Thermal Characteristics

The indicated thermal parameters apply to the full operating range, unless otherwise specified.

Table 5-4 Thermal Characteristics

| Parameter | Symbol | Values | | | Unit | Note / Test Condition |
|--|---------------|--------|------|------|------|--|
| | | Min. | Typ. | Max. | | |
| Thermal Resistance Junction to Ambient | R_{THJA} | - | 60 | - | K/W | $T_{amb}=25^{\circ}\text{C}$ ¹⁾ |
| Thermal Resistance Junction to Case (bottom) | $R_{THJCBOT}$ | - | - | 41 | K/W | $T_{amb}=25^{\circ}\text{C}$ ¹⁾ , |

1) Not subject to production test. This parameter is verified by design / characterization.

5.5 Electrical Characteristics

The indicated electrical parameters apply to the full operating range, unless otherwise specified.

5.5.1 Power Supply

Table 5-5 Power Supplies Characteristics

| Parameter | Symbol | Values | | | Unit | Note / Test Condition |
|--------------------------------------|----------------|--------|--------|-------|------|---|
| | | Min. | Typ. | Max. | | |
| UVLO1 Threshold High | V_{UVLO1H} | 4.20 | 4.45 | 4.65 | V | Referenced to GND1 |
| UVLO1 Threshold Low | V_{UVLO1L} | 4.15 | 4.40 | 4.60 | V | Referenced to GND1 |
| UVLO1 Hysteresis | $V_{UVLO1HYS}$ | 40 | 70 | 100 | mV | |
| UVLO2 Threshold High | V_{UVLO2H} | 11.5 | 12.5 | 13.0 | V | Referenced to GND2 |
| UVLO2 Threshold Low | V_{UVLO2L} | 11.0 | 11.7 | 12.5 | V | Referenced to GND2 |
| UVLO2 Hysteresis | $V_{UVLO2HYS}$ | 500 | 850 | - | mV | |
| OVLO2 Threshold High | V_{OVLO2H} | 18.5 | 19.14 | 20 | V | Referenced to GND2 |
| OVLO2 Threshold Low | V_{OVLO2L} | 18.5 | 19.10 | 20 | V | Referenced to GND2 |
| UVLO3 Threshold High | V_{UVLO3H} | -12.0 | -10.99 | -10.0 | V | Referenced to GND2 |
| UVLO3 Threshold Low | V_{UVLO3L} | -12.0 | -11.02 | -10.0 | V | Referenced to GND2 |
| OVLO3 Threshold High | V_{OVLO3H} | -5.0 | -3.99 | -3.0 | V | Referenced to GND2 |
| OVLO3 Threshold Low | V_{OVLO3L} | -5.0 | -4.02 | -3.0 | V | Referenced to GND2 |
| V_{CC2} Reset Level | V_{RST2} | 7.9 | 8.3 | 8.8 | V | Referenced to GND2 |
| Quiescent Current Input Chip | I_{Q1} | - | 8.0 | 10.0 | mA | $V_{CC1}=5.5V$, all I/Os inactive, OPM0 |
| Quiescent Current Output Chip (VCC2) | I_{QVCC2} | - | 11.4 | 14.0 | mA | $V_{CC2}=18V$, $V_{EE2}=-10V$, all I/Os inactive, OPM0 |
| Quiescent Current Output Chip (VEE2) | I_{QVEE2} | -4.6 | -1.1 | - | mA | $V_{CC2}=18V$, $V_{EE2}=-10V$, all I/Os inactive, OPM0 |
| VCC1 ramp-up / down slew rate | $ t_{RP1} $ | - | - | 0.5 | V/ms | Absolute value |
| VCC2 ramp-up / down slew rate | $ t_{RP2} $ | - | - | 1.5 | V/ms | Absolute value |
| VEE2 ramp-up / down slew rate | $ t_{RP3} $ | - | - | 0.8 | V/ms | Absolute value |
| Power Dissipation - Primary Chip | P_{DIS1} | - | 37 | - | mW | $T_{AMB}=25^{\circ}C$, $V_{CC1}=5V$, all I/Os inactive, OPM0 |
| Power Dissipation - Secondary Chip | P_{DIS2} | - | 170 | - | mW | $T_{AMB}=25^{\circ}C$, $V_{CC2}=15V$, $V_{EE2}=-8V$, all I/Os inactive, OPM0 |

5.5.2 Internal Oscillators

Table 5-6 Internal Oscillators

| Parameter | Symbol | Values | | | Unit | Note / Test Condition |
|---|------------------------|--------|------|------|------|---|
| | | Min. | Typ. | Max. | | |
| Primary main oscillator frequency | f_{clk1} | 14.0 | 16.6 | 19.1 | MHz | Resistances on pin IREF1 nominal |
| Secondary main oscillator / Start-Stop Oscillator Frequency | f_{clk2}, f_{clkst2} | 15.0 | 17.1 | 19.0 | MHz | Resistances on pin IREF2 nominal |

5.5.3 Primary I/O Electrical Characteristics

Table 5-7 Electrical Characteristics for Pins: **INP, **INSTP**, **EN****

| Parameter | Symbol | Values | | | Unit | Note / Test Condition |
|---|---------------|----------------------|------|----------------------|------------|---------------------------|
| | | Min. | Typ. | Max. | | |
| Low Input Voltage | V_{INPRL1} | 0 | - | $0.3 \times V_{CC1}$ | V | Referenced to REF0 |
| High Input Voltage | V_{INPRH1} | $0.7 \times V_{CC1}$ | - | V_{CC1} | V | Referenced to REF0 |
| Weak pull down resistance INP , INSTP , EN | R_{PDIN1} | 20 | - | 100 | k Ω | To REF0 |
| Input Current | $ I_{INPR1} $ | - | - | 300 | μ A | |
| Input Pulse Suppression | t_{INPS1} | - | 20 | - | ns | ¹⁾ |
| Time between EN valid and INP High Level | t_{INPEN} | 8 | - | - | μ s | See Chapter 2.4.3 |
| INP High / Low Duration | t_{INPPD} | 250 | - | - | ns | ¹⁾ |
| INSTP High / Low Duration | $t_{INSTPPD}$ | 250 | - | - | ns | ¹⁾ |
| Duration between EN valid-to-invalid transition and the next invalid-to-valid transition | t_{ENINV} | 8 | - | - | μ s | ¹⁾ |

¹⁾ Not subject to production test. This parameter is verified by design / characterization.

Table 5-8 Electrical Characteristics for Pins: **NRST/RDY, **SCLK**, **SDI**, **NCS****

| Parameter | Symbol | Values | | | Unit | Note / Test Condition |
|---|--------------|----------------------|------|----------------------|------------|---|
| | | Min. | Typ. | Max. | | |
| Low Input Voltage | V_{INPL1} | 0 | - | $0.3 \times V_{CC1}$ | V | Referenced to GND1 |
| High Input Voltage | V_{INPH1} | $0.7 \times V_{CC1}$ | - | V_{CC1} | V | Referenced to GND1 |
| Weak pull up resistance to SCLK , SDI , NCS | R_{PUSPI1} | 26.5 | - | 100 | k Ω | To VCC1 . |
| Input Current | $ I_{INP1} $ | - | - | 400 | μ A | |
| NRST/RDY Output Voltage in Non-Ready conditions. | V_{OUTNR} | - | - | 1 | V | $V_{CC1}=5V$, $I_{load} = 2 \text{ mA}$ |
| | | - | 0.7 | 1 | V | $V_{CC1}=0V$, $I_{load} = 500 \mu\text{A}$ |
| NRST/RDY driven-active time after power supplies are within operating range. | t_{RST} | - | 15.4 | - | μ s | ¹⁾ |
| NRST/RDY minimum activation time. | t_{RSTAT} | 10 | - | - | μ s | |

¹⁾ Not subject to production test. This parameter is verified by design / characterization.

Table 5-9 Electrical Characteristics for Pins: SDO

| Parameter | Symbol | Values | | | Unit | Note / Test Condition |
|---------------------|--------------|--------|------|------|------|-----------------------|
| | | Min. | Typ. | Max. | | |
| Low Output Voltage | V_{OUTPL1} | - | - | 0.5 | V | $I_{load} = 5mA$ |
| High Output Voltage | V_{OUTPH1} | 3.85 | - | - | V | $I_{load} = 5mA$ |

Table 5-10 Electrical Characteristics for Pins: NFLTA, NFLTB

| Parameter | Symbol | Values | | | Unit | Note / Test Condition |
|--------------------|--------------|--------|------|------|------|-----------------------|
| | | Min. | Typ. | Max. | | |
| Low Output Voltage | V_{OUTDL1} | - | - | 0.5 | V | $I_{SINK}=5mA$ |

5.5.4 Secondary I/O Electrical Characteristics

Table 5-11 Electrical Characteristics for Pins: GATE, DESAT

| Parameter | Symbol | Values | | | Unit | Note / Test Condition |
|--------------------------------------|---------------|-----------|------|-------------|------|---|
| | | Min. | Typ. | Max. | | |
| DESAT Input voltage range | $V_{15DESAT}$ | 0 | - | V_{CC2} | V | Referenced to GND2 ^{1) 2)} |
| GATE Input voltage range | V_{15GATE} | V_{EE2} | - | V_{CC2} | V | Referenced to GND2 ²⁾ |
| GATE Passive Clamping Voltage | V_{PCLPG} | - | - | $V_{EE2}+1$ | V | Secondary chip not supplied, $I_{CLAMP}=10$ mA. |
| GATE Passive Clamp Current | I_{PCLPG} | 5 | - | - | mA | Secondary chip not supplied, $V_{GATE}=V_{EE2}+2V$ |

1) Pin is robust against negative transient

2) Not subject to production test. This parameter is verified by design / characterization.

Table 5-12 Electrical Characteristics for Pins: TON, TOFF

| Parameter | Symbol | Values | | | Unit | Note / Test Condition |
|--------------------------|-------------|---------------|------|---------------|------|---|
| | | Min. | Typ. | Max. | | |
| Output Voltage High | V_{15OH2} | $V_{CC2}-1$ | - | $V_{CC2}+0.3$ | V | Referenced to GND2 |
| Output Voltage Low | V_{15OL2} | $V_{EE2}-0.3$ | - | $V_{EE2}+1$ | V | Referenced to GND2 |
| Source / Sink Current | I_{15O2} | 1 | - | - | A | Pin TOFF / TON ¹⁾ |
| Passive Clamping Voltage | V_{PCLP} | - | - | $V_{EE2}+2$ | V | Secondary chip not supplied, $I_{CLAMP}=10$ mA. |

1) Not subject to production test. This parameter is verified by design / characterization.

Table 5-13 Electrical Characteristics for Pins: OSD, DEBUG

| Parameter | Symbol | Values | | | Unit | Note / Test Condition |
|--------------------------------|--------------|--------|------|------|------------|---------------------------|
| | | Min. | Typ. | Max. | | |
| Low Input Voltage | V_{5INL2} | 0 | - | 1.5 | V | Referenced to GND2 |
| High Input Voltage | V_{5INH2} | 3.5 | - | 5.5 | V | Referenced to GND2 |
| Weak pull down on DEBUG | R_{PDIN2} | 40 | 100 | 175 | k Ω | To GND2 . |
| Weak pull down on OSD | R_{PDOSD2} | 60 | 100 | 175 | k Ω | To GND2 |

Table 5-14 Electrical Characteristics for Pin: **NUV2**

| Parameter | Symbol | Values | | | Unit | Note / Test Condition |
|--------------------|--------------|--------|------|------|------|--|
| | | Min. | Typ. | Max. | | |
| Low Output Voltage | V_{OUTDL2} | 0 | - | 0.5 | V | $I_{SINK}=5mA$, Referenced to GND2 |

Table 5-15 Electrical Characteristics for Pins: **DACL**

| Parameter | Symbol | Values | | | Unit | Note / Test Condition |
|---------------------|------------|--------|------|------|------|--|
| | | Min. | Typ. | Max. | | |
| Output Voltage High | V_{5OH2} | 4.0 | - | 5.25 | V | Referenced to GND2 , $I_{LOAD}=2mA$ |
| Output Voltage Low | V_{5OL2} | 0 | - | 0.5 | V | Referenced to GND2 , $I_{LOAD}=2mA$ |

Table 5-16 Electrical Characteristics for Pin: **VREG**

| Parameter | Symbol | Values | | | Unit | Note / Test Condition |
|----------------------------------|------------|--------|------|------|---------|---|
| | | Min. | Typ. | Max. | | |
| VREG output voltage range | V_{REG2} | 4.75 | 5 | 5.30 | V | Referenced to GND2 , $C_{LOAD}=1\mu F$ |
| VREG output DC current | I_{REG2} | - | - | 525 | μA | ¹⁾ |

1) Not subject to production test. This parameter is verified by design / characterization.

5.5.5 Switching Characteristics

Table 5-17 Switching Characteristics

| Parameter | Symbol | Values | | | Unit | Note / Test Condition |
|---|-----------------|--------|-------|--------|------------|---|
| | | Min. | Typ. | Max. | | |
| Input to Output Propagation Delay ON | t_{PDON} | 175 | 215 | 255 | ns | $V_{CC1}=5V, V_{CC2}=15V, V_{EE2}=-8V$ |
| Input to Output Propagation Delay OFF | t_{PDOFF} | 175 | 215 | 255 | ns | $V_{CC1}=5V, V_{CC2}=15V, V_{EE2}=-8V$ |
| Input to Output Propagation Delay Distortion ($t_{PDOFF}-t_{PDON}$) | t_{PDISTO} | -20 | 0 | 40 | ns | $V_{CC1}=5V, V_{CC2}=15V, V_{EE2}=-8V$ |
| Input to Output Propagation Delay Distortion Variation for two consecutive pulses | $t_{PDISTOV}$ | - | 25 | - | ns | $V_{CC1}=5V, V_{CC2}=15V, V_{EE2}=-8V, T_{JUNC}=25^{\circ}C$ ¹⁾ |
| Rise Time | t_{RISE} | - | 120 | 205 | ns | $V_{CC1}=5V, V_{CC2}=15V, V_{EE2}=-8V, C_{LOAD} = 10nF, 10\%-90\%$ |
| | | - | 30 | 50 | ns | $V_{CC1}=5V, V_{CC2}=15V, V_{EE2}=-8V, \text{no Load}, 90\%-10\%$ |
| Fall Time | t_{FALL} | - | 150 | 235 | ns | $V_{CC1}=5V, V_{CC2}=15V, V_{EE2}=-8V, C_{LOAD} = 10nF, 90\%-10\%$ |
| | | - | 60 | 100 | ns | $V_{CC1}=5V, V_{CC2}=15V, V_{EE2}=-8V, \text{no Load}, 90\%-10\%$ |
| TTOFF Plateau level | V_{GPOF0} | 9.250 | 9.740 | 10.250 | V | Referenced to GND2 , measured at pin TON (shorted with TOFF) $V_{CC2}=15V, T_{JUNC}=25^{\circ}C$, no VBE Compensation. |
| | V_{GPOF1} | 9.335 | 9.820 | 10.335 | V | |
| | ... | ... | ... | ... | ... | |
| | V_{GPOF14} | 10.440 | 10.95 | 11.440 | V | |
| | V_{GPOF15} | 11.1 | 11.7 | 12.3 | V | |
| TTOFF Plateau level | V_{GPOF0} | 8.600 | 9.08 | 9.600 | V | Referenced to GND2 , measured at pin TON (shorted with TOFF) $V_{CC2}=15V, T_{JUNC}=25^{\circ}C$, with VBE Compensation. |
| | V_{GPOF1} | 8.685 | 9.16 | 9.685 | V | |
| | ... | ... | ... | ... | ... | |
| | V_{GPOF14} | 9.790 | 10.28 | 10.790 | V | |
| | V_{GPOF15} | 10.4 | 11.0 | 11.6 | V | |
| Variation from configured V_{TTOFF} @ $T_J = -40^{\circ}C$ | dV_{Tm40} | - | 40 | - | mV | ¹⁾ |
| Variation from configured V_{TTOFF} @ $T_J = 150^{\circ}C$ | dV_{T150} | - | -80 | - | mV | ¹⁾ |
| TTOFF decrease rate | t_{SLEW} | - | 9 | - | V/ μs | |
| TTOFF delay deviation from nominal value | $t_{DEVTTTOFF}$ | -100 | 0 | 100 | ns | For a target time of 2 μs , using the TCF. ¹⁾ |

Table 5-17 Switching Characteristics (cont'd)

| Parameter | Symbol | Values | | | Unit | Note / Test Condition |
|---|-------------|--------|-------------|-------|---------------|---|
| | | Min. | Typ. | Max. | | |
| TTOFF (Regular) Plateau Time | t_{TTOFF} | 2.00 | 2.22 | 2.54 | μs | SRTTOF.RTVAL =26 _H , assuming no TCF. |
| Gate Voltage Reference 1 | V_{GATE1} | - | $V_{EE2}+2$ | - | V | Measured at pin GATE |
| Gate Voltage Reference 2 | V_{GATE2} | - | $V_{CC2}-3$ | - | V | Measured at pin GATE |
| Output Stage Monitoring (TON) | V_{OSMON} | - | $V_{CC2}-3$ | - | V | |
| Output Stage Monitoring (TOFF) | V_{OSMOF} | - | $V_{EE2}+2$ | - | V | |
| Active Clamping Activation Time | t_{ACL} | 2.00 | 2.22 | 2.54 | μs | Default value of bit field SACLT.AT . |
| WTO Level | V_{GPON0} | 8.65 | 9.25 | 9.95 | V | Referenced to GND2 , measured at pin TON (shorted with TOFF) $V_{CC2}=15\text{V}$, $T_{JUNC}=25^{\circ}\text{C}$, no VBE Compensation. |
| | V_{GPON1} | 9.85 | 10.5 | 11.25 | V | |
| | V_{GPON2} | 10.75 | 11.4 | 12.1 | V | |
| WTO Level | V_{GPON0} | 9.15 | 9.9 | 10.75 | V | Referenced to GND2 , measured at pin TON (shorted with TOFF) $V_{CC2}=15\text{V}$, $T_{JUNC}=25^{\circ}\text{C}$, with VBE Compensation. |
| | V_{GPON1} | 10.4 | 11.0 | 11.6 | V | |
| | V_{GPON2} | 11.1 | 11.6 | 12.2 | V | |

1) Not subject to production test. Parameters are verified by design / characterization.

5.5.6 Desaturation Protection

Table 5-18 DESAT characteristics

| Parameter | Symbol | Values | | | Unit | Note / Test Condition |
|--|-----------------------|--------|------|------|------------------|--|
| | | Min. | Typ. | Max. | | |
| DESAT Reference Level | V_{DESAT0} | 8.4 | 9 | 9.4 | V | $V_{\text{CC2}} = 15\text{V}$, $V_{\text{EE2}} = -8\text{V}$ |
| DESAT Pull-up Resistance | R_{PUDSAT2} | 19.5 | 30 | 50 | $\text{k}\Omega$ | to VCC2 |
| DESAT Low Voltage | V_{DESATL} | - | 200 | - | mV | Referenced to GND2 , Desat clamping enabled, $I_{\text{sink}} = 5\text{mA}$. |
| DESAT blanking time deviation from programmed value | dt_{DESATBL} | -20 | - | +20 | % | After transition of the PWM command, assuming a 1 μs programmed blanking time ¹⁾ |

1) Not subject to production test. Parameters are verified by design / characterization.

5.5.7 Overcurrent Protection

Table 5-19 OCP characteristics

| Parameter | Symbol | Values | | | Unit | Note / Test Condition |
|--|---------------------|--------|------|------|------------------|--|
| | | Min. | Typ. | Max. | | |
| OC error detection threshold | V_{OCPD1} | 270 | 300 | 330 | mV | Referenced to OCPG |
| OC current warning detection threshold | V_{OCPD2} | 35 | 50 | 70 | mV | Referenced to OCPG |
| OCP blanking time deviation from programmed value | dt_{OCPBL} | -20 | - | +20 | % | After transition of the PWM command, assuming a 1 μs programmed blanking time ¹⁾ |
| OCP Pull-up Resistance | R_{PUOCP2} | 40 | 100 | 175 | $\text{k}\Omega$ | to internal 5V reference. |

1) Not subject to production test. Parameters are verified by design / characterization.

5.5.8 Over temperature Warning

Table 5-20 Over temperature Warning Characteristics

| Parameter | Symbol | Values | | | Unit | Note / Test Condition |
|--------------------------------|--------------|--------|------|------|------|-----------------------|
| | | Min. | Typ. | Max. | | |
| Threshold Junction Temperature | T_{j_ovt} | 140 | - | - | °C | 1) |

1) Not subject to back-end test

5.5.9 Error Detection Timing

Table 5-21 Error Detection Timing

| Parameter | Symbol | Values | | | Unit | Note / Test Condition |
|---|-----------------|--------|------|------|------|--|
| | | Min. | Typ. | Max. | | |
| Dead Time for Shoot Through Protection | t_{DEAD} | 840 | - | 1200 | ns | |
| Class A event detection to NFLTA activation | t_{AFLTA} | - | 2 | 4.5 | μs | |
| Class A event detection to turn off sequence activation | t_{OFFCLA} | - | - | 400 | ns | $V_{TOFF}=V_{CC2} - 1\text{ V}$ |
| DESAT event detection to turn off sequence activation | $t_{OFFDESAT2}$ | - | - | 430 | ns | $V_{TOFF}=V_{CC2} - 1\text{ V}$, after blanking time elapsed |
| OCP event occurrence to turn off sequence activation | $t_{OFFOCP2}$ | - | 110 | 130 | ns | $V_{TOFF}=V_{CC2} - 1\text{ V}$, after blanking time elapsed |
| Class B event detection to NFLTB activation | t_{BFLTB} | - | 2 | 4.5 | μs | |
| Class B event detection to turn off sequence activation | $t_{OFFCLB2}$ | - | - | 400 | ns | $V_{TOFF}=V_{CC2} - 1\text{ V}^{1)}$ |
| Verification Mode time out | t_{VMTO} | - | 15 | - | ms | After a transition from OPM2 to OPM5, SCFG.TOSEN = 0 _B |
| | | - | 60 | - | ms | After a transition from OPM2 to OPM5, SCFG.TOSEN = 1 _B |
| Gate Monitoring time out | t_{GMTO} | - | 15.0 | - | μs | ¹⁾ |
| Life sign error detection time | t_{LS} | - | 5 | - | μs | After error condition detected by logic. |
| Output stage monitor inhibit time. | t_{OSM} | - | 4 | - | μs | After hard transition ¹⁾ . |

1) Verified by design / characterization. Not tested in production.

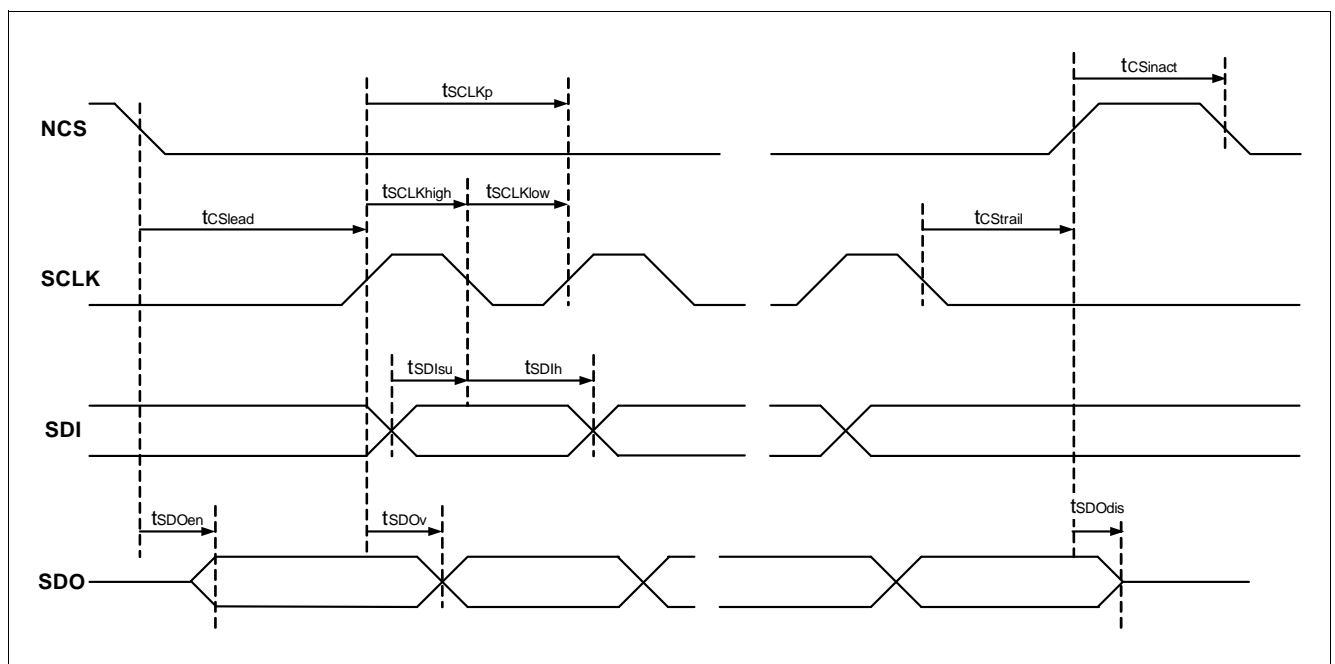
5.5.10 SPI Interface

Table 5-22 SPI Interface Characteristics

| Parameter | Symbol | Values | | | Unit | Note / Test Condition |
|--------------------------|----------------------|--------|--------------|------|------|---|
| | | Min. | Typ. | Max. | | |
| SPI frame size | N_{bit} | N.a. | $N \cdot 16$ | N.a. | bit | N is the daisy chain length |
| Baud rate | f_{SCLK} | 0.1 | - | 2.0 | MHz | Standard SPI configuration, ¹⁾ |
| | | 0.1 | - | 1.8 | MHz | Daisy chain configuration, ¹⁾ |
| SCLK duty cycle | D_{SCLK} | 45 | - | 55 | % | ²⁾ |
| SDI set-up time | t_{SDIsu} | 65 | - | - | ns | ²⁾ |
| SDI hold time | t_{SDIh} | 100 | - | - | ns | ²⁾ |
| NCS lead time | t_{CSlead} | 1 | - | - | μs | ²⁾ |
| NCS trail time | t_{CStrail} | 1 | - | - | μs | ²⁾ |
| NCS inactive time | t_{CSinact} | 10 | - | - | μs | ²⁾ |
| SDO enable time | t_{SDOen} | - | - | 500 | ns | $C_{\text{load}} = 20\text{pF}^{2)}$ |
| SDO disable time | t_{SDOdis} | - | - | 1 | μs | $C_{\text{load}} = 20\text{pF}^{2)}$ |
| SDO valid time | t_{SDOv} | 10 | - | 185 | ns | $C_{\text{load}} = 20\text{pF}^{2)}$ |

1) Low Limit verified by design / characterization. Not tested in production.

2) Verified by design / characterization. Not tested in production.


Figure 5-2 SPI Interface Timing

5.5.11 Insulation Characteristics

Table 5-23 Isolation Characteristics referring to DIN EN 60747-5-2 (VDE 0884 - 2):2003-01

| Description | Symbol | Characteristic | Unit |
|--|-------------------|-----------------------------|-------------------|
| Installation classification per EN60664-1, Table 1: rated main voltage less than 150 V _{rms} rated main voltage less than 300 V _{rms} rated main voltage less than 600 V _{rms} | | I - IV I - III I - II | |
| Climatic Classification | | 40 / 125 / 21 | |
| Pollution Degree (EN 60664-1) | | 2 | |
| Minimum External Clearance | CLR | 8.12 | mm |
| Minimum External Creepage | CPG | 8.24 | mm |
| Minimum Comparative Tracking Index | CTI | 175 | |
| Maximum Repetitive Insulation Voltage | V _{IORM} | 1420 | V _{PEAK} |
| Highest Allowable Overvoltage ¹⁾ | V _{IOTM} | 6000 | V _{PEAK} |
| Maximum Surge Insulation Voltage | V _{IOSM} | 6000 | V _{PEAK} |

1) Refer to VDE 0884 for a detailed description of Method a and Method b partial discharge

Table 5-24 Isolation Characteristics referring to UL 1577

| Description | Symbol | Characteristic | Unit |
|---------------------------------|------------------|----------------|------------------|
| Insulation Test Voltage / 1 min | V _{ISO} | 3750 | V _{rms} |
| Insulation Test Voltage / 1 sec | V _{ISO} | 4500 | V _{rms} |

6 Package Information

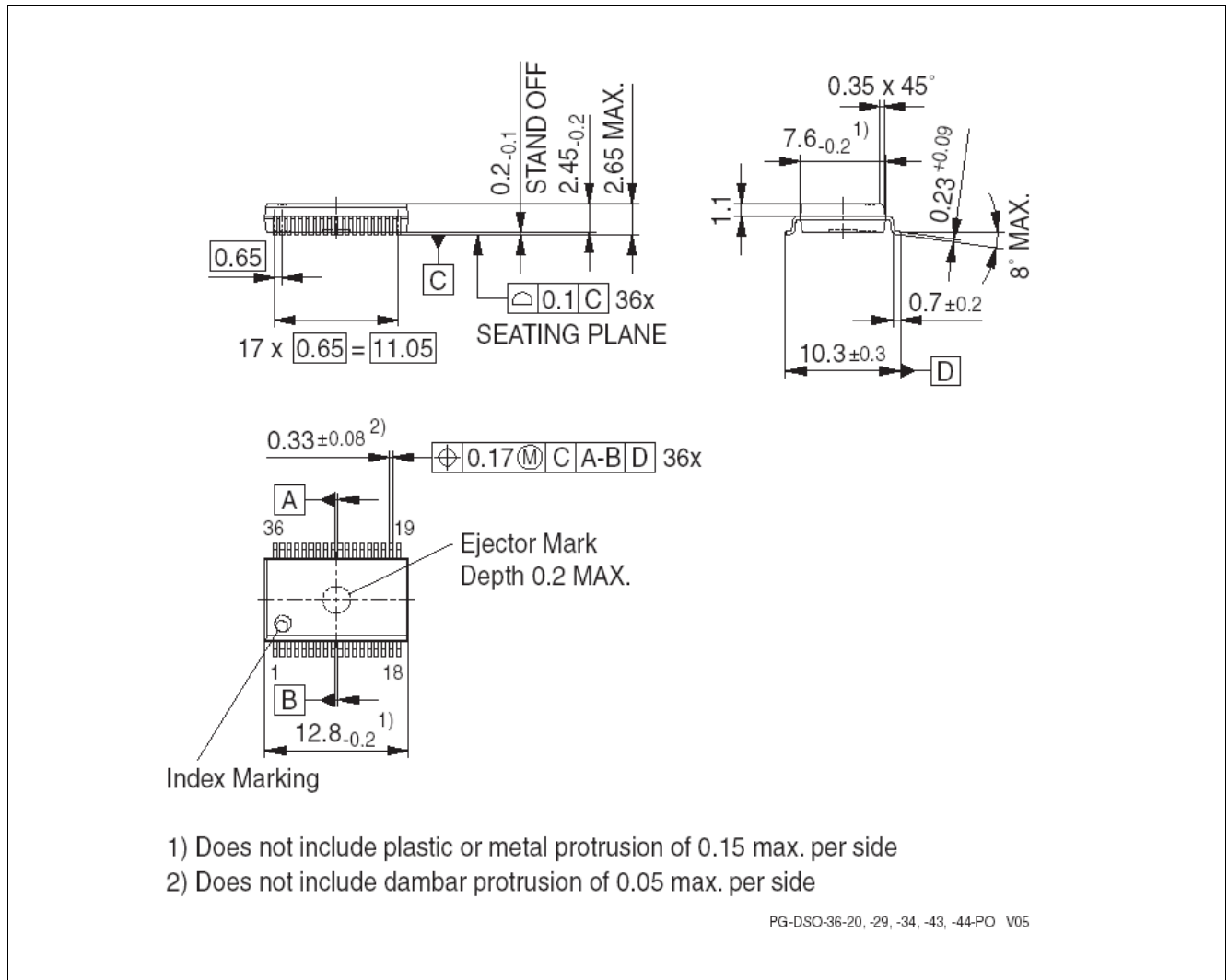


Figure 6-1 Package Dimensions

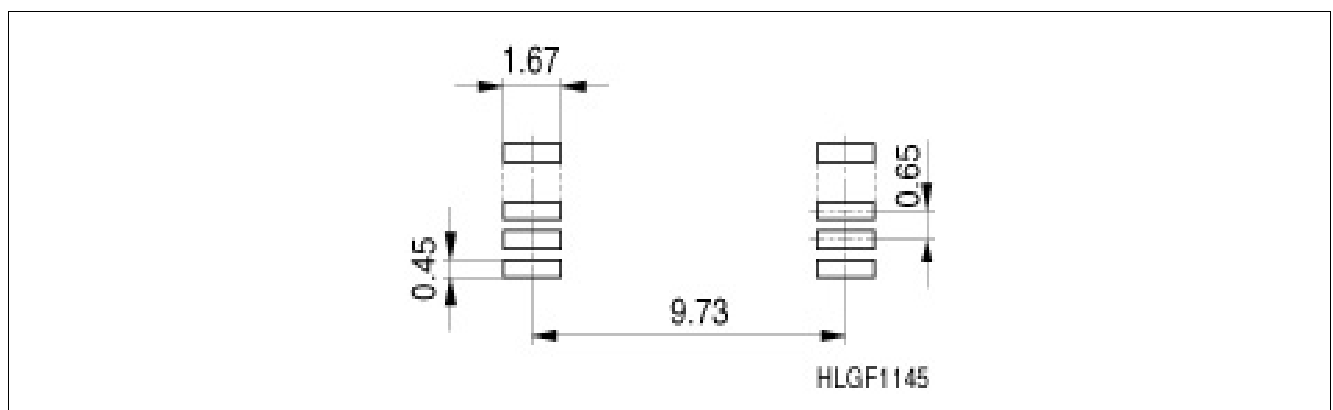


Figure 6-2 Recommended Footprint

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