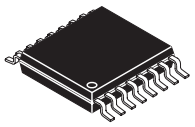
Document Number: MPC17517
Rev. 2.0, 7/2006

1.0 A 6.8 V Dual Motor Driver IC

17517

DUAL MOTOR DRIVER



DTB SUFFIX
98ASH70247A
16-PIN TSSOP

The 17517 is a monolithic triple totem-pole-output power IC designed to be used in portable electronic applications to control small DC motors and solenoids. The 17517 can operate efficiently with supply voltages as low as 2.0 V to as high as 6.8 V. Its low $R_{DS(ON)}$ totem-pole output MOSFETs (0.46 Ω typical) can provide continuous drive currents of 1.0 A and handle peak currents up to 3.0 A. It is easily interfaced to low-cost MCUs via parallel 3.0 V- or 5.0 V-compatible logic. The device can be pulse width modulated (PWM-ed) at up to 200 kHz.

The 17517 can drive two motors in two directions one at a time or drive one motor in two directions and one solenoid with synchronous rectification of freewheeling currents one at a time. Two-motor operation is accomplished by hooking one motor between OUTA and OUTB and hooking the other motor between OUTB and OUTC. Motor plus solenoid operation is accomplished by hooking a motor between OUTA and OUTB and a solenoid between OUTC and GND.

This device contains an integrated charge pump and level shifter (for gate drive voltages), integrated shoot-through current protection (cross-conduction suppression logic and timing), and undervoltage detection and shutdown circuitry.

The 17517 has four operating modes: Forward, Reverse, Brake, and Tri-Stated (High Impedance).

ORDERING INFORMATION		
Device	**Temperature Range (T_A)**	**Package**
MPC17517DTB/R2	-20°C to 65°C	16 TSSOP

Features

- 2.0 V to 6.8 V Continuous Operation
- Output Current 1.0 A (DC), 3.0 A (Peak)
- MOSFETs < 600 mΩ $R_{DS(ON)}$ @ 25°C Guaranteed
- 3.0 V/5.0 V TTL-/CMOS-Compatible Inputs
- PWM Frequencies up to 200 kHz
- Undervoltage Shutdown

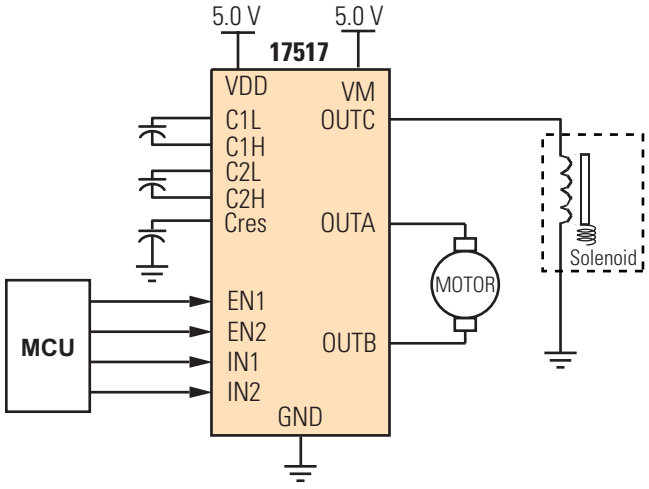


Figure 1. 17517 Simplified Application Diagram

* This document contains certain information on a new product.
Specifications and information herein are subject to change without notice.

INTERNAL BLOCK DIAGRAM

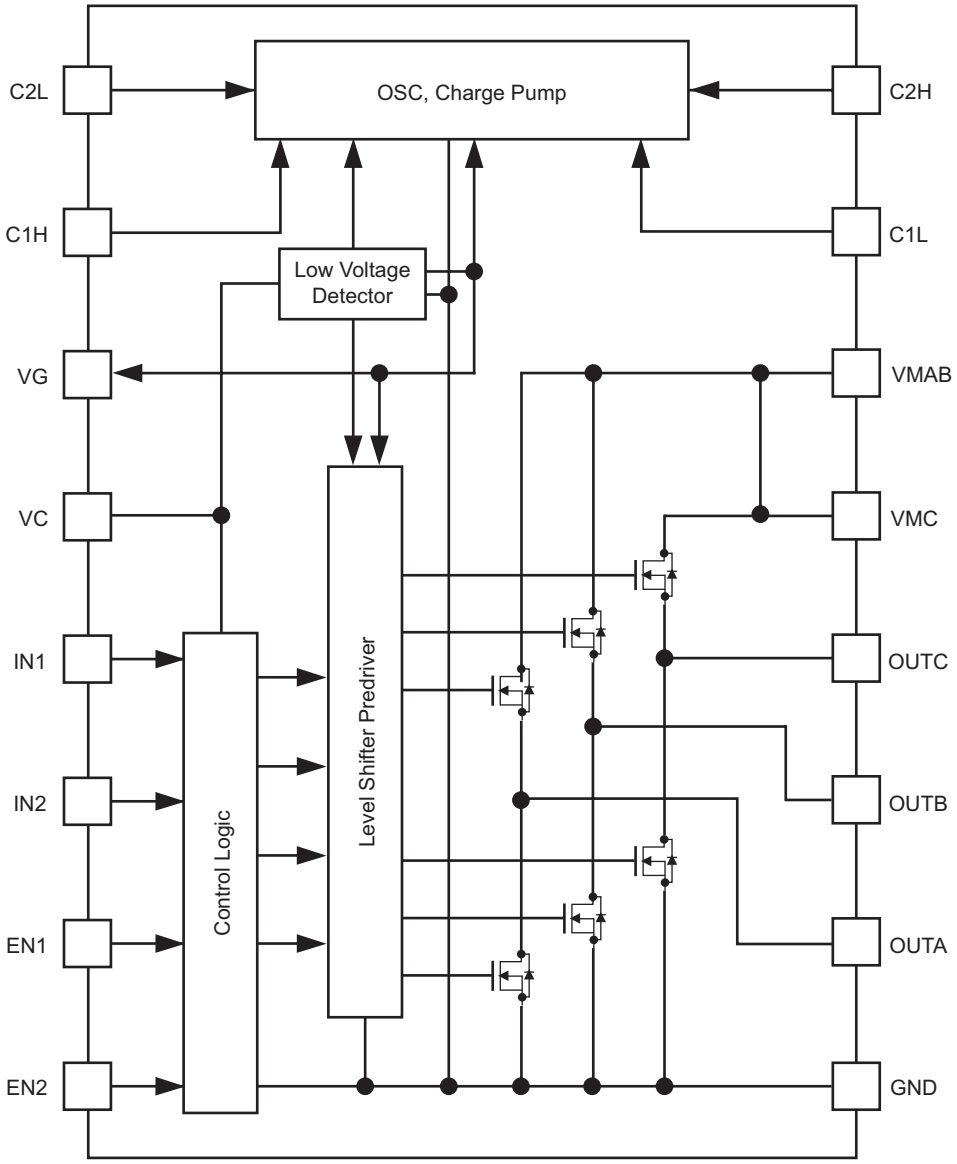


Figure 2. 17517 Simplified Internal Block Diagram

PIN CONNECTIONS

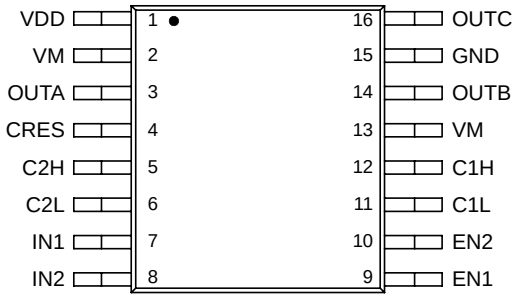


Figure 3. 17517 Pin Connections

Table 1. 17517 Pin Definitions

A functional description of each pin can be found in the Functional Pin Description section beginning on page 9.

Pin Number	Pin Name	Formal Name	Definition
1	VDD	Control Circuit Power Supply	Positive power source connection for control circuit.
2, 13	VM	Motor Drive Power Supply	Motor power supply voltage input pins.
3	OUTA	Output A	Driver output A pin.
4	CRES	Charge Pump Output Capacitor Connection	Charge pump reservoir capacitor pin.
5	C2H	Charge Pump 2H	Charge pump bucket capacitor 2 (positive pole).
6	C2L	Charge Pump 2L	Charge pump bucket capacitor 2 (negative pole).
7	IN1	Input Control 1	Control signal input 1 pin.
8	IN2	Input Control 2	Control signal input 2 pin.
9	EN1	Enable Control Signal Input 1	Enable control signal input 1 pin.
10	EN2	Enable Control Signal Input 2	Enable control signal input 2 pin.
11	C1L	Charge Pump 1L	Charge pump bucket capacitor 1 (negative pole).
12	C1H	Charge Pump 1H	Charge pump bucket capacitor 1 (positive pole).
14	OUTB	Output B	Driver output B pin.
15	GND	Ground	Ground connection.
16	OUTC	Output C	Driver output C pin.

ELECTRICAL CHARACTERISTICS

MAXIMUM RATINGS

Table 2. Maximum Ratings

All voltages are with respect to ground unless otherwise noted. Exceeding these ratings may cause a malfunction or permanent damage to the device.

Ratings	Symbol	Value	Unit
ELECTRICAL RATINGS			
Motor Supply Voltage	V_M	-0.5 to 8.0	V
Charge Pump Output Voltage	V_{CRES}	-0.5 to 14	V
Logic Supply Voltage	V_{DD}	-0.5 to 7.0	V
Signal Input Voltage	V_{IN}	-0.5 to V_{DD}+0.5	V
Driver Output Current Continuous Peak (1)	 I_O I_{OPK}	 1.0 3.0	A
ESD Voltage (2) Human Body Model Machine Model	 V_{ESD1} V_{ESD2}	 ±2000 ±100	V
THERMAL RATINGS			
Storage Temperature Range	T_{STG}	-65 to 150	°C
Operating Junction Temperature	T_J	-20 to 150	°C
Operating Ambient Temperature	T_A	-20 to 65	°C
Thermal Resistance (3)	$R_{\theta JA}$	190	°C/W
Power Dissipation (4)	P_D	657	mW
Soldering Temperature (5)	T_{SOLDER}	245	°C

Notes

1. T_A = 25°C, 10 ms pulse width at 200 ms intervals.
2. ESD1 testing is performed in accordance with the Human Body Model (C_{ZAP} = 100 pF, R_{ZAP} = 1500 Ω), ESD2 testing is performed in accordance with the Machine Model (C_{ZAP} = 200 pF, R_{ZAP} = 0 Ω).
3. 37 mm x 50 mm Cu area (1.6 mm FR-4 PCB).
4. Maximum at T_A = 25°C.
5. Soldering temperature limit is for 10 seconds maximum duration. Not designed for immersion soldering. Exceeding these limits may cause malfunction or permanent damage to the device.

STATIC ELECTRICAL CHARACTERISTICS

Table 3. Static Electrical Characteristics

Characteristics noted under conditions T_A = 25°C, V_{DD} = V_M = 5.0 V, GND = 0 V unless otherwise noted. Typical values noted reflect the approximate parameter means at T_A = 25°C under nominal conditions unless otherwise noted.

Characteristic	Symbol	Min	Typ	Max	Unit
POWER					
Motor Supply Voltage	V_M	2.0	5.0	6.8	V
Logic Supply Voltage	V_{DD}	2.7	5.0	5.7	V
Capacitor for Charge Pump	C1, C2, C3	0.01	0.1	1.0	µF
Standby Power Supply Current					
Motor Supply Standby Current	I_{VMSTBY}	–	–	1.0	µA
Logic Supply Standby Current (6)	$I_{VDDSTBY}$	–	–	1.0	mA
Operating Power Supply Current					mA
Logic Supply Current (7)	I_{VDD}	–	–	3.0	
Charge Pump Circuit Supply Current	I_{CRES}	–	–	0.7	
Low-Voltage Detection Circuit	V_{DD}DET				V
Detection Voltage (V_{DD}) (8)		1.5	2.0	2.5	
Driver Output ON Resistance (9)	$R_{DS(ON)}$	–	0.46	0.60	W
GATE DRIVE					
Gate Drive Voltage (10)	V_{CRES}				V
No Current Load		12	13	13.5	
Gate Drive Ability (Internally Supplied)	$V_{CRESLOAD}$				V
I_{CRES} = -1.0 mA		10	11.2	–	
CONTROL LOGIC					
Logic Input Voltage	V_{IN}	0	–	V_{DD}	V
Logic Input Function (2.7 V < V_{DD} < 5.7 V)					
High-Level Input Voltage	V_{IH}	V_{DD} x0.7	–	–	V
Low-Level Input Voltage	V_{IL}	–	–	V_{DD} x0.3	V
High-Level Input Current	I_{IH}	–	–	1.0	µA
Low-Level Input Current	I_{IL}	-1.0	–	–	µA

Notes

6. $I_{VDDSTBY}$ includes current to the predriver circuit.
7. I_{VDD} includes current to the predriver circuit.
8. Detection voltage is defined as when the output becomes high-impedance after V_{DD} drops below the detection threshold. When the gate voltage V_{CRES} is applied from an external source, V_{CRES} = 7.5 V.
9. I_O = 1.0 A source + sink.
10. Input logic signal not present.

DYNAMIC ELECTRICAL CHARACTERISTICS

Table 4. Dynamic Electrical Characteristics

Characteristics noted under conditions T_A = 25°C, V_{DD} = V_M = 5.0 V, GND = 0 V unless otherwise noted. Typical values noted reflect the approximate parameter means at T_A = 25°C under nominal conditions unless otherwise noted.

Characteristic	Symbol	Min	Typ	Max	Unit
INPUT (IN1, IN2, EN1, EN2)					
Pulse Input Frequency	f_{IN}	–	–	200	kHz
Input Pulse Rise Time (11)	t_R	–	–	1.0 (12)	µs
Input Pulse Fall Time (13)	t_F	–	–	1.0 (12)	µs
OUTPUT					
Propagation Delay Time					µs
Turn-ON Time	t_{PLH}	–	0.1	0.5	
Turn-OFF Time	t_{PHL}	–	0.1	0.5	
Charge Pump Wake-Up Time (14)	t_{VGON}	–	0.1	3.0	ms
Low-Voltage Detection Time	$t_{V_{DD}DET}$	–	–	10	ms

Notes
11. Time is defined between 10% and 90%.
12. That is, the input waveform slope must be steeper than this.
13. Time is defined between 90% and 10%.
14. When C1 = C2 = C3 = 0.1 µF.

TIMING DIAGRAMS

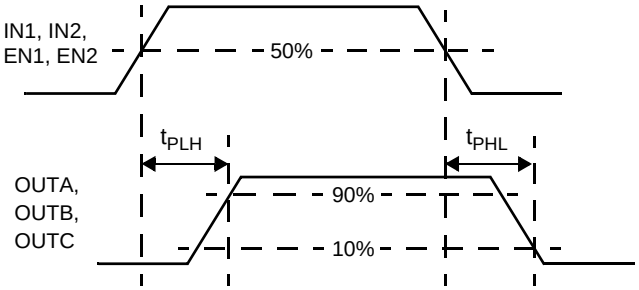


Figure 4. t_{PLH}, t_{PHL}, and t_{PZH} Timing

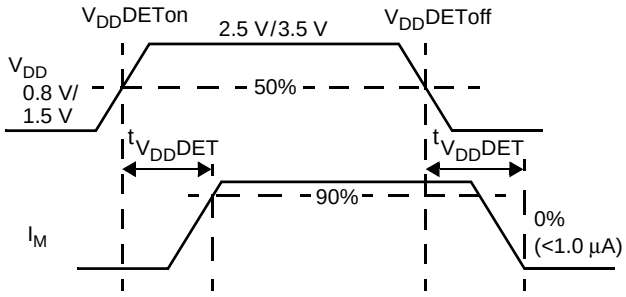


Figure 5. Low-Voltage Detection Timing

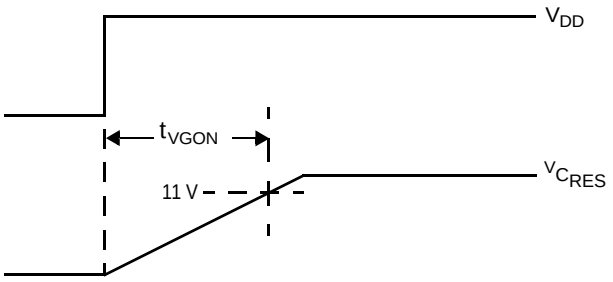


Figure 6. Charge Pump Timing

Table 5. Truth Table

INPUT				OUTPUT		
IN1	**IN2**	**EN1**	**EN2**	**OUTA**	**OUTB**	**OUTC**
SHUTDOWN MODE						
X	X	L	L	Z	Z	Z
CHANNEL 1 (A–B) DRIVING MODE						
H	H	H	L	L	L	Z
H	L	H	L	H	L	Z
L	H	H	L	L	H	Z
L	L	H	L	Z	Z	Z
CHANNEL 2 (B–C) DRIVING MODE						
H	H	L	H	Z	L	L
H	L	L	H	Z	H	L
L	H	L	H	Z	L	H
L	L	L	H	Z	Z	Z
HALF-BRIDGE (C) DRIVING MODE						
H	H	H	H	Z	Z	Z
H	L	H	H	Z	Z	H
L	H	H	H	Z	Z	L
L	L	H	H	Z	Z	Z

H = High.
L = Low.
Z = High impedance.
X = Don’t care.

FUNCTIONAL DESCRIPTION

INTRODUCTION

The 17517 is a triple totem-pole output H-Bridge power IC designed to drive small dc motors used in portable electronics. The 17517 can operate efficiently with supply voltages as low as 2.0 V to as high as 6.8 V, and provide continuos motor drive currents of 1.0 A while handling peak currents up to 3.0 A. It is easily interfaced to low cost MCUs via parallel 3.0 V- or 5.0 V-compatible logic. The device can be pulse width modulated (PWM-ed) at up to 200 kHz. The 17517 can drive two motors in two directions one at a time; or it can drive one motor in two directions and one solenoid with synchronous rectification of freewheeling currents one at a time. Two-motor operation is accomplished by hooking one motor between OUTA and OUTB, and the other motor between OUTB and OUTC. Motor + solenoid operation is accomplished by hooking a motor between OUTA and OUTB and placing a solenoid between OUTC and GND. Table 5, Truth Table, page 8, describes the operating states versus the input conditions.

As shown in Figure 2, 17517 Simplified Internal Block Diagram, page 2, the 17517 is a monolithic triple totem-pole output bridge with built-in charge pump circuitry. Each of the six MOSFETs forming the triple totem-pole output has an $R_{DS(ON)}$ of ≤ 0.6 Ω (guaranteed by design). The IC has an integrated charge pump and level shifter (for gate drive voltages). Additionally, the IC has a built-in shoot-through current protection circuit and undervoltage lockout function. This IC has four operating modes: Forward, Reverse, Brake, and Tri-Stated (High Impedance).

FUNCTIONAL PIN DESCRIPTION

DRIVER OUTPUT (OUTA, OUTB, OUTC)

These pins provide the connection to the internal power MOSFET triple-totem-pole H-bridge of the IC.

GROUND (GND)

Power and signal ground pin.

CHARGE PUMP OUTPUT CAPACITOR (CRES)

This pin provides the connection for the external reservoir capacitor (output of the charge pump). Alternatively, this pin can also be used as an input to supply gate-drive voltage from an external source via a series current-limiting resistor.

The voltage at the CRES pin will be approximately three times the V_{DD} voltage, as the internal charge pump utilizes a voltage tripler circuit. The V_{DDRES} voltage is used by the IC to supply gate drive for the internal power MOSFETs.

MOTOR DRIVE POWER SUPPLY (VM)

The two VM pins carry the main supply voltage and current into the power sections of the IC. This supply then becomes controlled and/or modulated by the IC as it delivers the power to the load attached between OUTA and OUTB.

The VM pins must be connected together on the printed circuit board with as short as possible traces offering as low impedance as possible between pins.

CONTROL SIGNAL INPUT AND ENABLE CONTROL SIGNAL INPUT (IN1, IN1, EN1, EN2)

These pins are input control pins used to control the outputs. These pins are 3.0 V/5.0 V CMOS-compatible inputs with hysteresis. These pins work together to control OUTA, OUTB, and OUTC (refer to Table 5, Truth Table).

CHARGE PUMP BUCKET CAPACITOR (C1L, C1H, C2L, C2H)

These two pairs of pins, the C1L and C1H and the C2L and C2H, connect to the external bucket capacitors required by the internal charge pump. The typical value for the bucket capacitors is 0.1 µF.

CONTROL CIRCUIT POWER SUPPLY (VDD)

This pin carries the logic supply voltage and current into the logic sections of the IC. V_{DD} has an undervoltage threshold. If the supply voltage drops below the undervoltage threshold, the output power stage switches to a tri-state condition. When the supply voltage returns to a level that is above the threshold, the power stage automatically resumes normal operation according to the established condition of the input pins.

TYPICAL APPLICATIONS

INTRODUCTION

Figure 7 shows a typical application for the 17517. When applying the gate voltage to the C_{RES} pin from an external source, be sure to connect it via a resistor equal to, or greater than, $R_G = {}^{V}C_{RES}/0.02\ \Omega$.

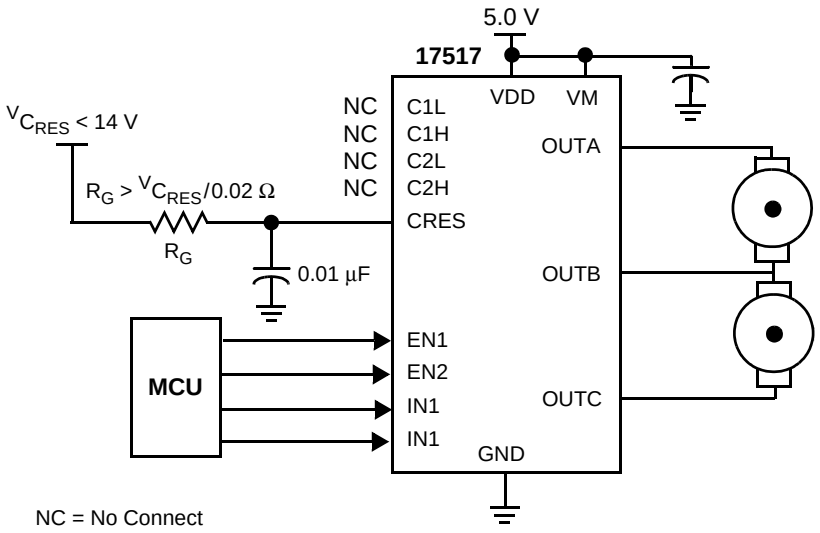


Figure 7. 17517 Typical Application Diagram

CEMF SNUBBING TECHNIQUES

Care must be taken to protect the IC from potentially damaging CEMF spikes induced when commutating currents in inductive loads. Typical practice is to provide snubbing of voltage transients by placing a capacitor or zener at the supply pin (VM) (see Figure 8).

PCB LAYOUT

When designing the printed circuit board (pcb), connect sufficient capacitance between power supply and ground pins to ensure proper filtering from transients. For all high-current paths, use wide copper traces and shortest possible distances.

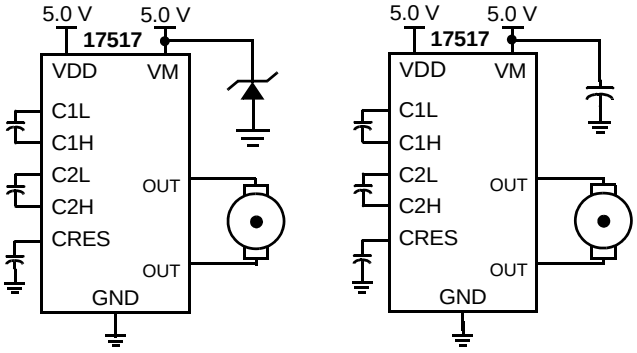
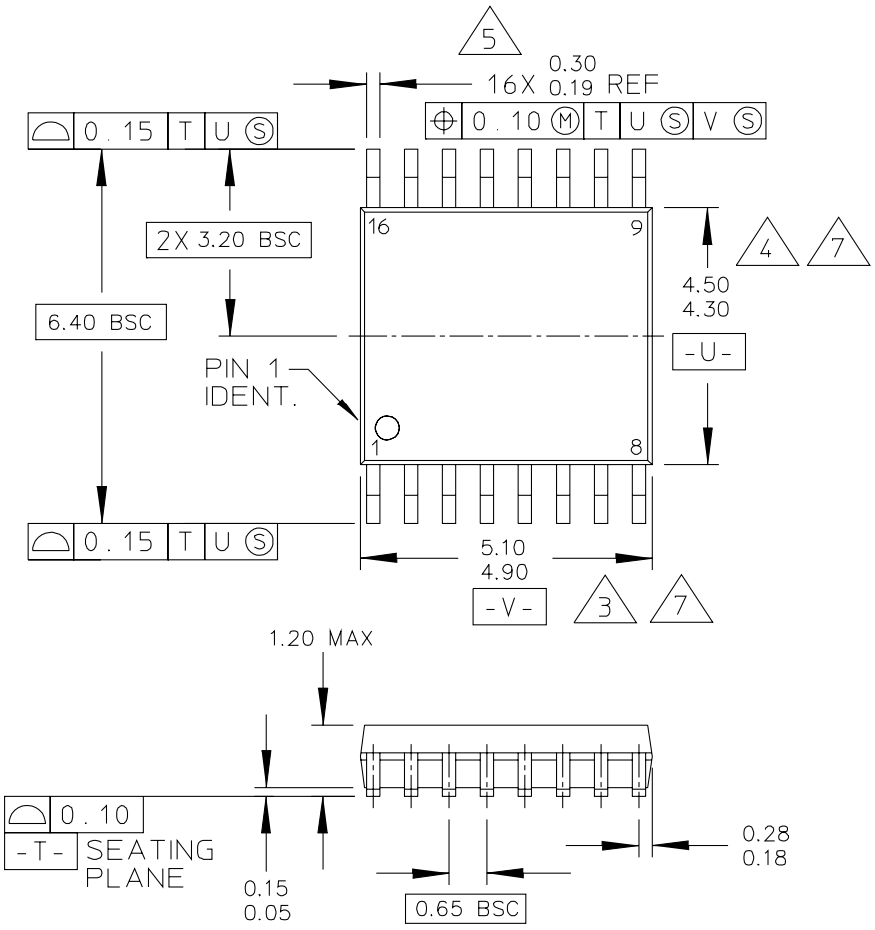


Figure 8. CEMF Snubbing Techniques

PACKAGING

PACKAGE DIMENSIONS

For the most current package revision, visit **www.freescale.com** and perform a keyword search using the “98A” listed below.



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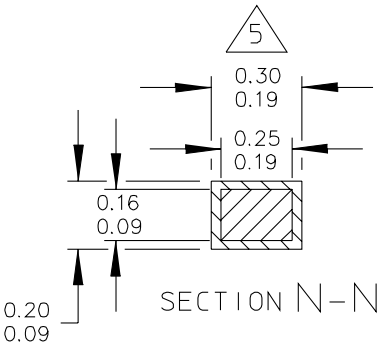

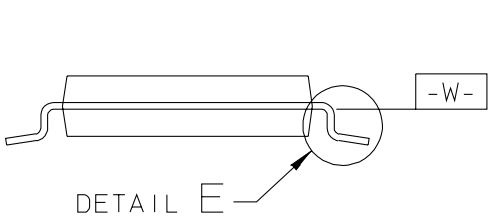

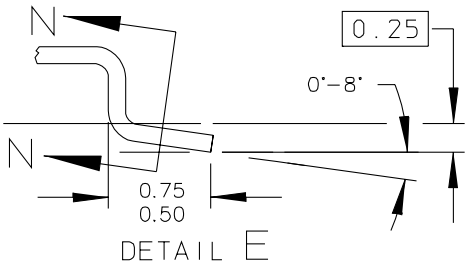

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	STANDARD: JEDEC	

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REVISION HISTORY

REVISION	DATE	DESCRIPTION OF CHANGES
2.0	7/2006	• Implemented Revision History page • Converted to Freescale format and updated to the prevailing form and style

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