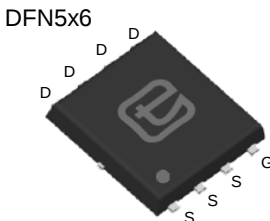
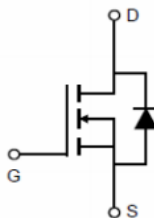




60V N-Channel DTMOS

Features ● Trench Power DTMOS Technology ● Low $R_{DS(ON)}$ ● Low Gate Charge ● Optimized for Fast-switching Applications Applications ● Synchronous Rectification in DC/DC and AC/DC Converters ● Isolated DC/DC Converters in Telecom and Industrial	Product Summary <table><tr><td>V_{DS}</td><td>60V</td></tr><tr><td>$R_{DS(ON)}$ (at $V_{GS}=10V$)</td><td>< 9mΩ</td></tr><tr><td>$R_{DS(ON)}$ (at $V_{GS}=4.5V$)</td><td>< 13.5mΩ</td></tr><tr><td>ID (at $V_{GS}=10V$)</td><td>60A</td></tr></table> 100% UIS Tested 	V_{DS}	60V	$R_{DS(ON)}$ (at $V_{GS}=10V$)	< 9mΩ	$R_{DS(ON)}$ (at $V_{GS}=4.5V$)	< 13.5mΩ	ID (at $V_{GS}=10V$)	60A
V_{DS}	60V								
$R_{DS(ON)}$ (at $V_{GS}=10V$)	< 9mΩ								
$R_{DS(ON)}$ (at $V_{GS}=4.5V$)	< 13.5mΩ								
ID (at $V_{GS}=10V$)	60A								
 									
Device	Package	Marking							
TSG12N06AT	DFN5×6	12N06AT							

Absolute Maximum Ratings $T_C = 25^{\circ}\text{C}$, unless otherwise noted				
Parameter		Symbol	Value	Unit
Drain-Source Voltage ($V_{GS} = 0\text{V}$)		V_{DSS}	60	V
Continuous Drain Current	$T_C = 25^{\circ}\text{C}$	I_D	60	A
	$T_C = 100^{\circ}\text{C}$		36	
Pulsed Drain Current (note1)		I_{DM}	240	A
Gate-Source Voltage		V_{GSS}	± 20	V
Single Pulse Avalanche Energy (note2)		E_{AS}	65	mJ
Avalanche Current (note1)		I_{AS}	36	A
Power Dissipation ($T_C = 25^{\circ}\text{C}$)		P_D	56.5	W
Operating Junction and Storage Temperature Range		T_J, T_{stg}	-55~+175	$^{\circ}\text{C}$

Thermal Resistance			
Parameter	Symbol	Value	Unit
Thermal Resistance, Junction-to-Case	R_{thJC}	1.7	$^\circ C/W$
Thermal Resistance, Junction-to-Ambient	R_{thJA}	50	



Specifications T _J = 25°C, unless otherwise noted						
Parameter	Symbol	Test Conditions	Value			Unit
			Min.	Typ.	Max.	
Static						
Drain-Source Breakdown Voltage	V _{(BR)DSS}	V _{GS} = 0V, I _D = 250μA	60	--	--	V
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} = 60V, V _{GS} = 0V, T _J = 25°C	--	--	1	μA
		V _{DS} = 60V, V _{GS} = 0V, T _J = 100°C	--	--	100	
Gate-Source Leakage	I _{GSS}	V _{GS} = ±20V	--	--	±100	nA
Gate-Source Threshold Voltage	V _{GS(th)}	V _{DS} = V _{GS} , I _D = 250μA	1.1	--	2.5	V
Drain-Source On-Resistance (Note3)	R _{DS(on)}	V _{GS} = 10V, I _D = 20A	--	6.5	9	mΩ
		V _{GS} = 4.5V, I _D = 20A	--	10.7	13.5	
Forward Transconductance (Note3)	g _{fs}	V _{DS} = 5V, I _D = 20A	--	85	--	S
Dynamic						
Input Capacitance	C _{iss}	V _{GS} = 0V, V _{DS} = 30V, f = 1.0MHz	--	2455	--	pF
Output Capacitance	C _{oss}		--	240	--	
Reverse Transfer Capacitance	C _{rss}		--	34	--	
Total Gate Charge	Q _g (10V)	V _{DD} = 30V, I _D = 20A, V _{GS} = 10V	--	45	--	nC
	Q _g (4.5V)		--	24	--	
Gate-Source Charge	Q _{gs}		--	6.8	--	
Gate-Drain Charge	Q _{gd}		--	11.5	--	
Turn-on Delay Time	t _{d(on)}	V _{DD} = 30V, I _D = 20A, R _G = 3Ω	--	8	--	ns
Turn-on Rise Time	t _r		--	3	--	
Turn-off Delay Time	t _{d(off)}		--	25	--	
Turn-off Fall Time	t _f		--	4	--	
Drain-Source Body Diode Characteristics						
Continuous Body Diode Current	I _S	T _C = 25°C	--	--	46	A
Pulsed Diode Forward Current	I _{SM}		--	--	138	
Body Diode Voltage	V _{SD}	T _J = 25°C, I _{SD} = 1A, V _{GS} = 0V	--	0.72	1	V
Reverse Recovery Time	t _{rr}	I _F = 20A, di _F /dt = 500A/μs	--	25	--	ns
Reverse Recovery Charge	Q _{rr}		--	110	--	nC

Notes

1. Repetitive Rating: Pulse Width limited by maximum junction temperature
2. $I_{AS} = 36A, V_{DD} = 50V, R_G = 25\Omega$, Starting $T_J = 25^{\circ}\text{C}$
3. Pulse Test: Pulse Width $\leq 300\mu s$, Duty Cycle $\leq 1\%$



Typical Characteristics $T_J = 25^\circ\text{C}$, unless otherwise noted

Figure 1. Output Characteristics

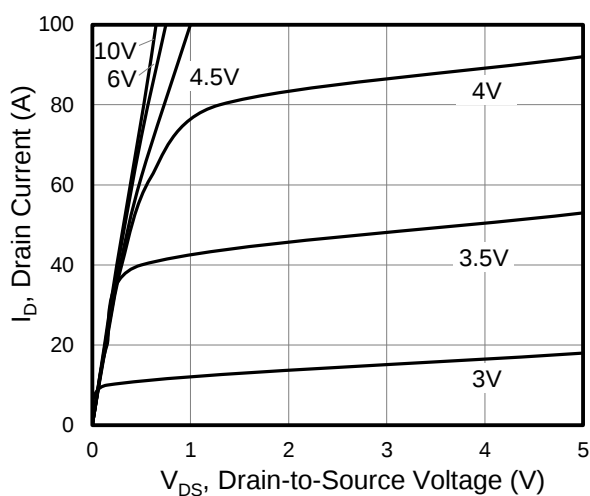


Figure 2. Transfer Characteristics

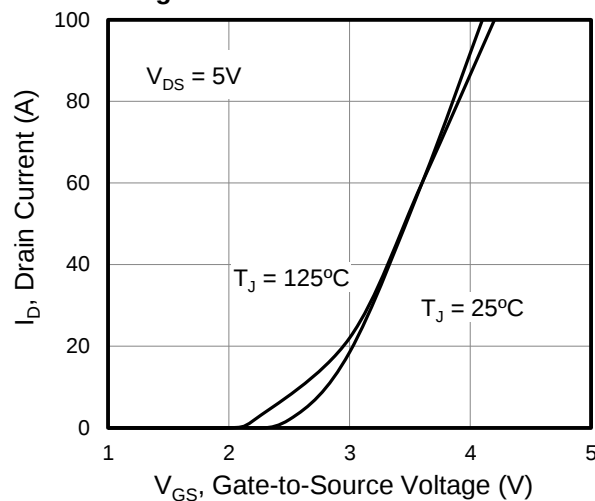


Figure 3. On-Resistance vs. Drain Current

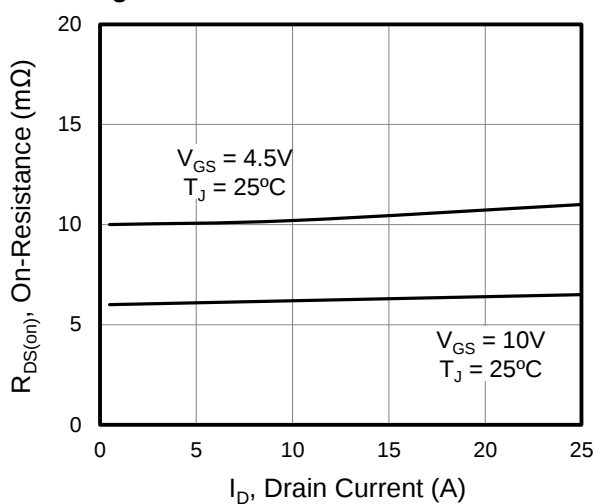


Figure 4. Capacitance

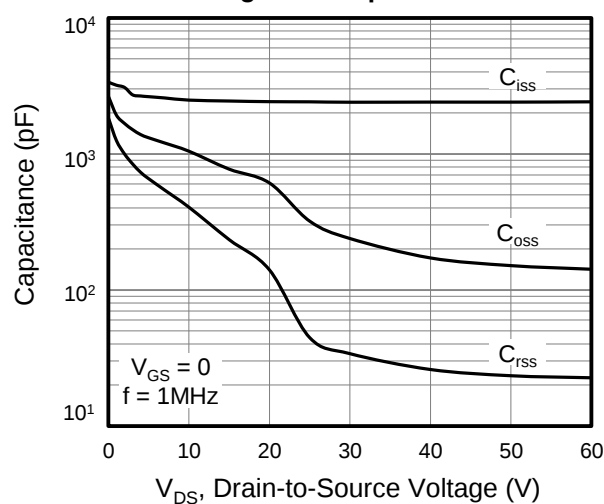


Figure 5. Gate Charge

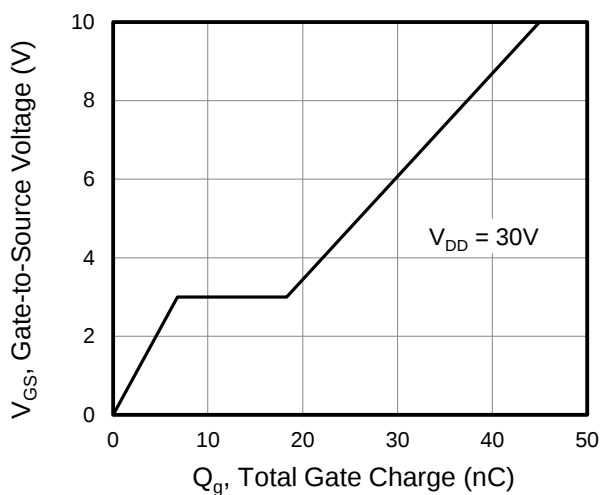
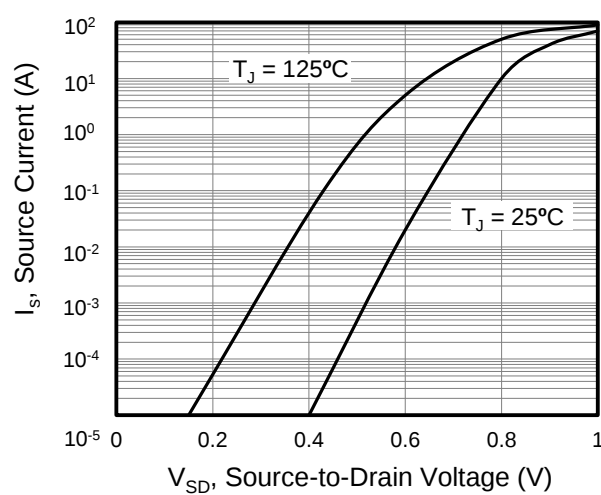


Figure 6. Body Diode Forward Voltage





Typical Characteristics $T_J = 25^\circ\text{C}$, unless otherwise noted

Figure 7. On-Resistance vs. Junction Temperature

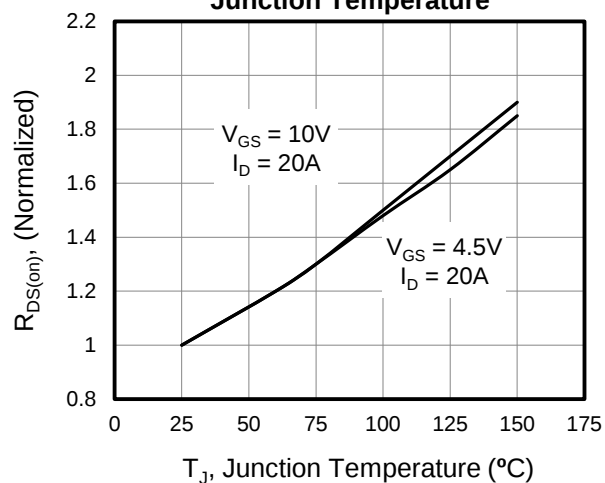


Figure 8. Threshold Voltage vs. Junction Temperature

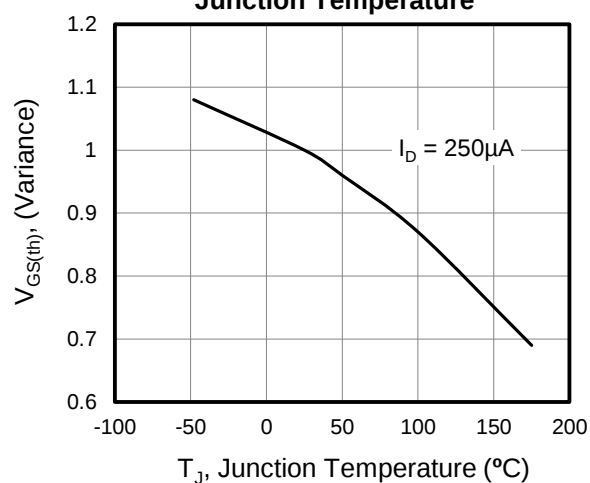


Figure 9. Transient Thermal Impedance

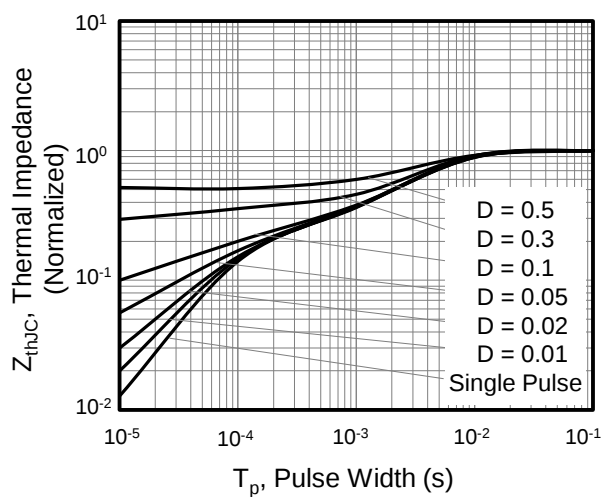


Figure 10. Safe operation area

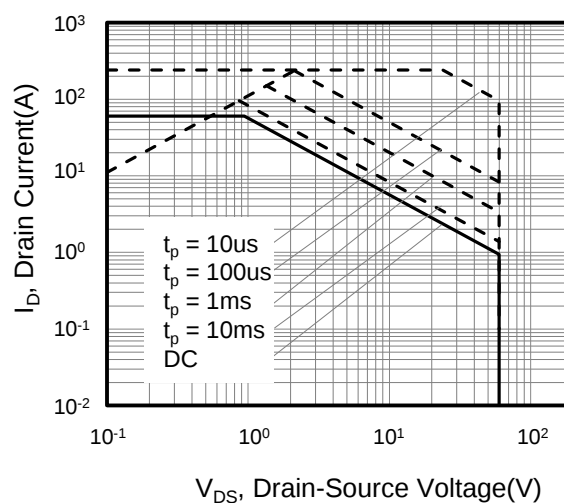




Figure A: Gate Charge Test Circuit and Waveform

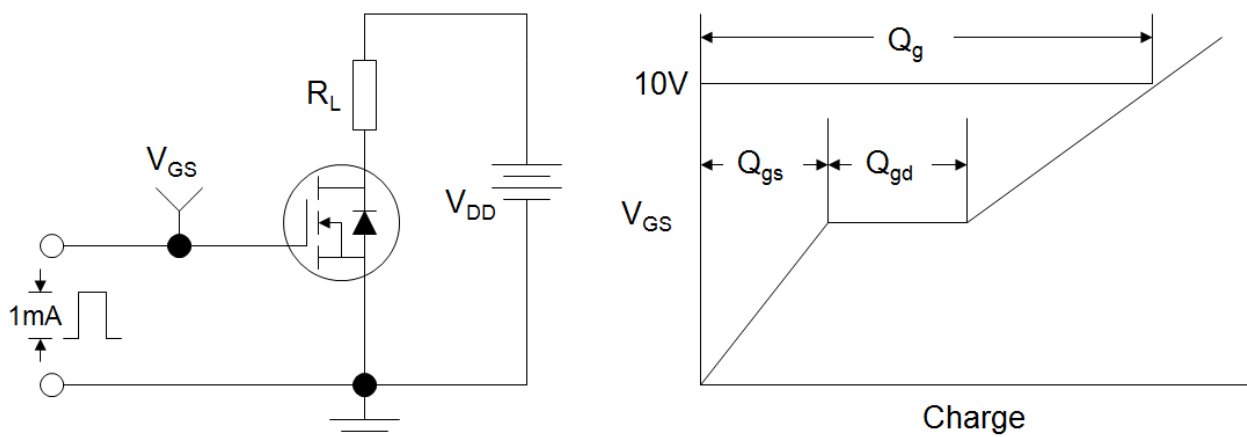


Figure B: Resistive Switching Test Circuit and Waveform

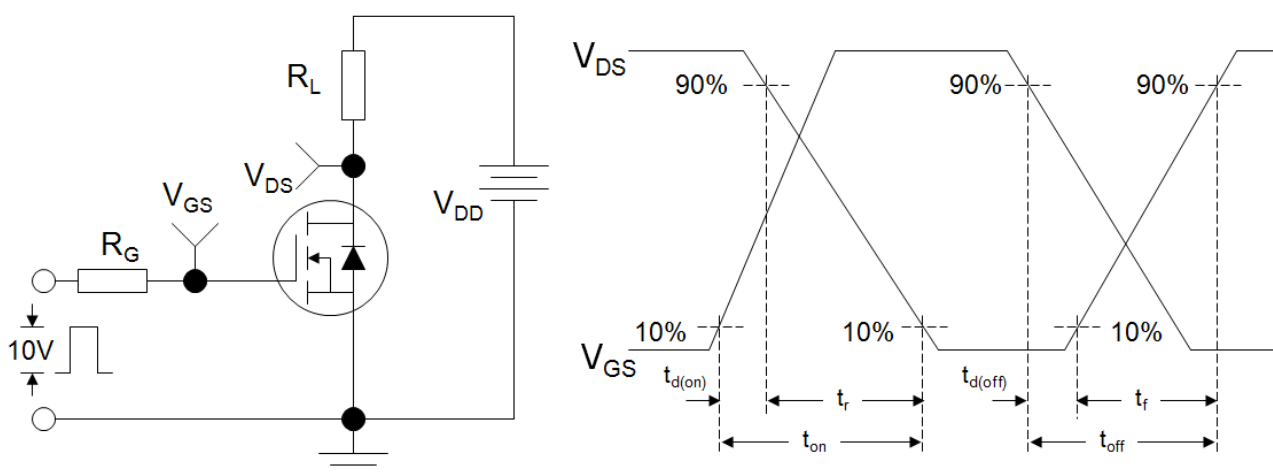
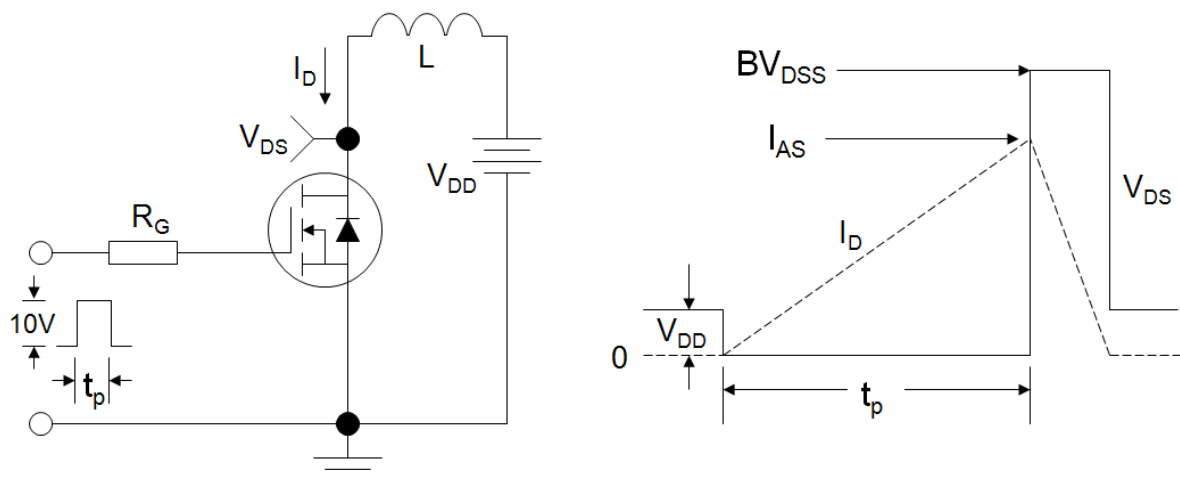
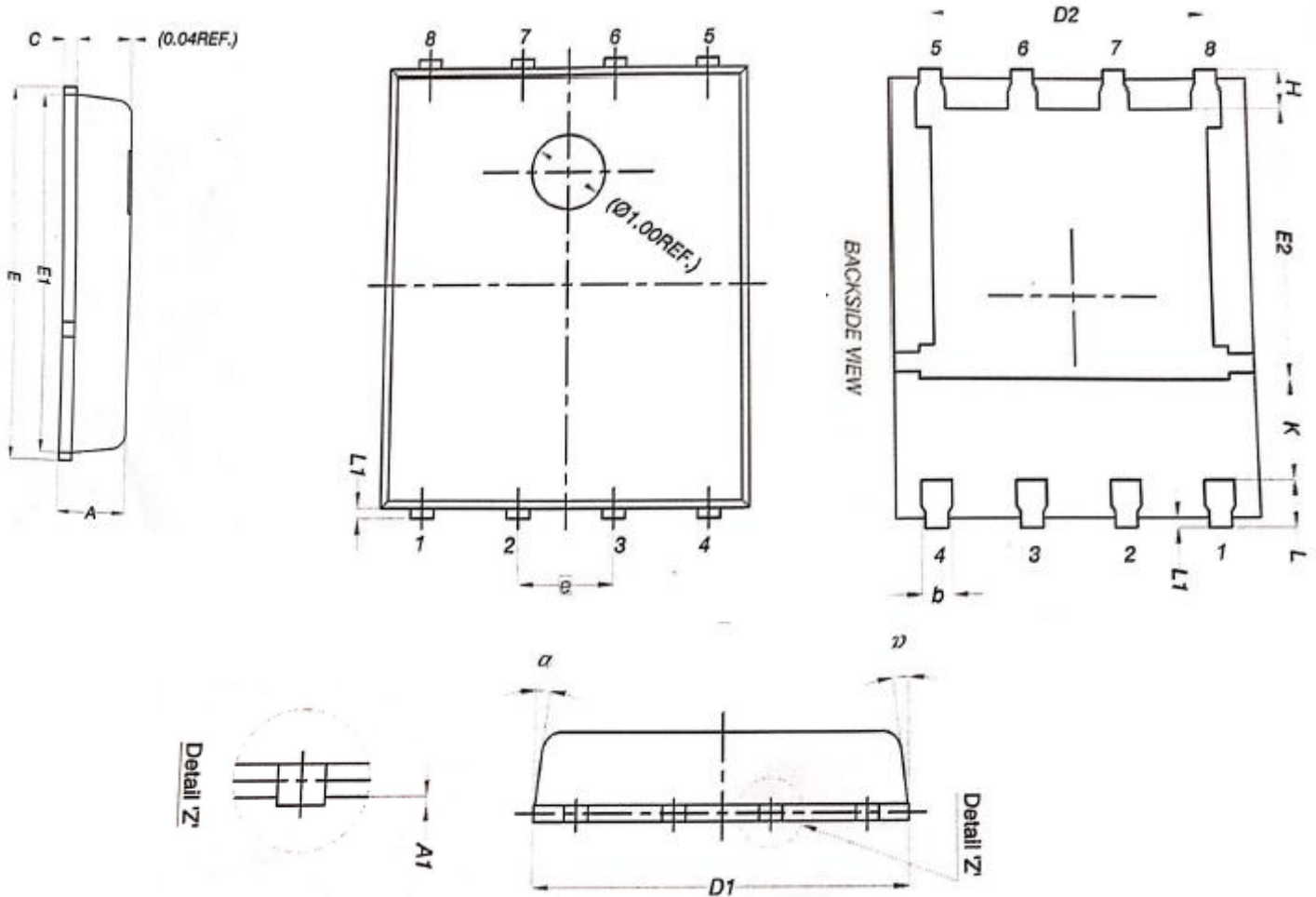


Figure C: Unclamped Inductive Switching Test Circuit and Waveform

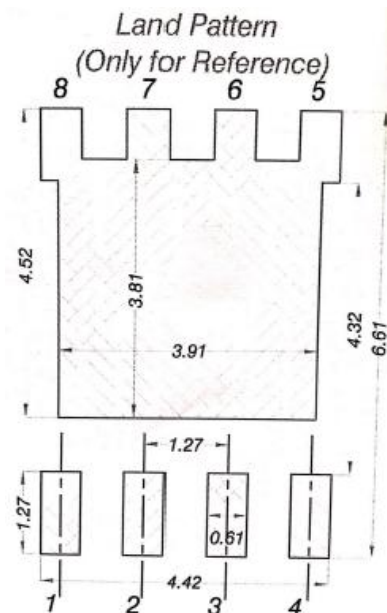




DFN5×6 PACKAGR OUTLINE



DIM.	MILLIMETERS		
	MIN.	NOM.	MAX.
A	0.90	1.00	1.10
A1	0	-	0.05
b	0.33	0.41	0.51
C	0.20	0.25	0.30
D1	4.80	4.90	5.00
D2	3.61	3.81	3.96
E	5.90	6.00	6.10
E1	5.70	5.75	5.80
E2	3.38	3.58	3.78
e	1.27 BSC		
H	0.41	0.51	0.61
K	1.10	-	-
L	0.51	0.61	0.71
L1	0.06	0.13	0.20
α	0°	-	12°





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