

STFH10N60M2

N-channel 600 V, 0.55 Ω typ., 7.5 A MDmesh™ M2 Power MOSFET in a TO-220FP wide creepage package

Datasheet - production data

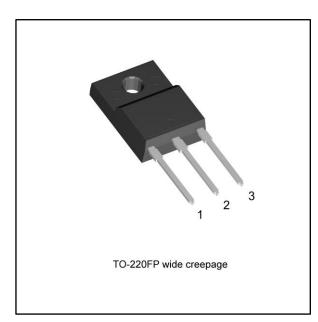
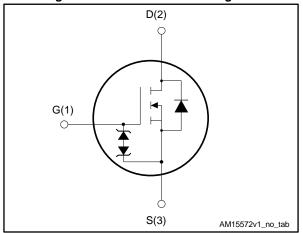


Figure 1: Internal schematic diagram



Features

Order code	V _{DS} @ T _{Jmax}	R _{DS(on)} max	ΙD
STFH10N60M2	650 V	0.60 Ω	7.5 A

- Extremely low gate charge
- Excellent output capacitance (Coss) profile
- 100% avalanche tested
- Zener-protected
- Wide distance of 4.25 mm between the pins

Applications

- Switching applications
- LLC converters, resonant converters

Description

This device is an N-channel Power MOSFET developed using MDmesh™ M2 technology. Thanks to its strip layout and an improved vertical structure, the device exhibits low on-resistance and optimized switching characteristics, rendering it suitable for the most demanding high efficiency converters.

The TO-220FP wide creepage package provides increased surface insulation for Power MOSFETs to prevent failure due to arcing, which can occur in polluted environments.

Table 1: Device summary

Order code	Marking	Package	Packing
STFH10N60M2	10N60M2	TO-220FP wide creepage	Tube

Contents STFH10N60M2

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STFH10N60M2 Electrical ratings

1 Electrical ratings

Table 2: Absolute maximum ratings

Symbol	Parameter	Value	Unit
V _G s	Gate-source voltage	± 25	V
I _D ⁽¹⁾	Drain current (continuous) at T _C = 25 °C	7.5	Α
I _D ⁽¹⁾	Drain current (continuous) at T _C = 100 °C	4.9	Α
I _{DM} (1)(2)	Drain current (pulsed)	30	Α
P _{TOT}	Total dissipation at $T_C = 25$ °C 25		W
dv/dt (3)	Peak diode recovery voltage slope 15		V/ns
dv/dt (4)	MOSFET dv/dt ruggedness	50	V/ns
V _{ISO}	Insulation withstand voltage (RMS) from all three leads to external heat sink (t = 1 s; TC = 25 °C)		V
T _{stg}	Storage temperature range	55 to 150	°C
Tj	Operating junction temperature range	- 55 to 150	

Notes:

Table 3: Thermal data

Symbol	Parameter	Value	Unit
R _{thj-case}	Thermal resistance junction-case	5	°C/W
R _{thj-amb}	Thermal resistance junction-ambient	62.5	°C/W

Table 4: Avalanche characteristics

Symbol	Parameter	Value	Unit
I _{AR}	Avalanche current, repetitive or not repetitive (pulse width limited by T_{jmax})	1.5	Α
Eas	Single pulse avalanche energy (starting T _j =25 °C, I _D = I _{AR} ; V _{DD} =50 V)	110	mJ

⁽¹⁾Limited by package.

⁽²⁾Pulse width limited by package.

 $^{^{(3)}}I_{SD} \leq 7.5$ A, di/dt ≤ 400 A/ $\mu s;$ VDS(peak) < V(BR)DSS, VDD = 400 V

 $^{^{(4)}}V_{DS} \le 480 \text{ V}$

Electrical characteristics STFH10N60M2

2 Electrical characteristics

(T_C = 25 °C unless otherwise specified)

Table 5: On /off states

Symbol	Parameter	Test conditions	Min.	Тур.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	$V_{GS} = 0 \text{ V}, I_D = 1 \text{ mA}$	600			V
	Zoro goto voltago droin	V _{GS} = 0 V, V _{DS} = 600 V			1	μΑ
IDSS	Zero gate voltage drain current	$V_{GS} = 0 \text{ V}, V_{DS} = 600 \text{ V},$ $T_{C}=125 \text{ °C}^{(1)}$			100	μΑ
I _{GSS}	Gate-body leakage current	$V_{DS} = 0 \text{ V}, V_{GS} = \pm 25 \text{ V}$			±10	μΑ
V _{GS(th)}	Gate threshold voltage	$V_{DS} = V_{GS}$, $I_D = 250 \mu A$	2	3	4	V
R _{DS(on)}	Static drain-source on- resistance	V _G S = 10 V, I _D = 3 A		0.55	0.60	Ω

Notes:

Table 6: Dynamic

Symbol	Parameter Test conditions		Min.	Тур.	Max.	Unit
Ciss	Input capacitance		-	400	-	pF
Coss	Output capacitance	V _{DS} = 100 V, f = 1 MHz,	-	22	-	pF
Crss	Reverse transfer capacitance	Ves = 0 V	-	0.84	-	pF
Coss	Equivalent output capacitance	V _{DS} = 0 to 480 V, V _{GS} = 0 V	-	83	-	pF
R _G	Intrinsic gate resistance	f = 1 MHz, I _D =0 A	-	6.4	-	Ω
Qg	Total gate charge	$V_{DD} = 480 \text{ V}, I_D = 7.5 \text{ A},$	-	13.5	-	nC
Qgs	Gate-source charge	V _{GS} = 0 to 10 V (see Figure 15: "Test circuit for	-	2.1	-	nC
Q_{gd}	Gate-drain charge	gate charge behavior")	-	7.2	-	nC

Notes:

 $^{^{(1)}}$ Defined by design, not subject to production test.

 $^{^{(1)}}C_{oss\ eq.}$ is defined as a constant equivalent capacitance giving the same charging time as C_{oss} when V_{DS} increases from 0 to 80% V_{DSS}

Table 7: Switching times

Symbol	Parameter	Test conditions	Min.	Тур.	Max.	Unit
t _{d(on)}	Turn-on delay time	$V_{DD} = 300 \text{ V}, I_D = 3.75 \text{ A},$	ı	8.8	1	ns
tr	Rise time	$R_G = 4.7 \Omega$, $V_{GS} = 10 V$ (see Figure 14: "Test circuit for	ı	8	ı	ns
t _{d(off)}	Turn-off delay time	resistive load switching times"	ı	32.5	ı	ns
t _f	Fall time	and Figure 19: "Switching time waveform")	-	13.2	-	ns

Table 8: Source drain diode

Symbol	Parameter	Test conditions	Min.	Тур.	Max.	Unit
I _{SD} ⁽¹⁾	Source-drain current		-		7.5	Α
I _{SDM} ⁽¹⁾⁽²⁾	Source-drain current (pulsed)		1		30	Α
V _{SD} ⁽³⁾	Forward on voltage	$I_{SD} = 7.5 \text{ A}, V_{GS} = 0 \text{ V}$	-		1.6	V
t _{rr}	Reverse recovery time	$I_{SD} = 7.5 \text{ A}, \text{ di/dt} = 100 \text{ A/}\mu\text{s}$	-	270		ns
Qrr	Reverse recovery charge	$V_{DD} = 60 \text{ V}$	-	2		μC
I _{RRM}	Reverse recovery current	(see Figure 16: "Test circuit for inductive load switching and diode recovery times")	-	14.4		Α
t _{rr}	Reverse recovery time	$I_{SD} = 7.5 \text{ A}, \text{ di/dt} = 100 \text{ A/}\mu\text{s}$	-	376		ns
Qrr	Reverse recovery charge	$V_{DD} = 60 \text{ V}, T_j = 150 ^{\circ}\text{C}$	-	2.8		μC
I _{RRM}	Reverse recovery current	(see Figure 16: "Test circuit for inductive load switching and diode recovery times")	-	15		А

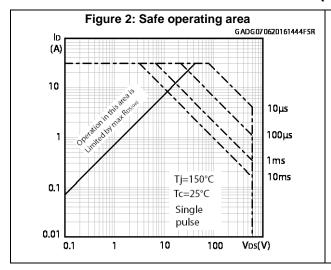
Notes:

⁽¹⁾Limited by package.

 $[\]ensuremath{^{(2)}}\mbox{Pulse}$ width limited by safe operating area.

 $^{^{(3)}}$ Pulsed: pulse duration = 300 μ s, duty cycle 1.5%.

2.1 Electrical characteristics (curves)



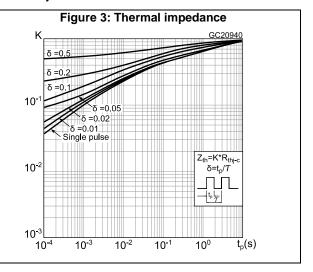
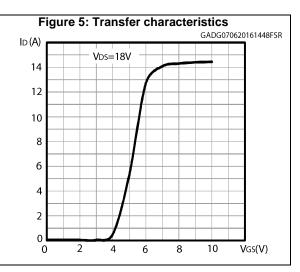
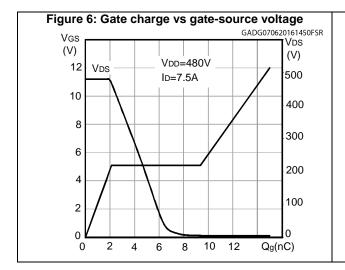
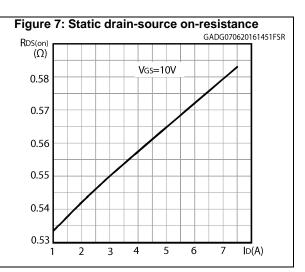


Figure 4: Output characteristics GADG070620161446FSR (A) VGS=7, 8, 9, 10V 14 12 10 8 6 5V 4 2 4V 0 10 15 20 VDS(V)







STFH10N60M2 Electrical characteristics

Figure 8: Capacitance variations

C (pF)

1000

10

10

Coss

Coss

Coss

Crss

O.1

O.1

1 1 10 100 VDS(V)

Figure 9: Normalized gate threshold voltage vs. temperature

VGS(th) GADG070620161458FSR

ID=250 μA

1.1

1.0

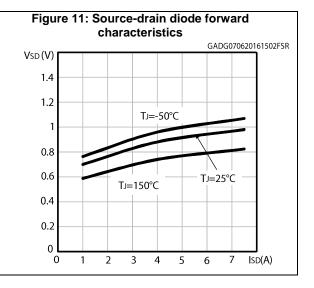
0.9

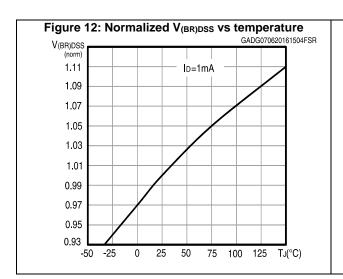
0.8

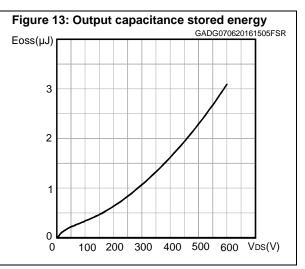
0.7

-50 -25 0 25 50 75 100 125 ΤJ(°C)

Figure 10: Normalized on-resistance vs temperature GADG070620161500FSR RDS(on) (narm) ID=3 A 2.5 2.3 2.1 1.9 1.7 1.5 1.3 1.1 0.9 0.7 25 50 75 100 125 TJ(°C)

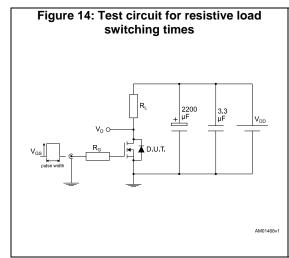






Test circuits STFH10N60M2

3 Test circuits



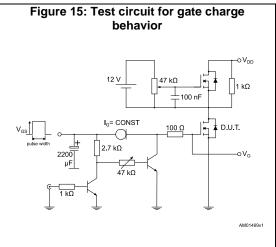
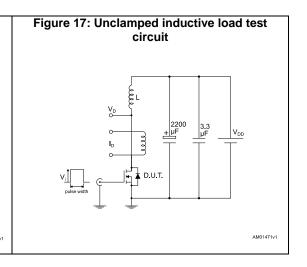
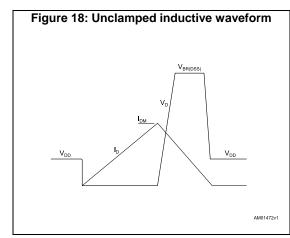
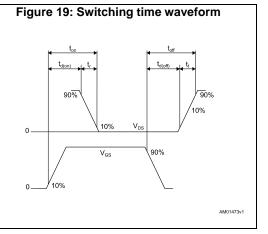


Figure 16: Test circuit for inductive load switching and diode recovery times







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4 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: **www.st.com**. ECOPACK® is an ST trademark.

4.1 TO-220FP wide creepage package information

В 57 D 7 G1 G Ε

Figure 20: TO-220FP wide creepage package outline

Table 9: TO-220FP wide creepage package mechanical data

Dim		mm	
Dim.	Min.	Тур.	Max.
Α	4.60	4.70	4.80
В	2.50	2.60	2.70
D	2.49	2.59	2.69
Е	0.46		0.59
F	0.76		0.89
F1	0.96		1.25
F2	1.11		1.40
G	8.40	8.50	8.60
G1	4.15	4.25	4.35
Н	10.90	11.00	11.10
L2	15.25	15.40	15.55
L3	28.70	29.00	29.30
L4	10.00	10.20	10.40
L5	2.55	2.70	2.85
L6	16.00	16.10	16.20
L7	9.05	9.15	9.25
Dia	3.00	3.10	3.20

STFH10N60M2 Revision history

5 Revision history

Table 10: Document revision history

Date	Revision	Changes
07-Jun-2016	1	First release.
16-Jun-2016	2	Document status promoted from preliminary data to production data. Minor text changes.
18-Aug-2016	3	Modified: title and R _{DS(on)} in cover page Modified: <i>Table 5: "On /off states"</i> and <i>Table 7: "Switching times"</i> Minor text changes
08-May-2017	4	Modified features on cover page. Modified Table 2: "Absolute maximum ratings" and Table 4: "Avalanche characteristics". Minor text changes.

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