Analog Front End for ADSL

AD6440

FEATURES

Complete Analog Front End for ADSL Modems
Part of ADI ADSL Chipset (AD20msp930)
Designed to ANSI T1.413/ETSI TR238/ITU G.adsl Performance
e.g., 6.1 Mbps Downstream Over 12K Ft.
Suitable for CO or CPE (ATU-C and ATU-R)
Includes Transmit and Receive Signal Paths:
DAC: 20 MSPS 14-Bit Current Output
ADC: 10 MSPS 12-Bit
PGA: –6 dB–30 dB of Gain with 1 dB Steps
Programmable Filters
8-Bit Auxiliary DAC for Timing Recovery
Interface to 3.3 V or 5 V Digital Logic
Low Power Consumption (525 mW)
80-Lead MQFP
–40°C to +85°C Operation

GENERAL DESCRIPTION

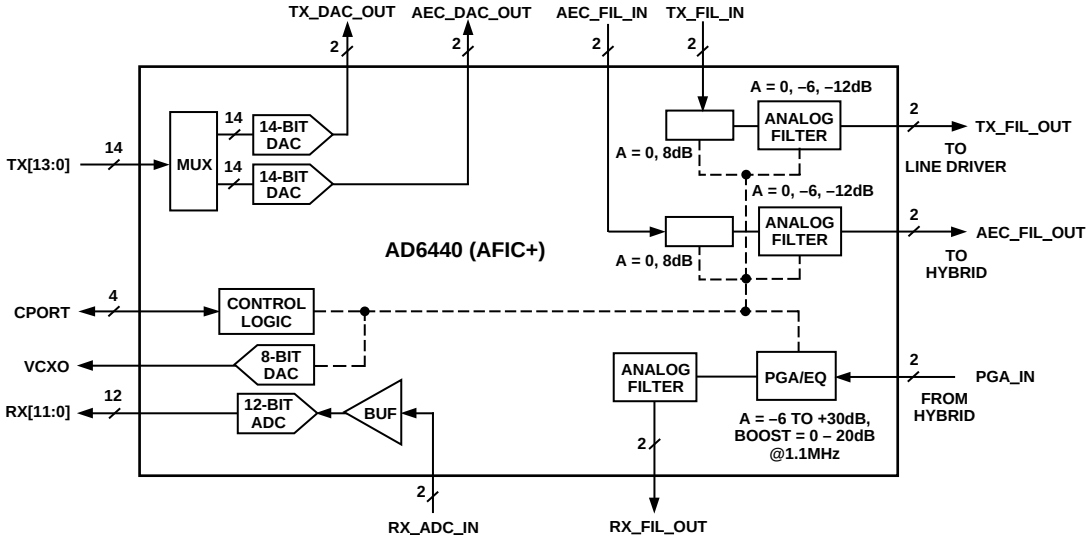
The AD6440 is a complete analog front end IC (AD6440) for ADSL systems. Although part of the Analog Devices DMT chipset, it is suitable for use with digital implementations from other suppliers.

As part of the AD20msp930 chipset, it complements the AD6449; together with the line driver and an external filter, they make a complete ADSL datapump, designed to comply with ANSI and ETSI standards for DMT-based ADSL.

The AD6440 includes both transmit and receive paths. These include the DAC (up to 20 MSPS, allowing for oversampling of the downstream transmit signal), ADC (up to 10 MSPS), low noise PGA and filters. The filters are software configurable for both the CO and RT modes. There is an 8-bit auxiliary DAC (e.g., for timing recovery).

The AD6440 has been designed to be versatile, and most blocks can be used or externally bypassed.

FUNCTIONAL BLOCK DIAGRAM



REV. 0

One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106, U.S.A.
Tel: 781/329-4700 World Wide Web Site: http://www.analog.com
Fax: 781/326-8703

AD6440–SPECIFICATIONS

Parameter	Min	Typ	Max	Units	Notes
TRANSMIT AND AEC CHANNELS					
THD (Co Mode)		76		dB	Sine Wave @ 400 kHz DAC CK = 17.66 MHz Output Voltage = 5 V ppd To 5th Harmonic
SNR (Co Mode)		83.5		dB	Sine Wave @ 400 kHz Bandlimited at 1.1 MHz DAC CK = 17.66 MHz Output Voltage = 5 V ppd
THD (Rt Mode)		77		dB	Sine Wave @ 30 kHz DAC CK = 17.66 MHz Output Voltage = 5 V ppd To 5th Harmonic
SNR (Rt Mode)		88		dB	Sine Wave @ 400 kHz Bandlimited at 138 kHz DAC CK = 17.66 MHz Output Voltage = 5 V ppd
DAC					
Resolution		14		Bits	
Linearity		11.5		Bits	
SNR		12.5		Bits	
Max Sample Rate	17.664			MHz	
Data Format					Straight Binary
Output Compliance Range		±1.0		V ppd	I_{FS} = 10 mA
8 dB Gain Stage/LP Filter					
Input Impedance		7.2 k‖2 pF		Ω	±30% Differential
Filter Response					4th Order Butterworth Load Impedance 10 kΩ, 15 pF into 2.3 V
Output Voltage Range		5.0		V ppd	
Gain Variation		±0.5		dB	@ 400 kHz for 0 dB, –6 dB, and –12 dB Attenuation
CO Mode					
3 dB Frequency		2.5		MHz	±20%
Passband		1.1		MHz	
Passband Ripple		±0.5		dB	Relative to 400 kHz
RT Mode					
3 dB Frequency		195		kHz	±15%
Passband		138		kHz	
Passband Ripple		±0.5		dB	Relative to 400 kHz
ISDN Mode					
3 dB Frequency		390		kHz	±20%
Passband		138–276		kHz	
Passband Ripple		±0.5		dB	
RECEIVE CHANNEL					
THD		74		dB	Sine Wave @ 400 kHz, Bandlimited at 1.1 MHz,
SNR		75		dB	PGA Gain = 18 dB, ADC CK = 8.832 MHz,
					Output Voltage = 5 V ppd
Input Impedance		20 k‖2 pF		Ω	±30% Single-Ended, PGA Gain ≥ 6 dB (Setting ≥ 100000)
		13 k‖C		Ω	±30% Single-Ended, 0 ≤ PGA Gain ≤ 6 dB (011000 to 011111)
		(13 k + 13 k‖C)		Ω	±30% Single-Ended, –6 ≤ PGA Gain ≤ 0 dB (010000 to 010111) hfbsel = 0xx; C = 25 pF hfbsel = 100; C = 35 pF hfbsel = 101; C = 40 pF hfbsel = 110; C = 60 pF hfbsel = 111; C = 90 pF

Parameter	Min	Typ	Max	Units	Notes
RECEIVE CHANNEL (Continued)					
Input Referred Noise		15		nV/√Hz	PGA Gain = 30 dB, hfbsel = 0xx
Input Voltage Range			5	V ppd	
PGA					
Gain Range		–6 to +30		dB	See Table I
Gain Step Error		±0.25		dB	@ 400 kHz
AAE					
Gain @ 1.1 MHz		0–20		dB	See Table VI
Gain Accuracy @ 1.1 MHz		±2		dB	(PGA Gain ≥ 6 dB, Setting ≥ 011000)
Receive Filter					4th Order Butterworth
					Load Impedance 20K, 15 pF into 2.5 Volts
Output Voltage Range			5	V ppd	
3 dB Frequency		2.5		MHz	±20%
Passband		1.1		MHz	
Passband Ripple		±0.5		dB	
PGA IN to RX_FIL OUT					
Absolute Gain Error		±1		dB	@ 400 kHz, (PGA Setting ≥ 011000)
ADC Buffer					
Input Impedance		40k		Ω	±30% Differential
Gain Error		±0.25		dB	
ADC					
Resolution		12		Bit	
Max Sampling Rate	8.832			MHz	
Data Format					Straight Binary
CONTROL					
Timing Recovery DAC					
Resolution		8		Bit	Monotonic
Max Sample Rate	4			kHz	
Output: Low (SEL5V = 0)		0.5		V	Source 1 mA max/Sink
					100 µA max
Output: Low (SEL5V = 1)		0.5		V	Source 1 mA max/Sink
					100 µA max
Output: High (SEL5V = 0)		3		V	Source 1 mA max/Sink
					100 µA max
Output: High (SEL5V = 1)		4.4		V	Source 1 mA max/Sink
					100 µA max
Data Format					Straight Binary
Output Impedance		100		Ω	
DIGITAL INTERFACE					
Input Levels					3.3 V or 5 V Compatible
Output Levels					3.3 V or 5 V Compatible
Serial Interface					
Max Clock Rate	20			MHz	
ELECTRICAL					
Analog Power Supply (AVDD)	4.75	5.0	5.25	V	
3 V Digital Power Supply (DVDD_3)	3.00	3.3	3.6	V	
5 V Digital Power Supply (DVDD_5)	4.50	5.0	5.50	V	
IDVDD 5 V		13		mA	
IDVDD 3 V		0.5		mA	
IAVDD		117		mA	I_{FS} = 10 mA (With Analog Echo Path On)
		92		mA	I_{FS} = 10 mA*
Power Consumption (Normal)		650		mW	I_{FS} = 10 mA (With Analog Echo Path On)
		525		mW	I_{FS} = 10 mA*
Power Consumption (Low Power)		240		mW	

NOTES
*Assumes AEC path powered down (see Table V).
Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS*

Supply Voltage . . . . . –0.3 V to +6.0 V
Input Voltage . . . . . –0.5 V to V_{DD} + 0.5 V
Output Voltage Swing . . . . . –0.5 V to V_{DD} + 0.5 V
Operating Temperature Range (Ambient) . . . –40°C to +85°C
Storage Temperature Range . . . . . –65°C to +150°C
Lead Temperature (5 sec) MQFP . . . . . +280°C

*Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only; functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

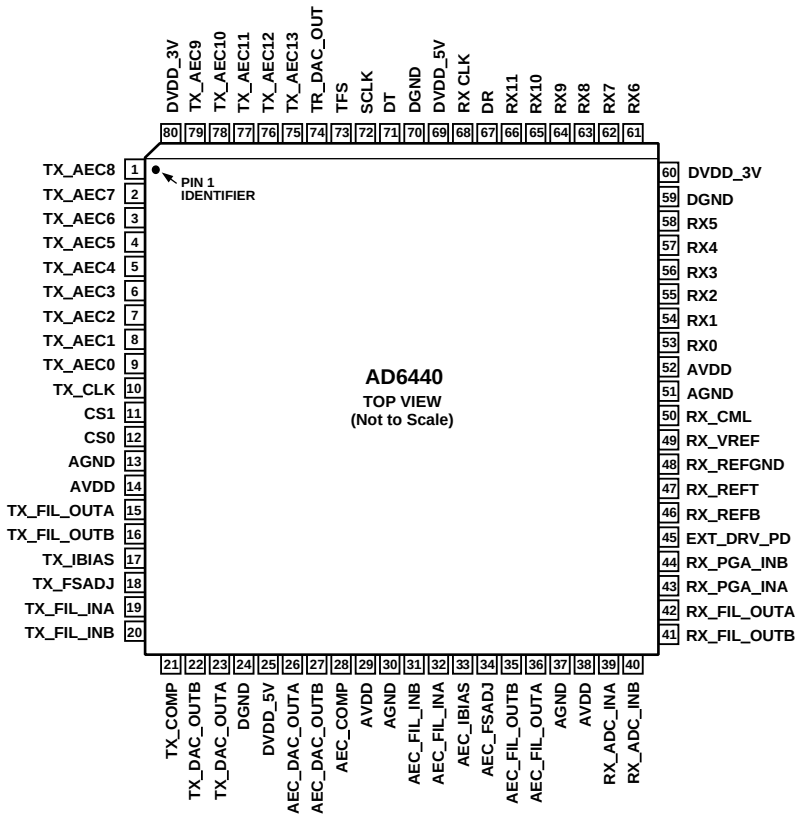
ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option
AD6440	–40°C to +85°C	Plastic Quad Flatpack	S-80A

CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the AD6440 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

PIN CONFIGURATION



PIN FUNCTION DESCRIPTIONS

Pin Name	Pin #	Description
TX_AEC[13:0]	1–9, 75–79	Digital Data to Tx DAC and AEC DAC.
TX_CLK	10	Clock Signal Used to Validate Transmit Data.
CS[1:0]	11, 12	Defines Chip Address.
AGND	13, 30, 37, 51	Analog Ground.
AVDD	14, 29, 38, 52	+5 V Analog Supply.
TX_FIL_OUT[A,B]	15, 16	Differential Output from Transmit LPF.
TX_IBIAS, TX_COMP	17, 21	Decoupling Pins for Internal Nodes.
TX_FSADJ	18	Resistor to AGND.
TX_FIL_IN[A,B]	19, 20	Differential Input to Transmit LPF.
TX_DAC_OUT[A,B]	23, 22	Complementary Current Outputs.
DGND	24, 59, 70	Digital Ground.
DVDD_5V	25, 69	+5 V Digital Supply for Converters. Must Be Connected to 5 V.
AEC_DAC_OUT[A,B]	26, 27	Complimentary Current Outputs.
AEC_FIL_IN[A,B]	32, 31	Differential Input to Echo LPF.
AEC_IBIAS, AEC_COMP	33, 28	Decoupling Pins for Internal Nodes.
AEC_FSADJ	34	Resistor to AGND.
AEC_FIL_OUT[A,B]	36, 35	Differential Output from Echo LPF.
RX_ADC_IN[A,B]	39, 40	Differential Input to ADC.
RX_FIL_OUT [B,A]	41, 42	Differential Output of Rx LPF Filter.
RX_PGA_IN[A,B]	43, 44	Differential Input to PGA.
EXT_DRV_PD	45	Test Pin.
RX_REFB, RX_REFT	46, 47	Decoupling Pins for ADC Reference.
RX_REFGND	48	External Voltage Reference Ground.
RX_VREF	49	External Voltage Reference.
RX_CML	50	Common-Mode Level.
RX[11:0]	53–58, 61–66	Digital Output (Receive) Data from ADC.
DVDD_3V	60, 80	Digital Supply for Interface. Can Be Connected to 3.3 V or 5 V to Suit Different Digital Circuitry.
DR	67	Serial Data Output. Used to Read Data Written to Registers.
RX CLK	68	Clock Input Qualifying ADC Data.
DT	71	Serial Data Input to Timing Recovery DAC.
SCLK	72	Clock for Timing Recovery DAC Serial Data.
TFS	73	Frame Sync for Timing Recovery DAC Data.
TR_DAC_OUT	74	Voltage Output from Timing Recovery DAC.

CIRCUIT DESCRIPTION

GENERAL

The AD6440 is designed as the analog front end for the AD20msp930 chipset or other ADSL systems. The AFIC contains programmable filters that make it suitable for both ATU-C and ATU-R modem applications. Many of the internal circuits of the AD6440 can be programmed or bypassed, making it a versatile codec that can be used in other ADSL applications or instrumentation and control systems.

There are five major sections to the AD6440. The transmit channel, which contains a 14-bit DAC and a fourth order reconstruction filter. There is an analog echo cancellation path for Category II ADSL, which is a duplicate of the transmit path. The receive channel, which includes a PGA with 36 dB of dynamic range, an adaptive analog equalizer, a fourth order antialiasing filter and a 12-bit, 10 MSPS ADC. Auxiliary and support circuitry that consists of an 8-bit DAC used for timing recovery and finally, there is the interface and control logic.

The AD6440 core runs from a single 5 V supply. The digital interface circuitry can run from either a 3.3 V or 5 V supply. All the analog input and output signals are processed in a fully differential mode. This affords greater immunity to externally coupled noise as well as greater signal swings throughout the signal path.

TRANSMIT/AEC CHANNEL

The data is received from the digital section (e.g., the AD6449) in parallel format. The data is then demultiplexed and passed to the corresponding D-to-A converter. The output from either DAC is available externally in complementary voltage. Typically, it will then be connected to a 4th order Butterworth active low-pass filter for on-chip reconstruction of the signal. A programmable gain stage is provided prior to the LPF to improve signal to noise ratio at the output of the channel. The filter and gain stage can be bypassed if a different filter is required (e.g., to use the AD6440 in a nonstandard application).

DAC Output

The DAC is a 14-bit differential output current DAC. The digital coding is straight binary. When the digital inputs are all 1s, I_{OUTA} is at full scale. The value of the outputs are complimentary (i.e., when I_{OUTA} is at full scale, the current from I_{OUTB} is zero). The current outputs are nominally set to 10 mA full-scale. The full-scale output current of the DAC is set through an external resistor. The relationship is:

$$I_{OUT\_full\text{-}scale} = 40/R_{SET}\ Amps$$

e.g., R_{SET} is 4 kΩ for a 10 mA full-scale output.

The current can be converted to a voltage by a grounded resistor. Ideally, this would be immediately converted to a large signal to preserve SNR. However, the output compliance of the DAC is 1.0 V. The resistors would be chosen to be <100 Ω for a 1.0 V output (2 V ppd) to stay within the compliance range.

Typically, a capacitor should be placed directly across the DAC outputs to band limit the signal into the 8 dB gain stage prior to the LPF. A value of 150 pF is recommended for a full-scale output current of 10 mA.

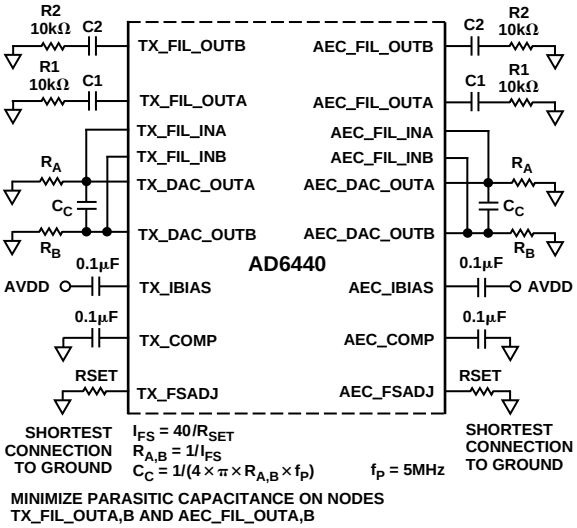


Figure 1. Typical Configuration: Transmit and AEC Path

Tx LPF

The AD6440 TxAEC filters can be switched between three corner frequencies, for use in CO mode or RT mode. For downstream operation (CO mode), the band ends at 1.1 MHz and the filter's 3 dB corner is set at 2.5 MHz. For upstream operation (RT mode), the filter could be set to 195 kHz, for use with POTS, with a flat response (±0.5 dB guaranteed) up to 138 kHz, or set to 390 kHz, for use with ISDN, with a flat response up to 276 kHz. The Tx and AEC filter selection is made by the mode select bits in Register 5. Each filter corner frequency and gain setting can be programmed independently of the serial interface.

The AFIC low-pass filters are designed to attenuate the images created at the DAC output due to the oversampling process. The amount of attenuation required is specified in the ANSI T1.413 specification in sections 6.12 and 7.12 for the ATU-C and ATU-R respectively. The AFIC filters are designed to provide course attenuation of 0 dB, –6 dB, or –12 dB to meet these requirements.

RECEIVE CHANNEL

The receive chain consists of a high impedance programmable gain amplifier with a dynamic range of 36 dB, an adaptive analog equalizer that is capable of providing up to 20 dB of high frequency boost at 1.1 MHz, a 4th order Butterworth active low-pass antialias filter, a high impedance, low distortion buffer that drives a 12-bit, 10 MSPS ADC.

Table I. Programmable Gain Amplifier Control

Pg 5	Pg 4	Pg 3	Pg 2	Pg 1	Pg 0	Relative Gain (dB)
0	0	x	x	x	x	–6
0	1	0	0	0	0	–6
0	1	0	0	0	1	–5
0	1	0	0	1	0	–4
0	1	0	0	1	1	–3
0	1	0	1	0	0	–2
0	1	0	1	0	1	–1
0	1	0	1	1	0	0
0	1	0	1	1	1	0
0	1	1	0	0	0	0
0	1	1	0	0	1	1
0	1	1	0	1	0	2
0	1	1	0	1	1	3
0	1	1	1	0	0	4
0	1	1	1	0	1	5
0	1	1	1	1	0	6
0	1	1	1	1	1	6
1	0	0	0	0	0	6
1	0	0	0	0	1	7
1	0	0	0	1	0	8
1	0	0	0	1	1	9
1	0	0	1	0	0	10
1	0	0	1	0	1	11
1	0	0	1	1	0	12
1	0	0	1	1	1	12
1	0	1	0	0	0	12
1	0	1	0	0	1	13
1	0	1	0	1	0	14
1	0	1	0	1	1	15
1	0	1	1	0	0	16
1	0	1	1	0	1	17
1	0	1	1	1	0	18
1	0	1	1	1	1	18
1	1	0	0	0	0	18
1	1	0	0	0	1	19
1	1	0	0	1	1	20
1	1	0	0	1	1	21
1	1	0	1	0	0	22
1	1	0	1	0	1	23
1	1	0	1	1	0	24
1	1	0	1	1	1	24
1	1	1	0	0	0	24
1	1	1	0	0	1	25
1	1	1	0	1	0	26
1	1	1	0	1	1	27
1	1	1	1	0	0	28
1	1	1	1	0	1	29
1	1	1	1	1	0	30
1	1	1	1	1	1	30

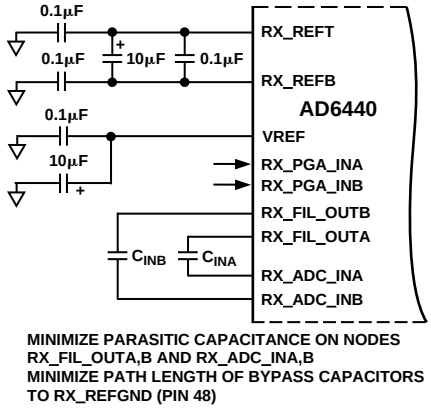


Figure 2. Typical Configuration: Receive Path

ANCILLARY AND SUPPORT SECTION

Auxiliary D/A

There is a 8-bit monotonic DAC, with an output buffer, that can be used for system control. Typically, this will be used with an external filter to drive a VCXO for timing recovery.

SERIAL INTERFACE

The AD6440 is designed to interface with a ADSP-2183 SPORT. The AD6440 serial interface contains four pins, a serial clock (SCLK), a transmit frame sync (TFS), a serial transmit data signal (DT), and a serial receive data signal (DR). The SCLK, TFS and DT are inputs to the AD6440, while the DR is an output. The four signals from the AD6440 connect directly to the respective signals on the ADSP-2183. In order for the ADSP-2183 to receive data from the AD6440, the TFS signal from the ADSP-2183 must be tied back around and connect to the RFS signal on the ADSP-2183.

Timing

The SCLK signal from the ADSP-2183 is a continuous clock with a maximum frequency of 20 MHz. In order for the ADSP-2183 to access the AD6440, it must pulse the TFS signal high for one SCLK. Then, on the successive 14 SCLK periods, the ADSP-2183 outputs the 14-bit code word out the DT pin. The TFS and DT signals are generated to be valid to the AFIC on the falling edge of the SCLK.

Programming Model

For a write to the AD6440, the code word is 14 bits and broken into 4-bit fields. For a read, the code word is six bits. During a read, the AD6440 receives the 6-bit code word, waits one SCLK period, and then drives the data out the DR pin on the subsequent eight SCLKs.

Table II. Code Word Decode

Bit Field	Range	Description
AD6440 Address	CS1–CS0	The DSP needs to access one of four AD6440s via the serial port. Therefore, this bit field is used to determine which of the four AD6440s is being accessed. The AD6440 address is tied directly to external pins.
Register Address	RS2–RS0	The DSP can access up to eight registers on the AD6440
Read/$\overline{\text{Write}}$ Bit	R/$\overline{\text{W}}$	This bit notifies the AD6440 whether a read (1) or write (0) cycle is being performed.
Date Byte	SD7–SD0	For a write cycle, this bit field contains the data for the specified register. For a read cycle, this bit field is ignored by the AD6440.

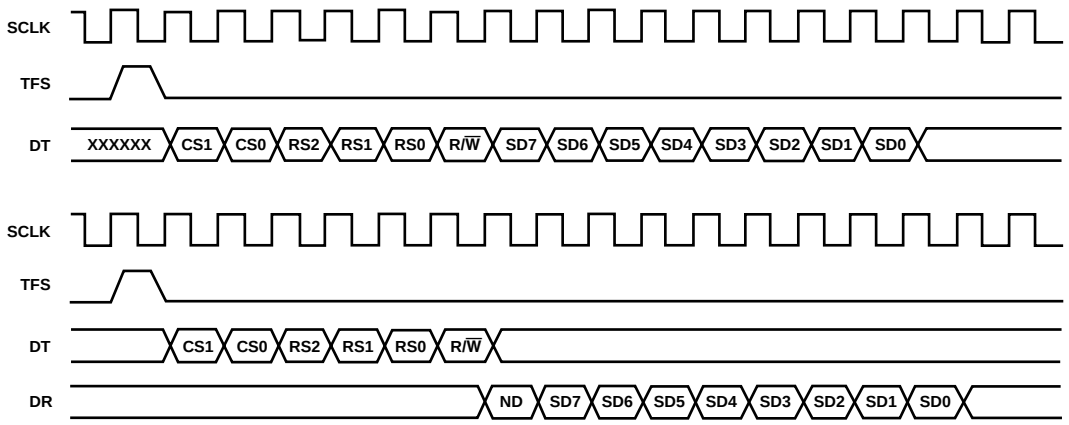


Figure 3. AD6440 Serial Port Timing

Table III. Serial Interface Data Format

CS [1:0]	RS [2:0]	R/$\overline{\text{W}}$	SD [7:0]
Determines if AFIC is selected. AD6440 address is tied directly to external pins.	Selects AFIC Register RS[2 1 0] 0 0 0 Reg0 0 0 1 Reg1 0 1 0 Reg2 0 1 1 Reg3 1 0 0 Reg4 1 0 1 Reg5 1 1 0 Reg6 1 1 1 Reg7	Read/$\overline{\text{Write}}$ 1 = Read 0 = Write	Data Byte Written (MSB First) SD7, MSB SD0, LSB

NOTE
All registers, except Reg0 Bit 5, will be preset to Logic 0 during chip power-up.

Table IV. AFIC Serial Port I/O

Pin Name	Definition	Type	Description
DT	Data Transmit	Input	Data Output from Host Processor (e.g., ADSP-2183)
TFS	Transmit Frame Sync	Input	Sync Output from Host Processor
SCLK	Serial Clock	Input	Clock Output from Host Processor
DR	Data Read	Output	Data Input to Host Processor (e.g., ADSP-2183)

Table V. Register Function

Register		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Reg0	Rx PGA Ctrl	tx8dB	aec8dB	pg5	pg4	pg3	pg2	pg1	pg0
Reg1	Power Mode	pdtxdac	pdaecdac	lpchip	pdrx	pdtx	pdaec	pdtrdac	pdext
Reg2	Aux DAC data	trd7	trd6	trd5	trd4	trd3	trd2	trd1	trd0
Reg3	Control 1	hfbsel2	hfbsel1	hfbsel0	pgtx1	pgtx0	pgaec1	pgaec0	low30
Reg4	AD6440 Rev	NC	NC	NC	NC	rev3	rev2	rev1	rev0
Reg5	Control 2	txm1	txm0	aecm1	aecm0	test53	low52	test51	trdac5v
Reg6	Test Mode	NC	NC	NC	NC	NC	NC	NC	NC
Reg7	Trim	NC	NC	T5	T4	T3	T2	T1	T0

Table VI. Register Bit Field Function

Name	Field	Description
tx8dB	Reg0 B[7]	Programmable Gain Tx Path, 0 = 0 dB, 1 = 8 dB
aec8dB	Reg0 B[6]	Programmable Gain AEC Path, 0 = 0 dB, 1 = 8 dB
pg[5:0]	Reg0 B[5:0]	Programmable Gain Amplifier Rx Gain Bits. Pg 0 LSB, Format Binary.
pdtxdac	Reg1 B[7]	Power-Down Tx DAC. Active High.
pdaecdac	Reg1 B[6]	Power-Down AEC DAC. Active High.
lpchip	Reg1 B[5]	Low Power Mode—Powers down all chip except ADC. Active High.
pdrx	Reg1 B[4]	Power-Down Receive PGA, AA Filter and ADC Buffer. Active High.
pdtx	Reg1 B[3]	Power-Down Tx Filter and 8 dB Gain Stage.
pdaec	Reg1 B[2]	Power-Down AEC Filter and 8 dB Gain Stage.
pdtrdac	Reg1 B[1]	Power-Down Timing Recovery DAC. Active High.
pdext	Reg1 B[0]	Power-Down External Driver. Active High. Pulls Pin 45 to within 100 Ω to ground.
trd[7:0]	Reg2	Timing Recover DAC Data. trd0 LSB, Data Format Binary.
hfbsel[2:0]	Reg3 B[7:5]	Programmable High Frequency Boost Rx Path. 0xx ≥ 0 dB, 2nd Order Butt 1 pF, –3 dB @ 3 MHz 100 ≥ 5.9 dB @ 1.1 MHz 101 ≥ 10.2 dB @ 1.1 MHz 110 ≥ 15.3 dB @ 1.1 MHz 111 ≥ 20.0 dB @ 1.1 MHz
pgtx[1:0]	Reg3 B[4:3]	Programmable Attenuator Tx Path. 00 ≥ 0 dB 01 ≥ –6 dB 1x ≥ –12 dB
pgaec[1:0]	Reg3 B[2:1]	Programmable Attenuator AEC Path. 00 ≥ 0 dB 01 ≥ –6 dB 1x ≥ –12 dB
rev[3:0]	Reg4 B[3:0]	Register value indicates chip revision, used only in Read mode.
txm[1:0]	Reg5 B[7:6]	Transmit Filter Corner Select. 00 ≥ fc = 195 kHz ± 15% 01 ≥ fc = 390 kHz ± 15% 10 ≥ fc = 1.25 MHz ± 20% 11 ≥ fc = 2.5 MHz ± 20%
aecm[1:0]	Reg5 B[5:4]	Transmit and AEC Filter Corner Select. 00 ≥ fc = 195 kHz ± 15% 01 ≥ fc = 390 kHz ± 15% 10 ≥ fc = 1.25 MHz ± 20% 11 ≥ fc = 2.5 MHz ± 20%
trdac5v	Reg5 B[0]	Sets Output Compliance Range for trdac. 0 = 3 V, 1 = 4.5 V.
trim	Reg7 B[5:0]	Used for Filter Trimming.

For normal operation:
must set Reg3, Bit 0 and Reg5, Bit 2 low,
must set Reg5, Bit 3 and Reg5, Bit 1 high only if Rx_CLK = 8.832 MHz, otherwise set Reg5, Bit 3 and Reg5, Bit 1 low.

TIMING

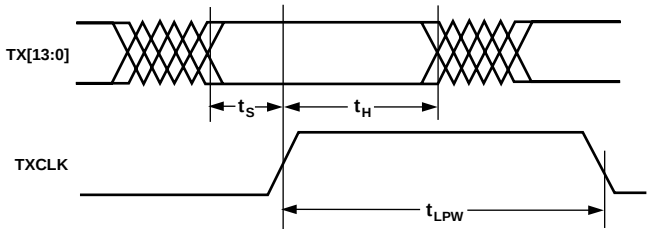


Figure 4. Transmit DAC Data Timing

Table VII. Transmit DAC Timing

	Min	Typ	Max	Unit
t_S	5			ns
t_H	5			ns
t_{LPW}	22		34	ns

RECEIVE INTERFACE

The analog input is sampled every rising edge of the ADC clock (RCVCK), with digital data (RX11:RX0) being valid on each falling edge of RCVCK. Due to the pipeline architecture used in the ADC, there is a three-cycle latency in the receive data as shown in the diagram.

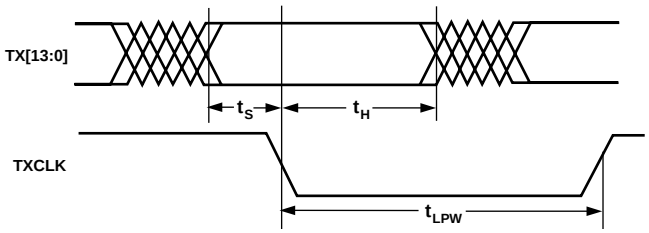


Figure 5. AEC DAC Data Timing

Table VIII. AEC DAC Timing

	Min	Typ	Max	Unit
t_S	5			ns
t_H	5			ns
t_{LPW}	22		34	ns

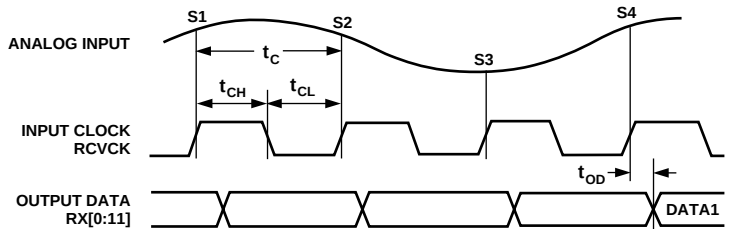


Figure 6. Receive Interface Timing Diagram

Table IX. Receive Switching Specifications

Symbol	Parameter	Min	Typ	Max	Units
t_C	Clock Period	100		104	ns
t_{CH}	CLOCK Pulsewidth High	45			ns
t_{CL}	CLOCK Pulsewidth Low	45			ns
t_{OD}	Output Delay	8	13	19	ns
Latency	Pipeline Delay	3	3	3	Cycles

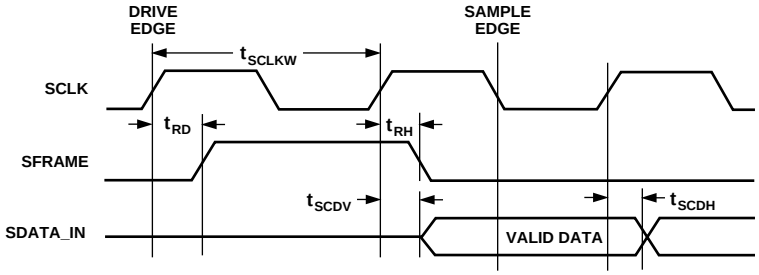


Figure 7. ADSP-2183 Timing

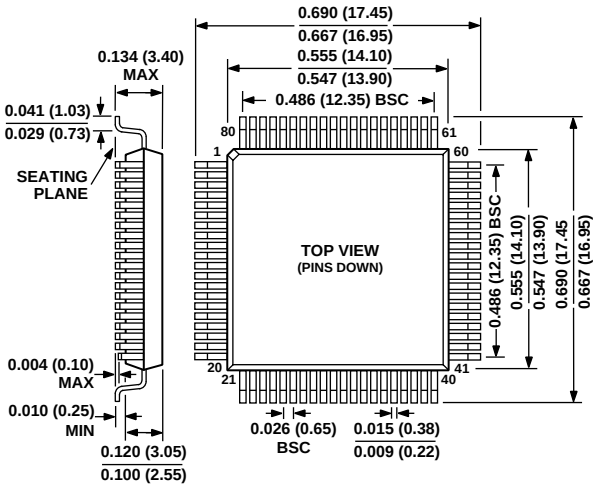
Table X. ADSP-2183 Timing Parameters

Symbol	External Clock Switching Characteristics	Typ	Min	Max	Units
t_{SCLKW}	Clock Period (13.248 MHz)	76			ns
t_{RD}	SFRAME Delay After SCLK			15	ns
t_{RH}	SFRAME Hold After SCLK		0		ns
t_{SCDV}	SCLK High to SDATA Valid			15	ns
t_{SCDH}	Transmit Data Hold After SCLK		0		ns

OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

80-Lead Plastic Quad Flatpack (MQFP)
(S-80A)



C3539–2.5–4/99

PRINTED IN U.S.A.