




## Product Specification

AU OPTRONICS CORPORATION

( V ) Preliminary Specifications

( ) Final Specifications

|  |  |
|--|--|
| Module   | 11.6"(11.57") HD 16:9 Color TFT-LCD<br>with LED Backlight design |
| Model Name   | B116XTN02.0 (H/W:1A)   |
| Note (  ) | <i>LED Backlight with driving circuit design</i>                 |

|   |      |
|---|------|
| Customer  | Date |
| Checked & Approved by   | Date |
| Note: This Specification is subject to change without notice. |      |

|   |                  |
|---|------------------|
| Approved by   | Date             |
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## Product Specification

AU OPTRONICS CORPORATION

### Record of Revision

| Version and Date | Page | Old description            | New Description | Remark |
|------------------|------|----------------------------|-----------------|--------|
| 0.1 2012/3/20    | All  | First Edition for Customer |                 |        |
| 0.2 2012/3/28    | 29   | TBD                        | Update EDID     |        |

## 1. Handling Precautions

- 1) Since front polarizer is easily damaged, pay attention not to scratch it.
- 2) Be sure to turn off power supply when inserting or disconnecting from input connector.
- 3) Wipe off water drop immediately. Long contact with water may cause discoloration or spots.
- 4) When the panel surface is soiled, wipe it with absorbent cotton or other soft cloth.
- 5) Since the panel is made of glass, it may break or crack if dropped or bumped on hard surface.
- 6) Since CMOS LSI is used in this module, take care of static electricity and insure human earth when handling.
- 7) Do not open nor modify the Module Assembly.
- 8) Do not press the reflector sheet at the back of the module to any directions.
- 9) At the insertion or removal of the Signal Interface Connector, be sure not to rotate nor tilt the Interface Connector of the TFT Module.
- 11) After installation of the TFT Module into an enclosure (Notebook PC Bezel, for example), do not twist nor bend the TFT Module even momentarily. At designing the enclosure, it should be taken into consideration that no bending/twisting forces are applied to the TFT Module from outside. Otherwise the TFT Module may be damaged.
- 12) Small amount of materials having no flammability grade is used in the LCD module. The LCD module should be supplied by power complied with requirements of Limited Power Source (IEC60950 or UL1950), or be applied exemption.
- 13) Disconnecting power supply before handling LCD modules, it can prevent electric shock, DO NOT TOUCH the electrode parts, cables, connectors and LED circuit part of TFT module that a LED light bar build in as a light source of back light unit. It can prevent electrostatic breakdown.

## 2. General Description

B116XTN02.0 is a Color Active Matrix Liquid Crystal Display composed of a TFT LCD panel, a driver circuit, and LED backlight system. The screen format is intended to support the 16:9 HD, 1366(H) x 768(V) screen and 262k colors (RGB 6-bits data driver) with LED backlight driving circuit. All input signals are LVDS interface compatible.

B116XTN02.0 is designed for a display unit of notebook style personal computer and industrial machine.

### 2.1 General Specification

The following items are characteristics summary on the table at 25 °C condition:

| Items   | Unit                 | Specifications                         |       |      |       |
|---|----------------------|--|-------|------|-------|
| Screen Diagonal   | [mm]                 | 293.8                                  |       |      |       |
| Active Area   | [mm]                 | 256.125 X 144.0                        |       |      |       |
| Pixels H x V  |                      | 1366x3(RGB) x 768                      |       |      |       |
| Pixel Pitch   | [mm]                 | 0.1875 x 0.1875                        |       |      |       |
| Pixel Format  |                      | R.G.B. Vertical Stripe                 |       |      |       |
| Display Mode  |                      | Normally White                         |       |      |       |
| White Luminance (I <sub>LED</sub> =20mA)<br>(Note: I <sub>LED</sub> is LED current) | [cd/m <sup>2</sup> ] | 200 typ. (5 points average)            |       |      |       |
| Luminance Uniformity  |                      | 1.6 max. (13 points)                   |       |      |       |
| Contrast Ratio  |                      | 500 typ                                |       |      |       |
| Response Time   | [ms]                 | 8 typ                                  |       |      |       |
| Nominal Input Voltage VDD   | [Volt]               | +3.3 typ.                              |       |      |       |
| Power Consumption   | [Watt]               | 2.6 max. (Include Logic and BLU power) |       |      |       |
| Weight  | [Grams]              | 220 max.                               |       |      |       |
| Physical Size<br>Include bracket  | [mm]                 |  | Min.  | Typ. | Max.  |
|   |                      | Length                                 | 277.5 | 278  | 278.5 |
|   |                      | Width                                  | 167.5 | 168  | 168.5 |
|   |                      | Thickness                              | -     | -    | 3.0   |
| Electrical Interface  |                      | 1 channel LVDS                         |       |      |       |
| Glass Thickness   | [mm]                 | 0.4                                    |       |      |       |
| Surface Treatment   |                      | Glare, Hardness 3H,                    |       |      |       |
| Support Color   |                      | 262K colors ( RGB 6-bit )              |       |      |       |

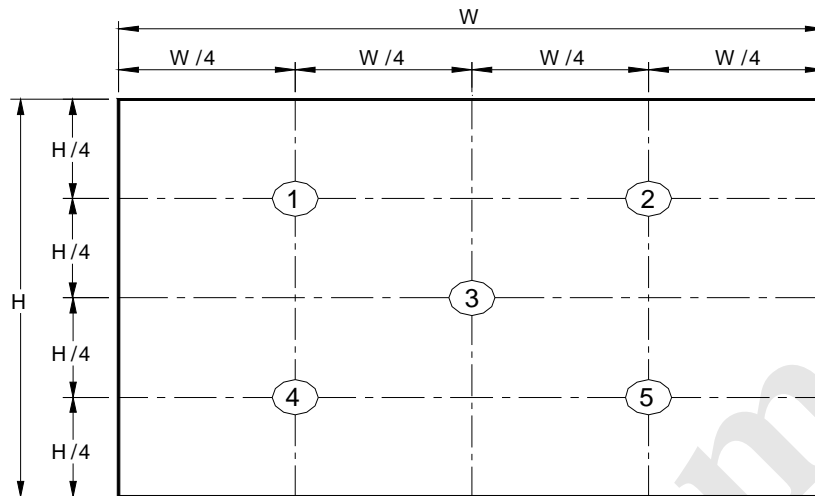
|   |              |                        |
|---|--------------|------------------------|
| Temperature Range<br>Operating<br>Storage (Non-Operating) | [°C]<br>[°C] | 0 to +50<br>-20 to +60 |
| RoHS Compliance   |              | RoHS Compliance        |

## 2.2 Optical Characteristics

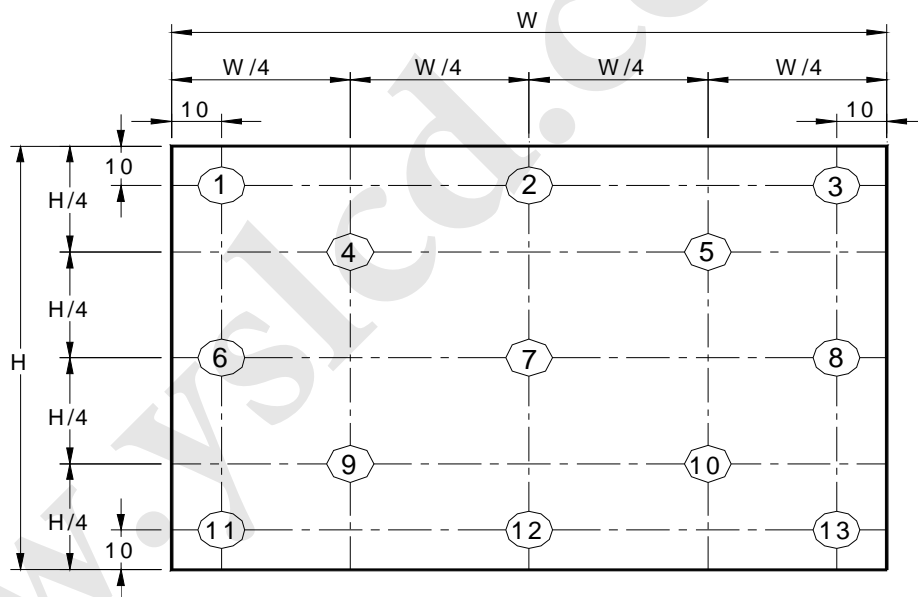
The optical characteristics are measured under stable conditions at 25°C (Room Temperature) :

| Item                              | Symbol         | Conditions         | Min.  | Typ.  | Max.  | Unit              | Note     |
|-----------------------------------|----------------|--------------------|-------|-------|-------|-------------------|----------|
| White Luminance<br>$I_{LED}=20mA$ |                | 5 points average   | 170   | 200   | -     | cd/m <sup>2</sup> | 1, 4, 5. |
| Viewing Angle                     | $\theta_R$     | Horizontal (Right) | 40    | 45    | -     | degree            | 4, 9     |
|                                   | $\theta_L$     | CR = 10 (Left)     | 40    | 45    | -     |                   |          |
|                                   | $\phi_H$       | Vertical (Upper)   | 10    | 15    | -     |                   |          |
|                                   | $\phi_L$       | CR = 10 (Lower)    | 30    | 35    | -     |                   |          |
| Luminance Uniformity              | $\delta_{5P}$  | 5 Points           | -     | -     | 1.25  |                   | 1, 3, 4  |
| Luminance Uniformity              | $\delta_{13P}$ | 13 Points          | -     | -     | 1.6   |                   | 2, 3, 4  |
| Contrast Ratio                    | CR             |                    | 400   | 500   | -     |                   | 4, 6     |
| Cross talk                        | %              |                    |       |       | 4     |                   | 4, 7     |
| Response Time                     | $T_r$          | Rising             | -     |       | -     | msec              | 4, 8     |
|                                   | $T_f$          | Falling            | -     |       | -     |                   |          |
|                                   | $T_{RT}$       | Rising + Falling   | -     | 8     | 16    |                   |          |
| Color / Chromaticity Coordinates  | Red            | Rx                 | 0.537 | 0.567 | 0.597 |                   | 4        |
|                                   |                | Ry                 | 0.304 | 0.334 | 0.364 |                   |          |
|                                   | Green          | Gx                 | 0.300 | 0.330 | 0.360 |                   |          |
|                                   |                | Gy                 | 0.539 | 0.569 | 0.599 |                   |          |
|                                   | Blue           | Bx                 | 0.125 | 0.155 | 0.185 |                   |          |
|                                   |                | By                 | 0.106 | 0.136 | 0.166 |                   |          |
|                                   | White          | Wx                 | 0.283 | 0.313 | 0.343 |                   |          |
|                                   |                | Wy                 | 0.299 | 0.329 | 0.359 |                   |          |
| NTSC                              | %              |                    | -     | 45    | -     |                   |          |

**Note 1:** 5 points position (Ref: Active area)



**Note 2:** 13 points position (Ref: Active area)



**Note 3:** The luminance uniformity of 5 or 13 points is defined by dividing the maximum luminance values by the minimum test point luminance

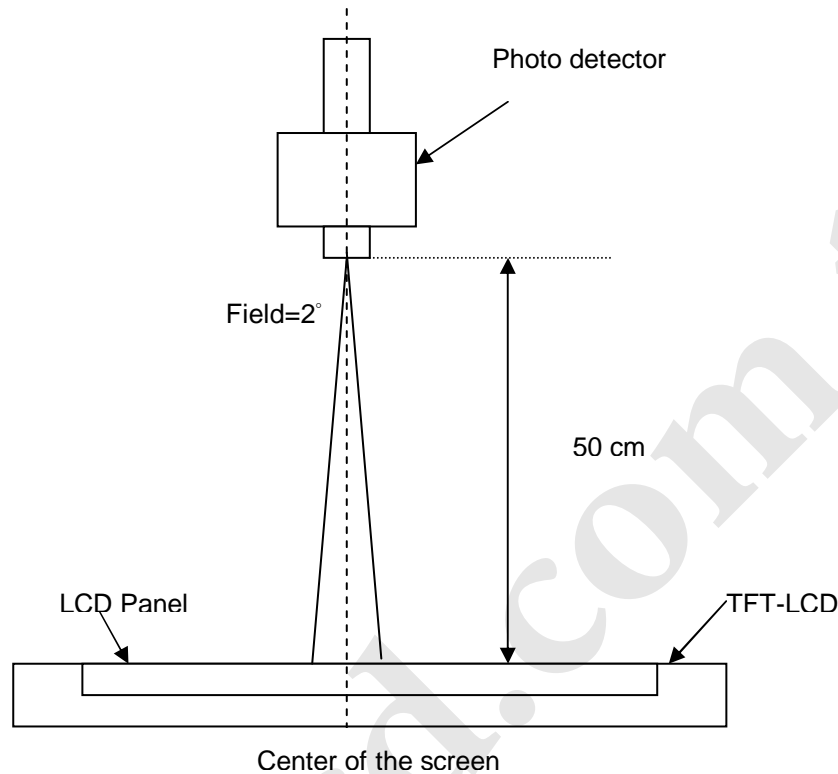
$$\delta_{W5} = \frac{\text{Maximum Brightness of five points}}{\text{Minimum Brightness of five points}}$$

$$\delta_{W13} = \frac{\text{Maximum Brightness of thirteen points}}{\text{Minimum Brightness of thirteen points}}$$

**Note 4:** Measurement method

The LCD module should be stabilized at given temperature for 30 minutes to avoid abrupt temperature change during measuring. In order to stabilize the luminance, the measurement should be executed after

lighting Backlight for 30 minutes in a stable, windless and dark room, and it should be measured in the center of screen.



**Note 5 :** Definition of Average Luminance of White ( $Y_L$ ):

Measure the luminance of gray level 63 at 5 points ,  $Y_L = [L(1) + L(2) + L(3) + L(4) + L(5)] / 5$

$L(x)$  is corresponding to the luminance of the point X at Figure in Note (1).

**Note 6 :** Definition of contrast ratio:

Contrast ratio is calculated with the following formula.

$$\text{Contrast ratio (CR)} = \frac{\text{Brightness on the "White" state}}{\text{Brightness on the "Black" state}}$$

**Note 7 :** Definition of Cross Talk (CT)

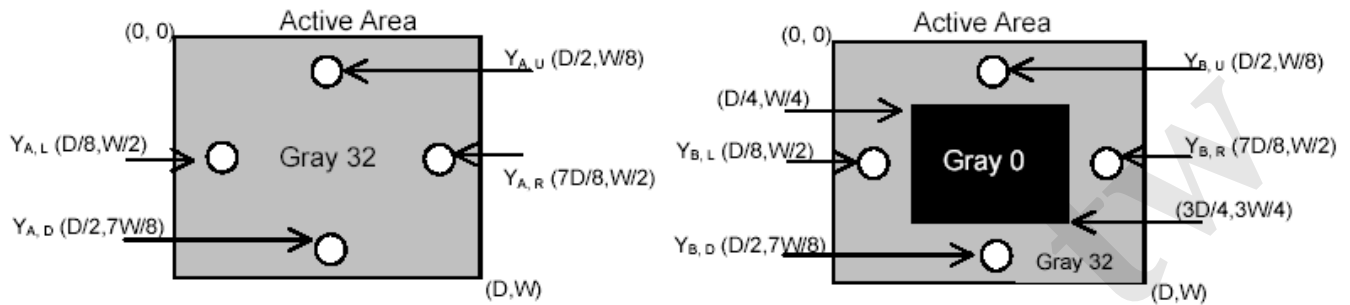
$$CT = |Y_B - Y_A| / Y_A \times 100 (\%)$$

Where

$Y_A$  = Luminance of measured location without gray level 0 pattern (cd/m<sup>2</sup>)

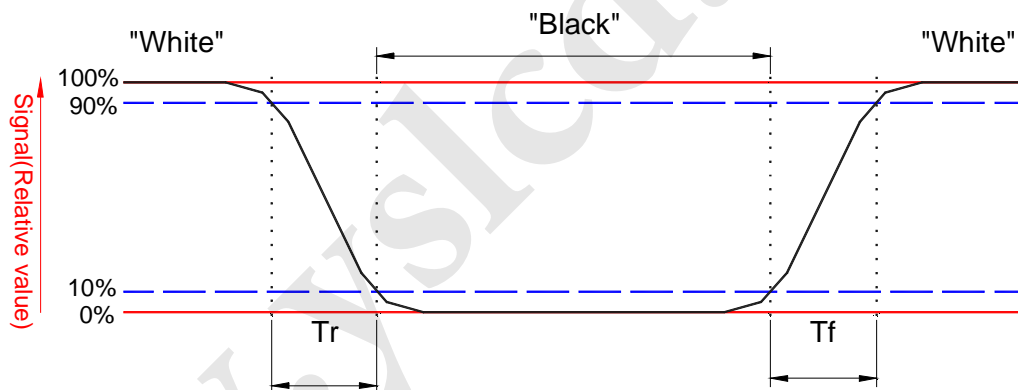
$Y_B$  = Luminance of measured location with gray level 0 pattern (cd/m<sup>2</sup>)





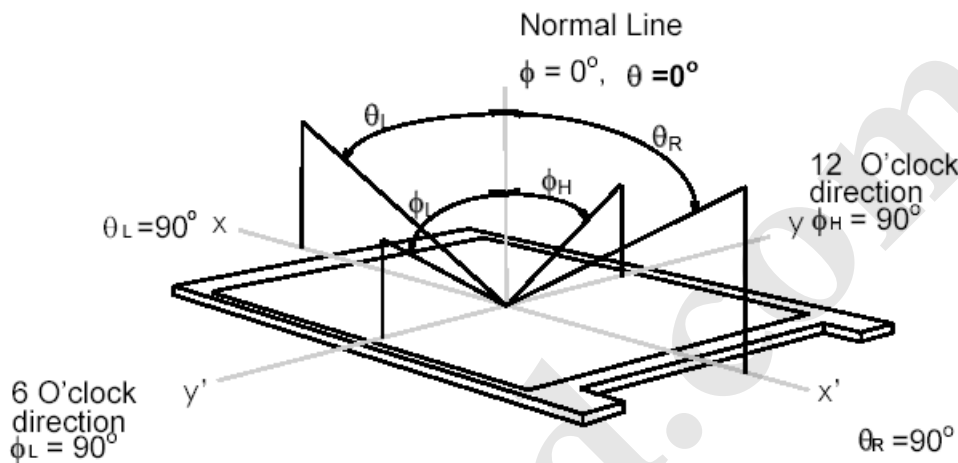
**Note 8:** Definition of response time:

The output signals of BM-7 or equivalent are measured when the input signals are changed from "Black" to "White" (falling time) and from "White" to "Black" (rising time), respectively. The response time interval between the 10% and 90% of amplitudes. Refer to figure as below.



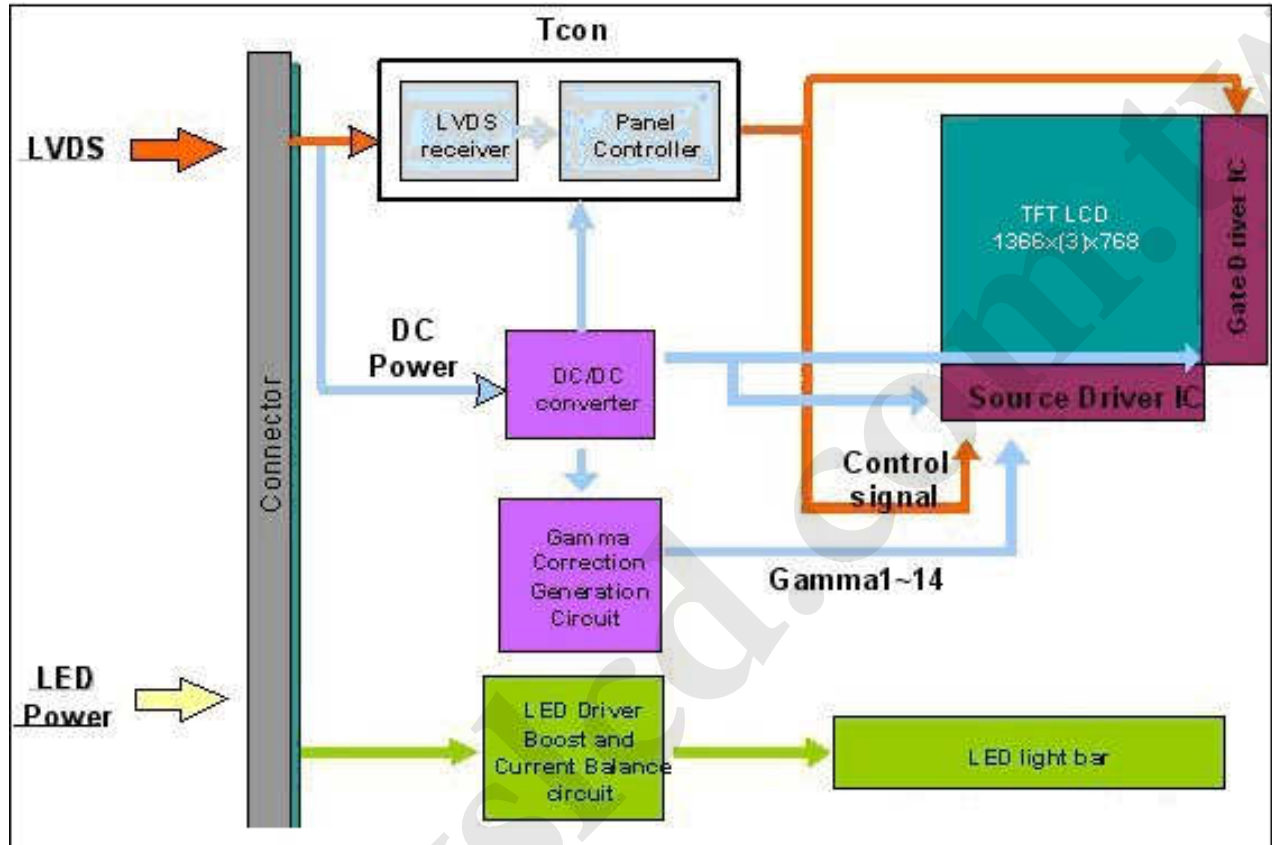
## Note 9. Definition of viewing angle

Viewing angle is the measurement of contrast ratio  $\geq 10$ , at the screen center, over a  $180^\circ$  horizontal and  $180^\circ$  vertical range (off-normal viewing angles). The  $180^\circ$  viewing angle range is broken down as follows;  $90^\circ$  ( $\theta$ ) horizontal left and right and  $90^\circ$  ( $\phi$ ) vertical, high (up) and low (down). The measurement direction is typically perpendicular to the display surface with the screen rotated about its center to develop the desired measurement viewing angle.



## 3. Functional Block Diagram

The following diagram shows the functional block of the 11.6 inches wide Color TFT/LCD 40 Pin one channel Module



## 4. Absolute Maximum Ratings

An absolute maximum rating of the module is as following:

### 4.1 Absolute Ratings of TFT LCD Module

| Item            | Symbol | Min  | Max  | Unit   | Conditions |
|-----------------|--------|------|------|--------|------------|
| Logic/LCD Drive | Vin    | -0.3 | +4.0 | [Volt] | Note 1,2   |

### 4.2 Absolute Ratings of Environment

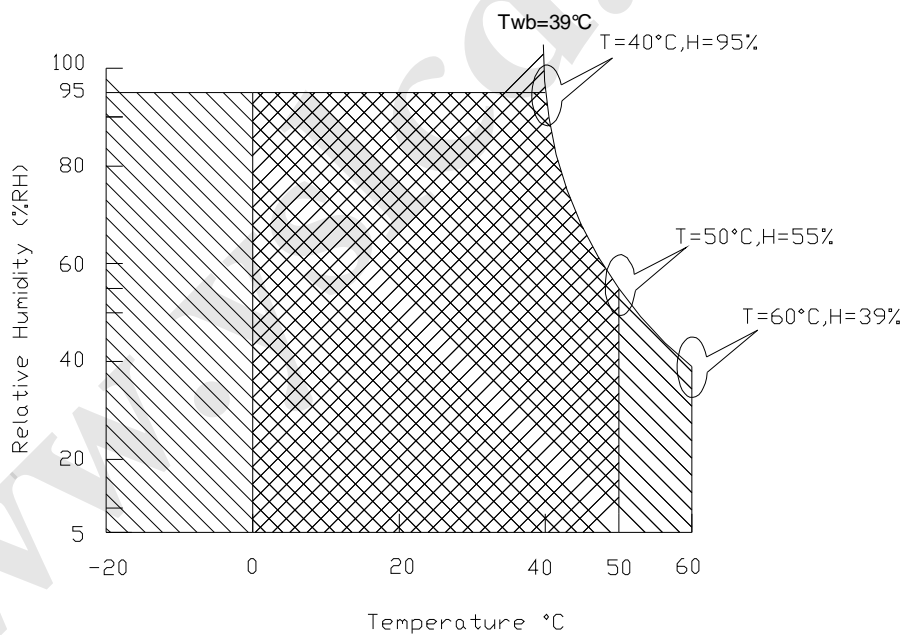
| Item                  | Symbol | Min | Max | Unit  | Conditions |
|-----------------------|--------|-----|-----|-------|------------|
| Operating Temperature | TOP    | 0   | +50 | [°C]  | Note 4     |
| Operation Humidity    | HOP    | 5   | 95  | [%RH] | Note 4     |
| Storage Temperature   | TST    | -20 | +60 | [°C]  | Note 4     |
| Storage Humidity      | HST    | 5   | 95  | [%RH] | Note 4     |

Note 1: At Ta (25°C )

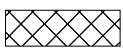
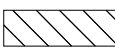
Note 2: Permanent damage to the device may occur if exceed maximum values

Note 3: LED specification refer to section 5.2

Note 4: For quality performance, please refer to AUO IIS (Incoming Inspection Standard).



Operating Range 

Storage Range  + 

## 5. Electrical Characteristics

### 5.1 TFT LCD Module

#### 5.1.1 Power Specification

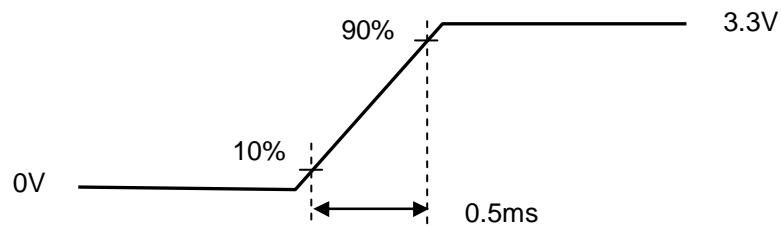
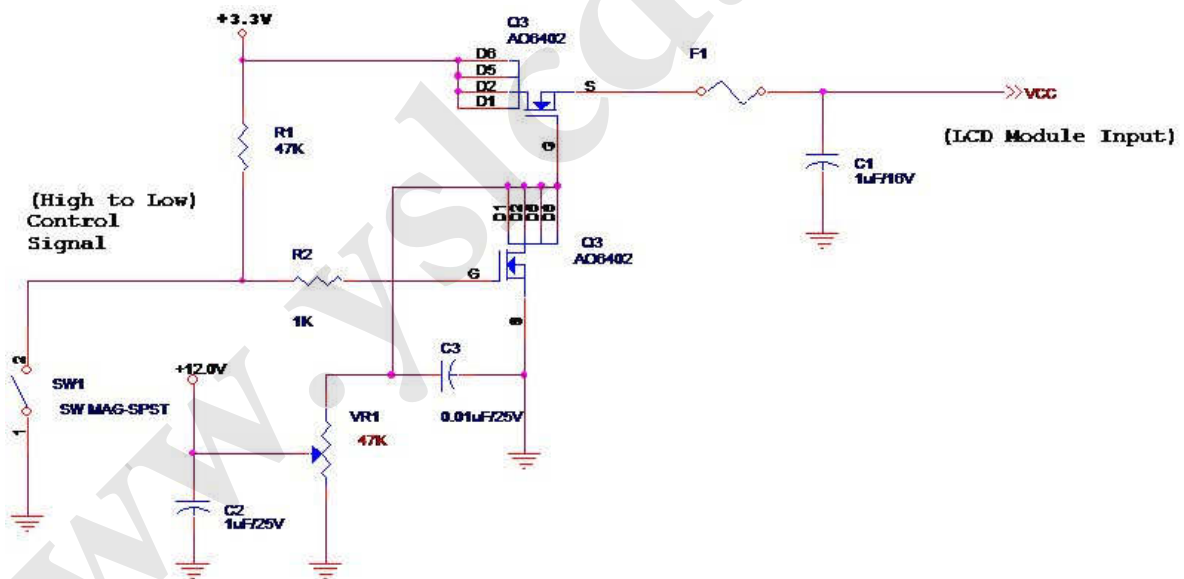
Input power specifications are as follows;

The power specification are measured under 25°C and frame frequency under 60Hz

| Symble | Parameter                                | Min | Typ | Max  | Units       | Note   |
|--------|--|-----|-----|------|-------------|--------|
| VDD    | Logic/LCD Drive Voltage                  | 3.0 | 3.3 | 3.6  | [Volt]      |        |
| PDD    | VDD Power                                | -   | -   | 0.65 | [Watt]      | Note 1 |
| IDD    | IDD Current                              | -   | -   | 606  | [mA]        | Note 1 |
| IRush  | Inrush Current                           | -   | -   | 2000 | [mA]        | Note 2 |
| VDDrp  | Allowable Logic/LCD Drive Ripple Voltage | -   | -   | 100  | [mV]<br>p-p |        |

Note 1 : Maximum Measurement Condition : Black Pattern at 3.3V driving voltage. ( $P_{max}=V_{3.3} \times I_{black}$ )

Note 2 : Measure Condition



Vin rising time

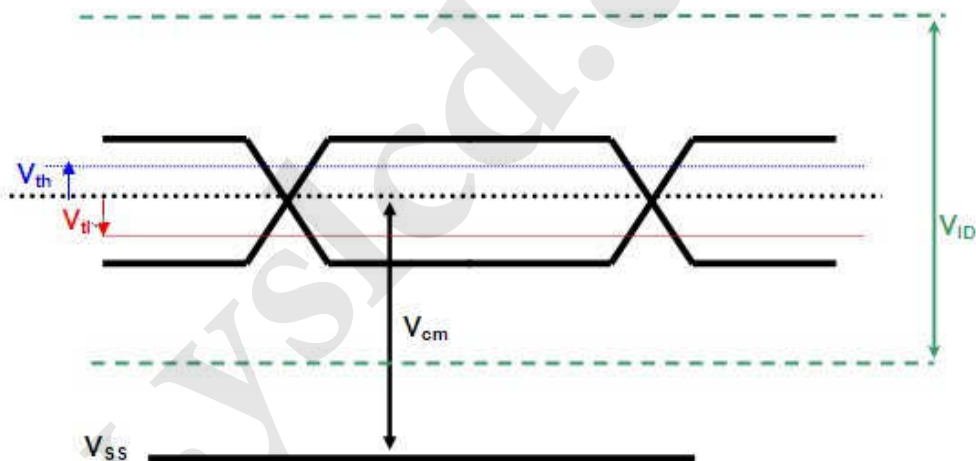
## 5.1.2 Signal Electrical Characteristics

Input signals shall be low or High-impedance state when VDD is off.

Signal electrical characteristics are as follows;

| Parameter | Condition  | Min   | Max   | Unit |
|-----------|--|-------|-------|------|
| $V_{th}$  | Differential Input High Threshold ( $V_{cm}=+1.2V$ ) |       | 100   | [mV] |
| $V_{tl}$  | Differential Input Low Threshold ( $V_{cm}=+1.2V$ )  | -100  | -     | [mV] |
| $V_{ID}$  | Differential Input Voltage                           | 100   | 600   | [mV] |
| $V_{cm}$  | Differential Input Common Mode Voltage               | 1.125 | 1.375 | [V]  |

Note: LVDS Signal Waveform





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### 5.2 Backlight Unit

#### 5.2.1 LED characteristics

| Parameter                   | Symbol | Min   | Typ | Max | Units  | Condition                     |
|-----------------------------|--------|-------|-----|-----|--------|-------------------------------|
| Backlight Power Consumption | PLED   | -     | -   | 1.8 | [Watt] | (Ta=25°C), Note 1<br>Vin =12V |
| LED Life-Time               | N/A    | 15000 | -   | -   | Hour   | (Ta=25°C), Note 2<br>IF=20 mA |

**Note 1:** Calculator value for reference  $P_{LED} = V_F$  (Normal Distribution) \*  $I_F$  (Normal Distribution) / Efficiency

**Note 2:** The LED life-time define as the estimated time to 50% degradation of initial luminous.

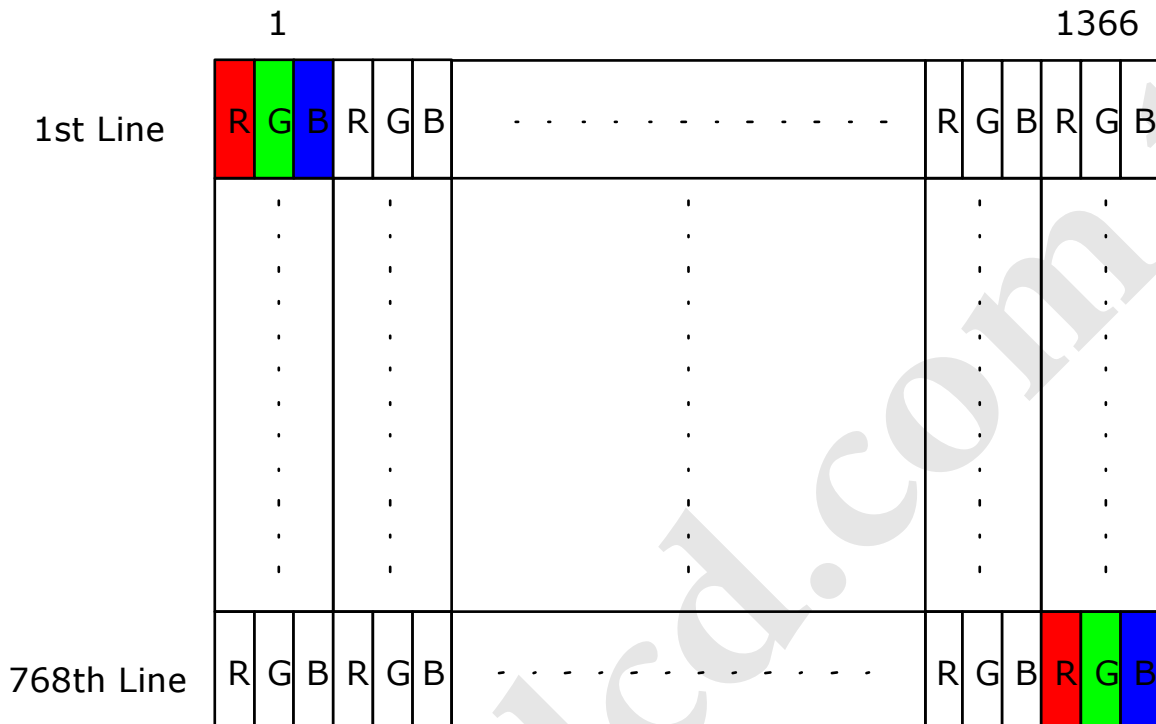
#### 5.2.2 Backlight input signal characteristics

| Parameter                      | Symbol  | Min | Typ  | Max  | Units  | Remark   |
|--------------------------------|---------|-----|------|------|--------|--|
| LED Power Supply               | VLED    | 6.0 | 12.0 | 21.0 | [Volt] | Define as<br>Connector<br>Interface<br>(Ta=25°C) |
| LED Enable Input<br>High Level | VLED_EN | 2.5 | -    | 5.5  | [Volt] |  |
| LED Enable Input<br>Low Level  |         | -   | -    | 0.5  | [Volt] |  |
| PWM Logic Input<br>High Level  | VPWM_EN | 2.5 | -    | 5.5  | [Volt] |  |
| PWM Logic Input<br>Low Level   |         | -   | -    | 0.5  | [Volt] |  |
| PWM Input Frequency            | FPWM    | 200 | 1K   | 10K  | Hz     |  |
| PWM Duty Ratio                 | Duty    | 5   | --   | 100  | %      |  |

## 6. Signal Interface Characteristic

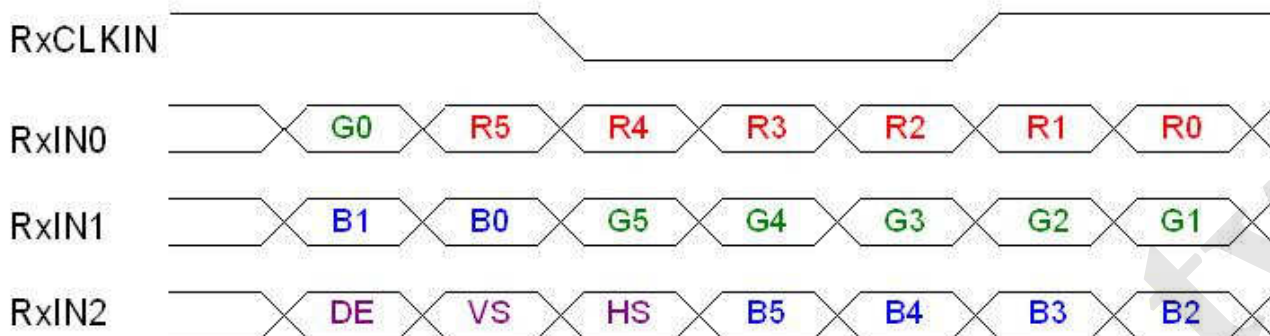
### 6.1 Pixel Format Image

Following figure shows the relationship of the input signals and LCD pixel format.





## 6.2 The Input Data Format



| Signal Name                      | Description  |   |
|----------------------------------|--|---|
| R5<br>R4<br>R3<br>R2<br>R1<br>R0 | Red Data 5 (MSB)<br>Red Data 4<br>Red Data 3<br>Red Data 2<br>Red Data 1<br>Red Data 0 (LSB)<br><br>Red-pixel Data               | Red-pixel Data<br>Each red pixel's brightness data consists of these 6 bits pixel data.   |
| G5<br>G4<br>G3<br>G2<br>G1<br>G0 | Green Data 5 (MSB)<br>Green Data 4<br>Green Data 3<br>Green Data 2<br>Green Data 1<br>Green Data 0 (LSB)<br><br>Green-pixel Data | Green-pixel Data<br>Each green pixel's brightness data consists of these 6 bits pixel data.   |
| B5<br>B4<br>B3<br>B2<br>B1<br>B0 | Blue Data 5 (MSB)<br>Blue Data 4<br>Blue Data 3<br>Blue Data 2<br>Blue Data 1<br>Blue Data 0 (LSB)<br>Blue-pixel Data            | Blue-pixel Data<br>Each blue pixel's brightness data consists of these 6 bits pixel data.   |
| RxCLKIN                          | Data Clock   | The signal is used to strobe the pixel data and DE signals. All pixel data shall be valid at the falling edge when the DE signal is high. |
| DE                               | Display Timing   | This signal is strobed at the falling edge of RxCLKIN. When the signal is high, the pixel data shall be valid to be displayed.            |
| VS                               | Vertical Sync  | The signal is synchronized to RxCLKIN .   |
| HS                               | Horizontal Sync  | The signal is synchronized to RxCLKIN .   |

Note: Output signals from any system shall be low or High-impedance state when VDD is off.

## 6.3 Integration Interface Requirement

### 6.3.1 Connector Description

Physical interface is described as for the connector on module.

These connectors are capable of accommodating the following signals and will be following components.

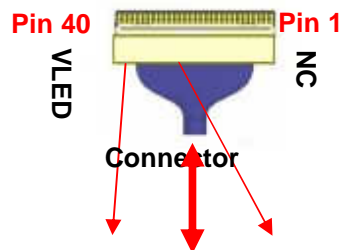
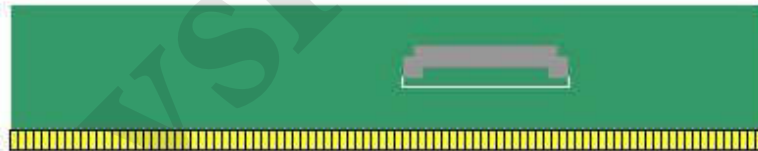
| Connector Name / Designation | For Signal Connector             |
|------------------------------|----------------------------------|
| Manufacturer                 | IPEX or compatible               |
| Type / Part Number           | STM(MASK24025P40)                |
| Mating Housing/Part Number   | IPEX 20353-040T-11 or compatible |

### 6.3.2 Pin Assignment

LVDS is a differential signal technology for LCD interface and high speed data transfer device.

| PIN# | Signal Name | Description                                       |
|------|-------------|---|
| 1    | NC          | No connection                                     |
| 2    | VDD         | Power Supply +3.3V                                |
| 3    | VDD         | Power Supply +3.3V                                |
| 4    | VEDID       | EDID +3.3V Power                                  |
| 5    | AGING       | AGING Enable                                      |
| 6    | CLK_EDID    | EDID Clock Input                                  |
| 7    | DAT_EDID    | EDID Data Input                                   |
| 8    | RxOIN0-     | -LVDS Differential Data INPUT(Odd R0-R5,G0)       |
| 9    | RxOIN0+     | +LVDS Differential Data INPUT(Odd R0-R5,G0)       |
| 10   | VSS         | Ground  |
| 11   | RxOIN1-     | -LVDS Differential Data INPUT(Odd G1-G5,B0-B1)    |
| 12   | RxOIN1+     | +LVDS Differential Data INPUT(Odd G1-G5,B0-B1)    |
| 13   | VSS         | Ground  |
| 14   | RxOIN2-     | -LVDS Differential Data INPUT(Odd B2-B5,HS,VS,DE) |
| 15   | RxOIN2+     | +LVDS Differential Data INPUT(Odd B2-B5,HS,VS,DE) |
| 16   | VSS         | Ground  |
| 17   | RxOCKIN-    | -LVDS Odd Differential Clock INPUT                |
| 18   | RxOCKIN+    | +LVDS Odd Differential Clock INPUT                |
| 19   | NC          | No connection                                     |
| 20   | NC          | No connection                                     |
| 21   | NC          | No connection                                     |
| 22   | VSS         | Ground  |

|    |          |                        |
|----|----------|------------------------|
| 23 | NC       | No connection          |
| 24 | NC       | No connection          |
| 25 | VSS      | Ground                 |
| 26 | NC       | No connection          |
| 27 | NC       | No connection          |
| 28 | VSS      | Ground                 |
| 29 | NC       | No connection          |
| 30 | NC       | No connection          |
| 31 | VLED_GND | LED Ground             |
| 32 | VLED_GND | LED Ground             |
| 33 | VLED_GND | LED Ground             |
| 34 | NC       | No connection          |
| 35 | VPWM_EN  | PWM logic input level  |
| 36 | VLED_EN  | LED enable input level |
| 37 | NC       | No connection          |
| 38 | VLED     | LED Power Supply       |
| 39 | VLED     | LED Power Supply       |
| 40 | VLED     | LED Power Supply       |



Note1: Input signals shall be low or High-impedance state when VDD is off.

## 6.4 Interface Timing

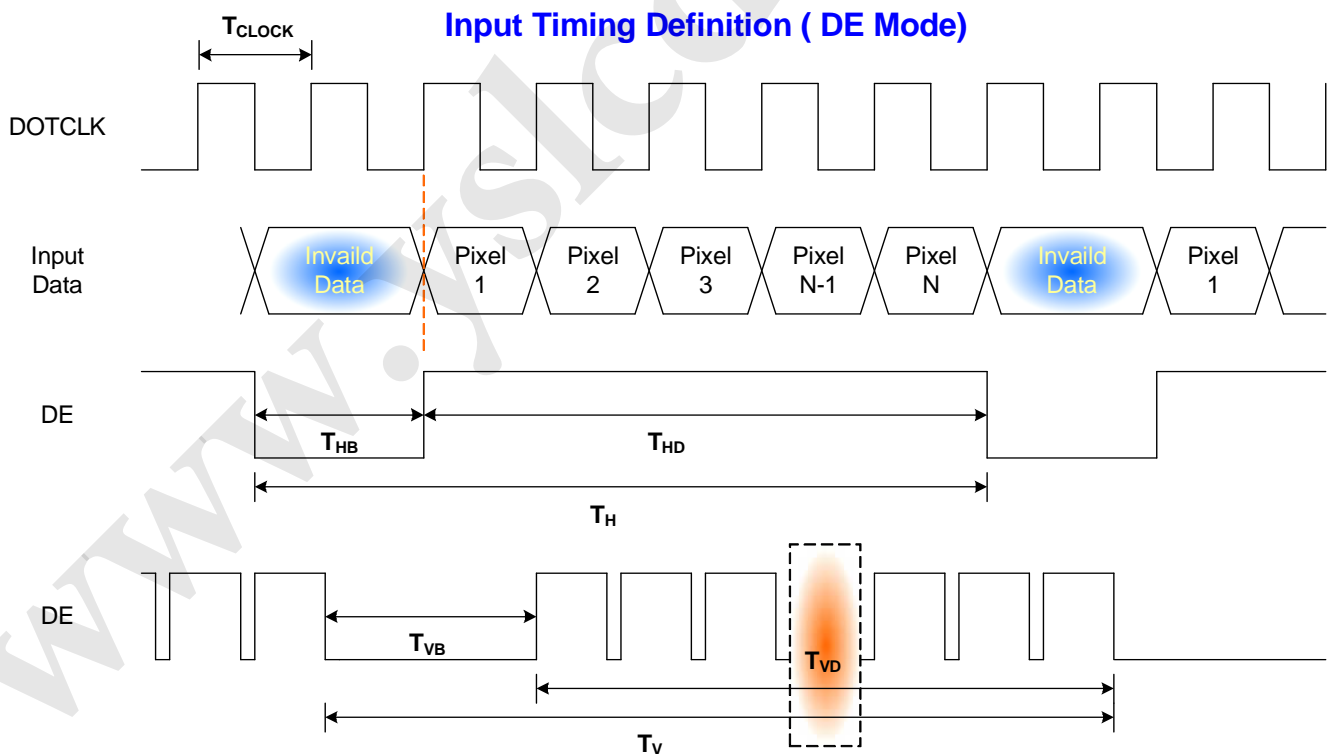
### 6.4.1 Timing Characteristics

Basically, interface timings should match the 1366x768 /60Hz manufacturing guide line timing.

| Parameter             |          | Symbol                | Min. | Typ. | Max. | Unit               |
|-----------------------|----------|-----------------------|------|------|------|--------------------|
| Frame Rate            |          | -                     |      | 60   | -    | Hz                 |
| Clock frequency       |          | 1/ T <sub>Clock</sub> | 66.4 | 76.3 | 80   | MHz                |
| Vertical<br>Section   | Period   | T <sub>V</sub>        | 776  | 798  | 801  | T <sub>Line</sub>  |
|                       | Active   | T <sub>VD</sub>       | 768  |      |      |                    |
|                       | Blanking | T <sub>VB</sub>       | 8    | 30   | 33   |                    |
| Horizontal<br>Section | Period   | T <sub>H</sub>        | 1416 | 1592 | 1666 | T <sub>Clock</sub> |
|                       | Active   | T <sub>HD</sub>       | 1366 |      |      |                    |
|                       | Blanking | T <sub>HB</sub>       | 50   | 226  | 300  |                    |

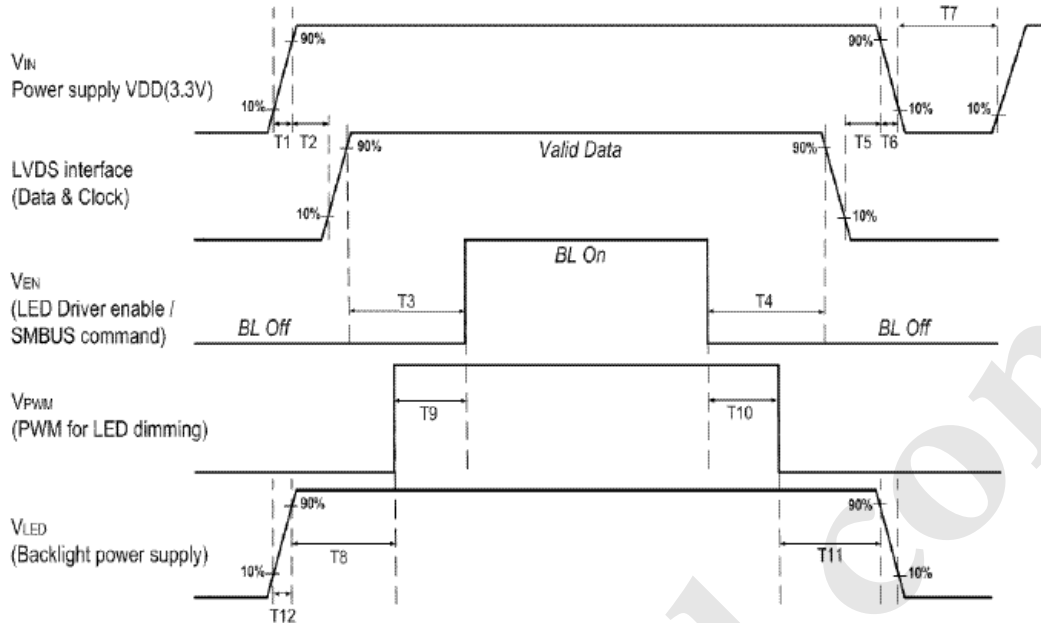
Note : DE mode only

### 6.4.2 Timing diagram

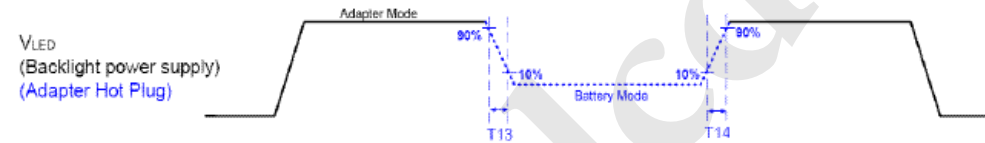


## 6.5 Power ON/OFF Sequence

Power on/off sequence is as follows. Interface signals and LED on/off sequence are also shown in the chart. Signals from any system shall be Hi-Z state or low level when VDD is off



Note : When the adapter is hot plugged, the backlight power supply sequence is shown as below.



|     | Min (ms) | Max (ms) |
|-----|----------|----------|
| T1  | 0.5      | 10       |
| T2  | 0        | 50       |
| T3  | 200      | -        |
| T4  | 200      | -        |
| T5  | 0        | 50       |
| T6  | 0        | 10       |
| T7  | 500      | -        |
| T8  | 10       | -        |
| T9  | 10       | -        |
| T10 | 10       | -        |
| T11 | 10       | -        |
| T12 | 0.5      | 10       |
| T13 | 1*       | -        |
| T14 | 1*       | -        |

Seamless change:  $T13/T14 = 5 \times T_{PWM}^*$

\* $T_{PWM} = 1/\text{PWM Frequency}$

## 7. Panel Reliability Test

### 7.1 Vibration Test

**Test Spec:**

- Test method: Non-Operation
- Acceleration: 1.5 G
- Frequency: 10 - 500Hz Random
- Sweep: 30 Minutes each Axis (X, Y, Z)

### 7.2 Shock Test

**Test Spec:**

- Test method: Non-Operation
- Acceleration: 220 G , Half sine wave
- Active time: 2 ms
- Pulse: X,Y,Z .one time for each side

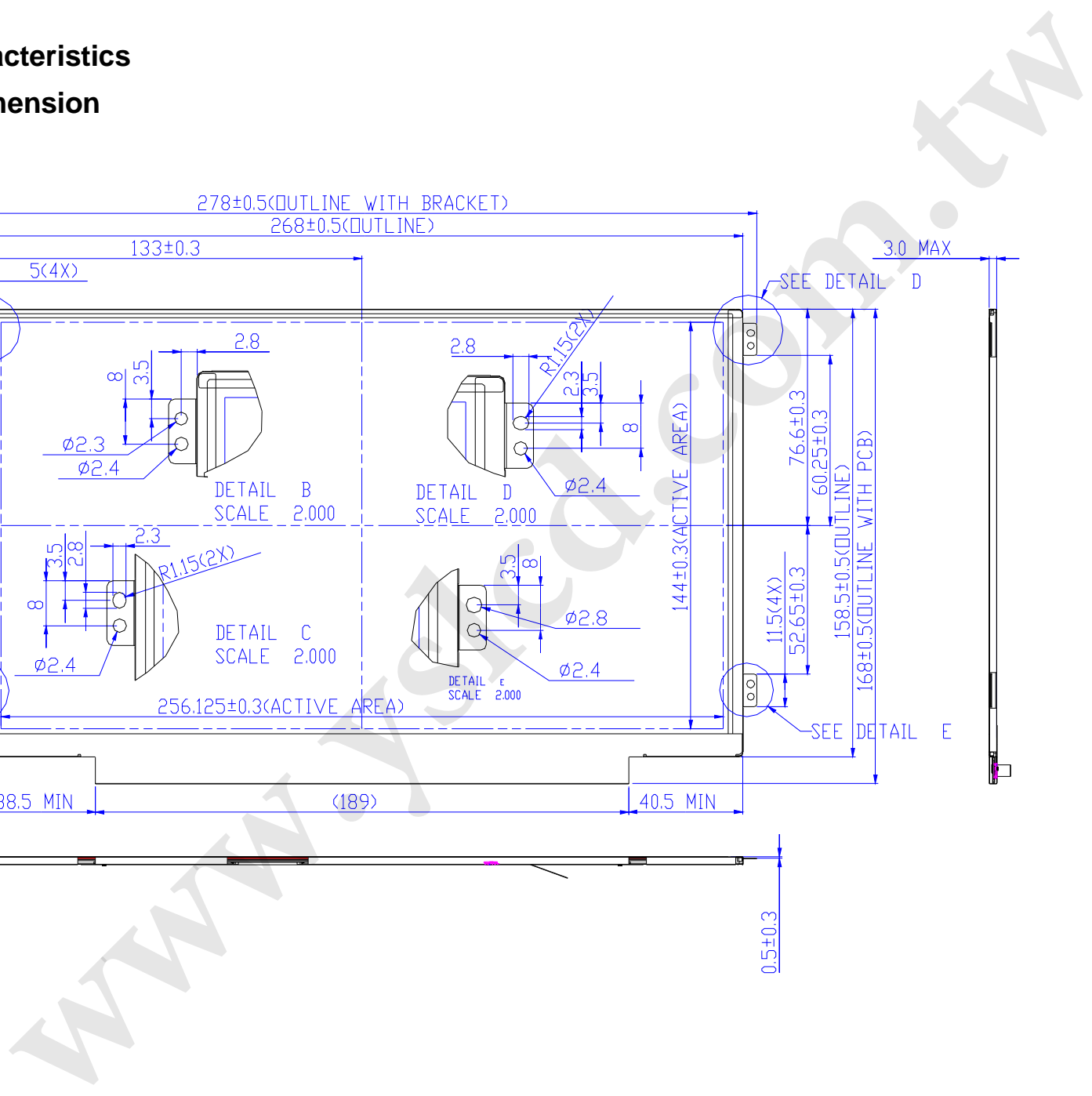
### 7.3 Reliability Test

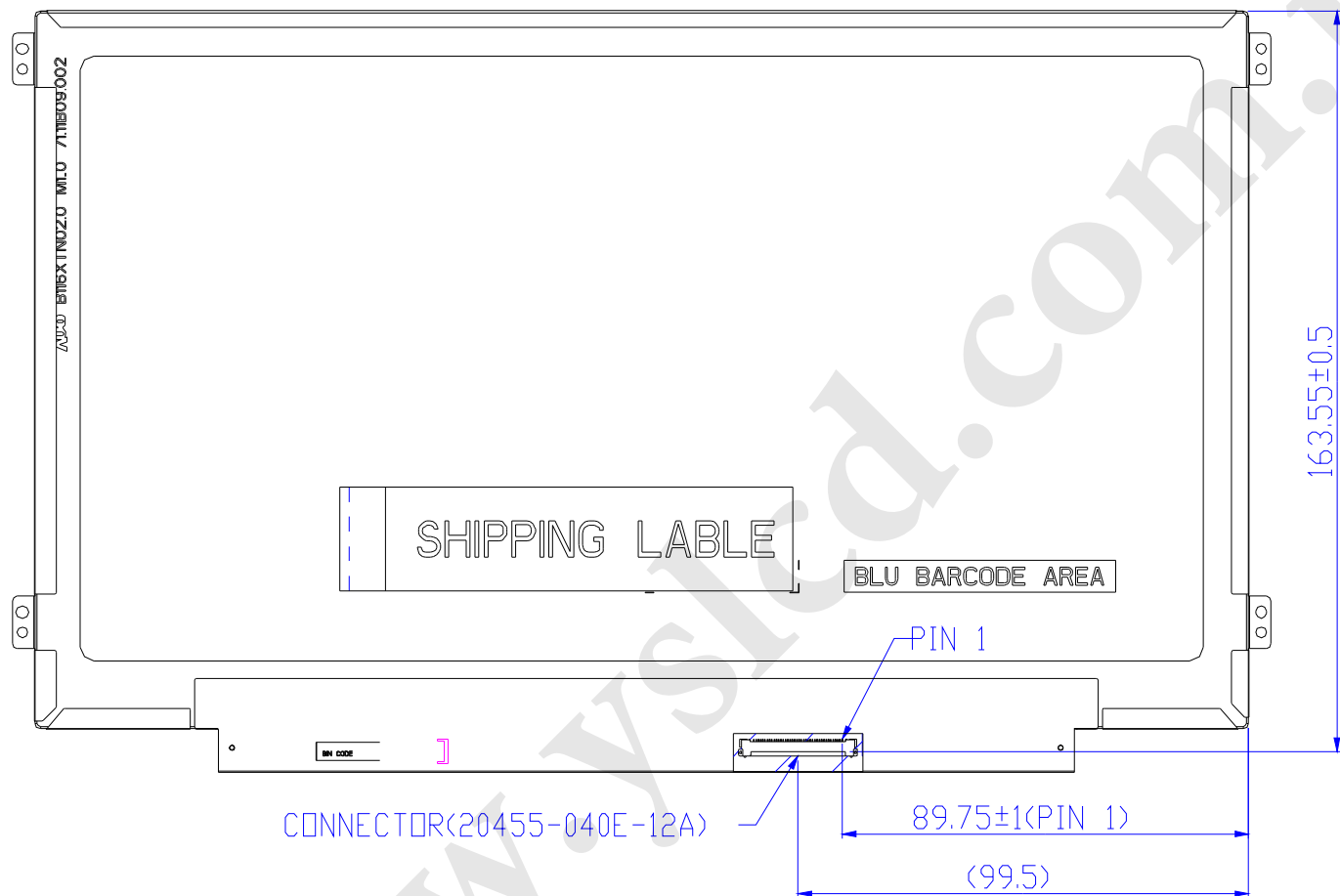
| Items                      | Required Condition                               | Note   |
|----------------------------|--|--------|
| Temperature Humidity Bias  | Ta= 40°C, 90%RH, 300h                            |        |
| High Temperature Operation | Ta= 50°C, Dry, 300h                              |        |
| Low Temperature Operation  | Ta= 0°C, 300h                                    |        |
| High Temperature Storage   | Ta= 60°C, 35%RH, 300h                            |        |
| Low Temperature Storage    | Ta= -20°C, 50%RH, 250h                           |        |
| Thermal Shock Test         | Ta=-20°C to 60°C, Duration at 30 min, 100 cycles |        |
| ESD                        | Contact : ±8 KV<br>Air : ±15 KV                  | Note 1 |

**Note1:** According to EN 61000-4-2 , ESD class B: Some performance degradation allowed. No data lost  
 . Self-recoverable. No hardware failures.

**Remark:** MTBF (Excluding the LED): 30,000 hours with a confidence level 90%

## 8.1 LCM Outline Dimension







## 9. Shipping and Package

### 9.1 Shipping Label Format

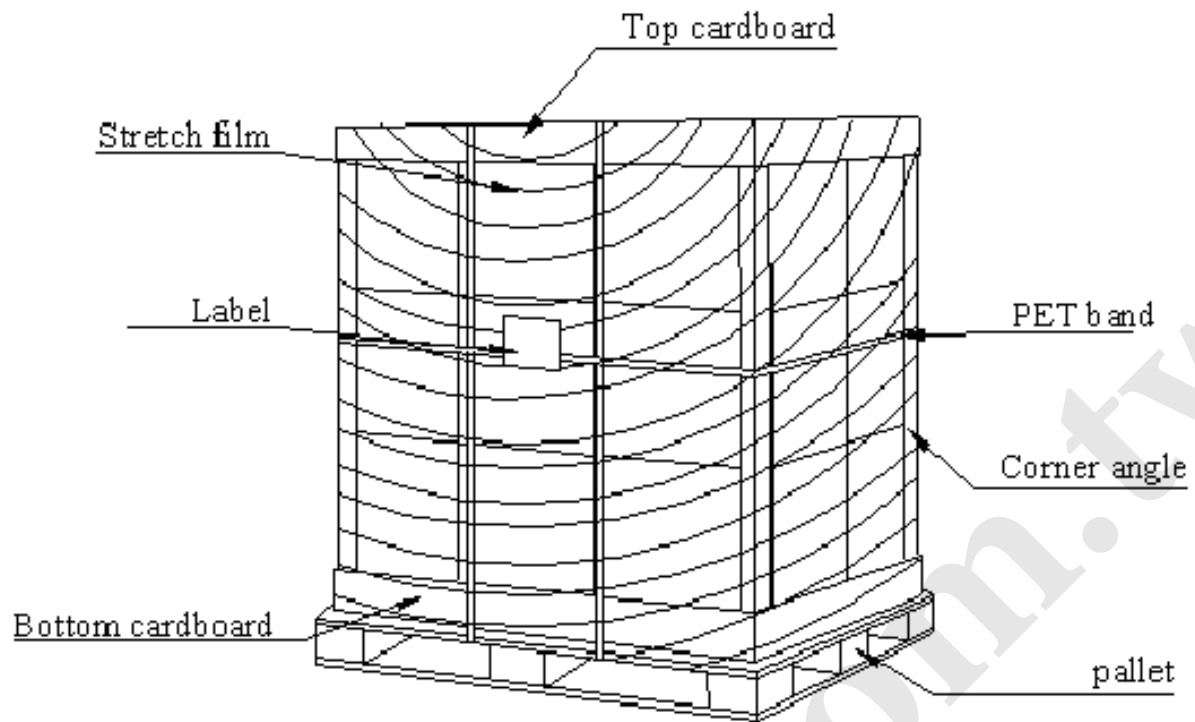
TBD

### 9.2 Carton Package

The outside dimension of carton is 553(L)mm\* 275(W)mm\* 379(H)mm



### 9.3 Shipping Package of Palletizing Sequence



## 9.4 Handling guide

This is a thin and slime LCD model, and please be cautious when pulling it out of package or assembling it onto platform. Careless handlings, e.g. twist, bending, pressing, or collision, will result malfunction of LCD models.

### (1) Handling method notice



Do not lift and hold the panel with single hand at right or left side from tray.



Lift and hold the panel up with both hands from tray.

### (2) On the table notice



Do not press edge of panel to avoid glass broken.

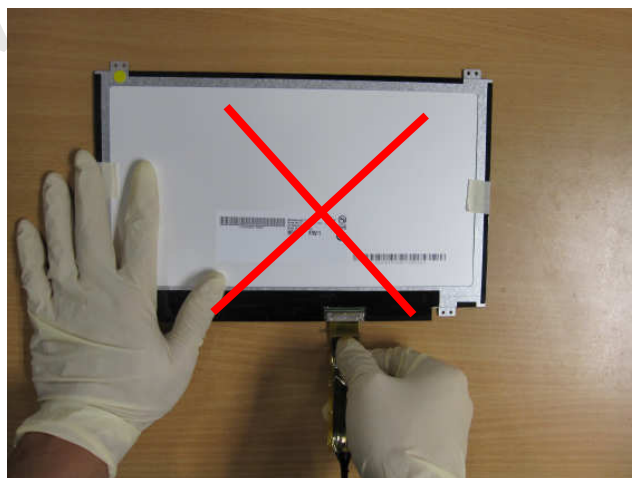


Do not press the surface of the panel to avoid the glass broken or polarizer scratch.



Do not put anything or tool on the panel to avoid the glass broken or polarizer scratch.

### (3) Cable assembly notice



Do not insert the connector with single hand and touching the PCBA.



Insert the connector by pushing right and left edge.

## 10. Appendix: EDID Description

| Address | FUNCTION                                       | Value | Value    | Value | Note |
|---------|--|-------|----------|-------|------|
| HEX     |  | HEX   | BIN      | DEC   |      |
| 00      | Header   | 00    | 00000000 | 0     |      |
| 01      |  | FF    | 11111111 | 255   |      |
| 02      |  | FF    | 11111111 | 255   |      |
| 03      |  | FF    | 11111111 | 255   |      |
| 04      |  | FF    | 11111111 | 255   |      |
| 05      |  | FF    | 11111111 | 255   |      |
| 06      |  | FF    | 11111111 | 255   |      |
| 07      |  | 00    | 00000000 | 0     |      |
| 08      | EISA Manuf. Code LSB                           | 06    | 00000110 | 6     |      |
| 09      | Compressed ASCII                               | AF    | 10101111 | 175   |      |
| 0A      | Product Code                                   | 5C    | 01011100 | 92    |      |
| 0B      | hex, LSB first                                 | 20    | 00100000 | 32    |      |
| 0C      | 32-bit ser #                                   | 00    | 00000000 | 0     |      |
| 0D      |  | 00    | 00000000 | 0     |      |
| 0E      |  | 00    | 00000000 | 0     |      |
| 0F      |  | 00    | 00000000 | 0     |      |
| 10      | Week of manufacture                            | 00    | 00000000 | 0     |      |
| 11      | Year of manufacture                            | 16    | 00010110 | 22    |      |
| 12      | EDID Structure Ver.                            | 01    | 00000001 | 1     |      |
| 13      | EDID revision #                                | 04    | 00000100 | 4     |      |
| 14      | Video input def. (digital I/P, non-TMDS, CRGB) | 90    | 10010000 | 144   |      |

|    |   |    |          |     |
|----|---|----|----------|-----|
| 15 | Max H image size (rounded to cm)                      | 1A | 00011010 | 26  |
| 16 | Max V image size (rounded to cm)                      | 0E | 00001110 | 14  |
| 17 | Display Gamma $(=(\text{gamma} \times 100) - 100)$    | 78 | 01111000 | 120 |
| 18 | Feature support (no DPMS, Active OFF, RGB, tmg Blk#1) | 02 | 00000010 | 2   |
| 19 | Red/green low bits (Lower 2:2:2:2 bits)               | 99 | 10011001 | 153 |
| 1A | Blue/white low bits (Lower 2:2:2:2 bits)              | 85 | 10000101 | 133 |
| 1B | Red x (Upper 8 bits)                                  | 95 | 10010101 | 149 |
| 1C | Red y/ highER 8 bits                                  | 55 | 01010101 | 85  |
| 1D | Green x   | 56 | 01010110 | 86  |
| 1E | Green y   | 92 | 10010010 | 146 |
| 1F | Blue x  | 28 | 00101000 | 40  |
| 20 | Blue y  | 22 | 00100010 | 34  |
| 21 | White x   | 50 | 01010000 | 80  |
| 22 | White y   | 54 | 01010100 | 84  |
| 23 | Established timing 1                                  | 00 | 00000000 | 0   |
| 24 | Established timing 2                                  | 00 | 00000000 | 0   |
| 25 | Established timing 3                                  | 00 | 00000000 | 0   |
| 26 | Standard timing #1                                    | 01 | 00000001 | 1   |
| 27 |   | 01 | 00000001 | 1   |
| 28 | Standard timing #2                                    | 01 | 00000001 | 1   |
| 29 |   | 01 | 00000001 | 1   |
| 2A | Standard timing #3                                    | 01 | 00000001 | 1   |
| 2B |   | 01 | 00000001 | 1   |
| 2C | Standard timing #4                                    | 01 | 00000001 | 1   |
| 2D |   | 01 | 00000001 | 1   |
| 2E | Standard timing #5                                    | 01 | 00000001 | 1   |
| 2F |   | 01 | 00000001 | 1   |
| 30 | Standard timing #6                                    | 01 | 00000001 | 1   |
| 31 |   | 01 | 00000001 | 1   |
| 32 | Standard timing #7                                    | 01 | 00000001 | 1   |
| 33 |   | 01 | 00000001 | 1   |
| 34 | Standard timing #8                                    | 01 | 00000001 | 1   |
| 35 |   | 01 | 00000001 | 1   |
| 36 | Pixel Clock/10000 LSB                                 | CE | 11001110 | 206 |
| 37 | Pixel Clock/10000 USB                                 | 1D | 00011101 | 29  |
| 38 | Horz active Lower 8bits                               | 56 | 01010110 | 86  |
| 39 | Horz blanking Lower 8bits                             | E2 | 11100010 | 226 |
| 3A | HorzAct:HorzBlnk Upper 4:4 bits                       | 50 | 01010000 | 80  |
| 3B | Vertical Active Lower 8bits                           | 00 | 00000000 | 0   |
| 3C | Vertical Blanking Lower 8bits                         | 1E | 00011110 | 30  |
| 3D | Vert Act : Vertical Blanking (upper 4:4 bit)          | 30 | 00110000 | 48  |



|    |   |    |          |     |                      |
|----|---|----|----------|-----|----------------------|
| 3E | HorzSync. Offset  | 26 | 00100110 | 38  |                      |
| 3F | HorzSync.Width  | 16 | 00010110 | 22  |                      |
| 40 | VertSync.Offset : VertSync.Width                            | 36 | 00110110 | 54  |                      |
| 41 | Horz&Vert Sync Offset/Width <b>Upper 2bits</b>              | 00 | 00000000 | 0   |                      |
| 42 | Horizontal Image Size <b>Lower 8bits</b>                    | 00 | 00000000 | 0   |                      |
| 43 | Vertical Image Size <b>Lower 8bits</b>                      | 90 | 10010000 | 144 |                      |
| 44 | Horizontal & Vertical Image Size <b>(upper 4:4 bits)</b>    | 10 | 00010000 | 16  |                      |
| 45 | Horizontal Border <i>(zero for internal LCD)</i>            | 00 | 00000000 | 0   |                      |
| 46 | Vertical Border <i>(zero for internal LCD)</i>              | 00 | 00000000 | 0   |                      |
| 47 | Signal <i>(non-intr, norm, no stero, sep sync, neg pol)</i> | 18 | 00011000 | 24  |                      |
| 48 | Pixel Clock/10,000 (LSB)                                    | DF | 11011111 | 223 | 40Hz frame rate      |
| 49 | Pixel Clock/10,000 (MSB)                                    | 13 | 00010011 | 19  |                      |
| 4A | Horizontal Addressable Pixels, lower 8 bits                 | 56 | 01010110 | 86  |                      |
| 4B | Horizontal Blanking Pixels, lower 8 bits                    | E2 | 11100010 | 226 |                      |
| 4C | H Pixels, upper nibble : H Blanking, upper nibble           | 50 | 01010000 | 80  |                      |
| 4D | Vertical Addressable Lines, lower 8 bits                    | 00 | 00000000 | 0   |                      |
| 4E | Vertical Blanking Lines, lower 8 bits                       | 1E | 00011110 | 30  |                      |
| 4F | V lines, upper nibble : V blanking, upper nibble            | 30 | 00110000 | 48  |                      |
| 50 | Horizontal Front Porch, lower 8 bits                        | 26 | 00100110 | 38  |                      |
| 51 | Horizontal Sync Pulse, lower 8 bits                         | 16 | 00010110 | 22  |                      |
| 52 | V Front Porch, lower nibble : V Sync Pulse, lower nibble    | 36 | 00110110 | 54  |                      |
| 53 | VFP, 2 bits: VSP 2 bits: HFP 2 bits: HFP 2 bits             | 00 | 00000000 | 0   |                      |
| 54 | Horizontal Image Size in mm, lower 8 bits                   | 00 | 00000000 | 0   |                      |
| 55 | Vertical Image Size in mm, lower 8 bits                     | 90 | 10010000 | 144 |                      |
| 56 | H Image Size, upper nibble : V Image Size, upper nibble     | 10 | 00010000 | 16  |                      |
| 57 | Horizontal Border   | 00 | 00000000 | 0   |                      |
| 58 | Vertical Border   | 00 | 00000000 | 0   |                      |
| 59 | Bit Encode Sync Information                                 | 18 | 00011000 | 24  |                      |
| 5A | DC  | 00 | 00000000 | 0   | nVDPS<br>Reserved 00 |
| 5B | HTOTAL  | 00 | 00000000 | 0   |                      |
| 5C | HA  | 00 | 00000000 | 0   |                      |
| 5D | HBL   | 00 | 00000000 | 0   |                      |
| 5E | HFP   | 00 | 00000000 | 0   |                      |
| 5F | HFPe  | 00 | 00000000 | 0   |                      |
| 60 | HBP   | 00 | 00000000 | 0   |                      |
| 61 | HB  | 00 | 00000000 | 0   |                      |
| 62 | HSO   | 00 | 00000000 | 0   |                      |
| 63 | HS  | 00 | 00000000 | 0   |                      |
| 64 | VTOTAL  | 00 | 00000000 | 0   |                      |
| 65 | VA  | 00 | 00000000 | 0   |                      |

|    |   |    |          |     |                   |
|----|---|----|----------|-----|-------------------|
| 66 | VBL   | 00 | 00000000 | 0   |                   |
| 67 | VFP   | 00 | 00000000 | 0   |                   |
| 68 | VBP   | 00 | 00000000 | 0   |                   |
| 69 | VB  | 00 | 00000000 | 0   |                   |
| 6A | VSO   | 00 | 00000000 | 0   |                   |
| 6B | VS  | 00 | 00000000 | 0   |                   |
| 6C | Detail Timing Description #4                    | 00 | 00000000 | 0   | Header            |
| 6D | Flag  | 00 | 00000000 | 0   |                   |
| 6E | Reserved  | 00 | 00000000 | 0   |                   |
| 6F | For Brightness Table and Power Consumption      | 02 | 00000010 | 2   |                   |
| 70 | Flag  | 00 | 00000000 | 0   |                   |
| 71 | PWM % [7:0] @ Step 0                            | 0C | 00001100 | 12  | Brightness Table  |
| 72 | PWM % [7:0] @ Step 5                            | 33 | 00110011 | 51  |                   |
| 73 | PWM % [7:0] @ Step 10                           | F9 | 11111001 | 249 |                   |
| 74 | Nits [7:0] @ Step 0                             | 0A | 00001010 | 10  |                   |
| 75 | Nits [7:0] @ Step 5                             | 3C | 00111100 | 60  |                   |
| 76 | Nits [7:0] @ Step 10                            | 64 | 01100100 | 100 |                   |
| 77 | Panel Electronics Power @ 32x32 Chess Pattern = | 1F | 00011111 | 31  | Power Consumption |
| 78 | Backlight Power @ 60 nits =                     | 14 | 00010100 | 20  |                   |
| 79 | Backlight Power @ Step 10 =                     | 22 | 00100010 | 34  |                   |
| 7A | Nits @ 100% PWM Duty =                          | 6E | 01101110 | 110 |                   |
| 7B | Flag  | 20 | 00100000 | 32  |                   |
| 7C | Flag  | 20 | 00100000 | 32  |                   |
| 7D | Flag  | 20 | 00100000 | 32  |                   |
| 7E | Extension Flag                                  | 00 | 00000000 | 0   |                   |
| 7F | Checksum  | B6 | 10110110 | 182 |                   |