# Product Specification

AU OPTRONICS CORPORATION

**(  ) Preliminary Specifications**

**( V ) Final Specifications**

| Module | 11.6" HD 16:9 Color TFT-LCD with LED Backlight design |
|---|---|
| Model Name | B116XAN03.1 ( HW: 1 A ) |
| Note | *LED Backlight with driving circuit design* |

| Customer | Date |
|---|---|
| **Checked & Approved by** | **Date** |

Note: This Specification is subject to change without notice.

| Approved by | Date |
|---|---|
| Kevin KH Shen | 2012/12/10 |
| **Prepared by** | |
| Lanie Huang | 2012/12/10 |

**NBBU Marketing Division**
**AU Optronics corporation**

# Contents

# Record of Revision

| Version and Date | Page | Old description | New Description | Remark |
|---|---|---|---|---|
| 0.1_2012/3/15 | | First Edition for Customer | | |
| 0.2_2012/3/30 | 28, 5 | | Update Drawing/OD/Power | |
| 0.3_2012/5/2 | 28, 32 | | Update Drawing / EDID | |
| 0.4_2012/8/27 | 5 | Final Edition | Outline dimension update | |
| | 25 | | Update power ON/OFF Sequence | |
| | 30 | | Label/ Package update | |
| | 32 | | EDID update | |
| 0.5_2012/9/20 | 5 | | Luminance Uniformity | |
| 0.6_2012/12/10 | 30 | Shipping label (HW:0 A) | Shipping label (HW: 1 A) | 1. Ehance ESD Capaility 2. Cell tape開口加大 |
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# 1. Handling Precautions

1) Since front polarizer is easily damaged, pay attention not to scratch it.

2) Be sure to turn off power supply when inserting or disconnecting from input connector.

3) Wipe off water drop immediately. Long contact with water may cause discoloration or spots.

4) When the panel surface is soiled, wipe it with absorbent cotton or other soft cloth.

5) Since the panel is made of glass, it may break or crack if dropped or bumped on hard surface.

6) Since CMOS LSI is used in this module, take care of static electricity and insure human earth when handling.

7) Do not open nor modify the Module Assembly.

8) Do not press the reflector sheet at the back of the module to any directions.

9) At the insertion or removal of the Signal Interface Connector, be sure not to rotate nor tilt the Interface Connector of the TFT Module.

11) After installation of the TFT Module into an enclosure (Notebook PC Bezel, for example), do not twist nor bend the TFT Module even momentary. At designing the enclosure, it should be taken into consideration that no bending/twisting forces are applied to the TFT Module from outside.   Otherwise the TFT Module may be damaged.

12) Small amount of materials having no flammability grade is used in the LCD module. The LCD module should be supplied by power complied with requirements of Limited Power Source (IEC60950 or UL1950), or be applied exemption.

13) Disconnecting power supply before handling LCD modules, it can prevent electric shock, DO NOT TOUCH the electrode parts, cables, connectors and LED circuit part of TFT module that a LED light bar build in as a light source of back light unit. It can prevent electrostic breakdown.

## 2. General Description

B116XAN03 V1 is a Color Active Matrix Liquid Crystal Display composed of a TFT LCD panel, a driver circuit, and LED backlight system. The screen format is intended to support the 16:9 HD, 1366(H) x768(V) screen and 262k colors (RGB 6-bits data driver) with LED backlight driving circuit. All input signals are MIPI interface compatible.

B116XAN03 V1 is designed for a display unit of notebook style personal computer and industrial machine.

## 2.1 General Specification

The following items are characteristics summary on the table at 25 ℃ condition:

| Items | Unit | Specifications | | | |
|---|---|---|---|---|---|
| Screen Diagonal | [mm] | 293.83 (11.6W") | | | |
| Active Area | [mm] | 256.125 (H) x 144 (V) | | | |
| Pixels H x V | | 1366 x 3(RGB) x 768 | | | |
| Pixel Pitch | [mm] | 0.1875 X  0.1875 | | | |
| Pixel Format | | R.G.B. Vertical Stripe | | | |
| Display Mode | | Normally Black | | | |
| White Luminance | [cd/m$^2$] | 400 | | | |
| Luminance Uniformity | | 1.25 max. (5 points)<br>1.67   max (13 points) | | | |
| Contrast Ratio | | 800 typ. | | | |
| Response Time | [ms] | 35 Max | | | |
| Nominal Input Voltage VDD | [Volt] | +3.3 typ. | | | |
| Power Consumption | [Watt] | 0.90W Max (Logic)<br>2.31W Max (B/L) | | | |
| Weight | [Grams] | 170 max. (W/O Digitizer) | | | |
| Physical Size (panel only) | [mm] | | Min. | Typ. | Max. |
| | | Length | 269.87 | 270.37 | 270.87 |
| | | Width | 159.29 | 159.79 | 160.29 |
| | | Thickness | --- | --- | 4.8 |

| Electrical Interface | | MIPI |
|---|---|---|
| Surface Treatment | | Anti-Glare |
| Support Color | | 262K colors ( RGB 6-bit ) |
| Temperature Range<br>Operating<br>Storage (Non-Operating) | [$^{o}$C]<br>[$^{o}$C] | 0 to +50<br>-20 to +60 |
| RoHS Compliance | | RoHS Compliance |

## 2.2 Optical Characteristics

The optical characteristics are measured under stable conditions at 25℃ (Room Temperature) :

| Item | | Symbol | Conditions | Min. | Typ. | Max. | Unit | Note |
|---|---|---|---|---|---|---|---|---|
| White Luminance | | | 5 points average | 340 | 400 | --- | cd/m$^2$ | 1, 4, 5. |
| Viewing Angle | | $\theta_R$<br>$\theta_L$ | Horizontal (Right)<br>CR = 10 (Left) | ---<br> | 85<br>85 | ---<br> | degree | 4, 9 |
| | | $\psi_H$<br>$\psi_L$ | Vertical (Upper)<br>CR = 10 (Lower) | ---<br> | 85<br>85 | ---<br> | | |
| Luminance Uniformity | | $\delta_{5P}$ | 5 Points | --- | --- | 1.25 | | 1, 3, 4 |
| Luminance Uniformity | | $\delta_{13P}$ | 13 Points | --- | --- | 1.67 | | 2, 3, 4 |
| Contrast Ratio | | CR | | --- | 800 | --- | | 4, 6 |
| Cross talk | | % | | --- | --- | 4 | | 4, 7 |
| Response Time | | $T_{RT}$ | Rising + Falling | --- | 25 | 35 | msec | 4, 8 |
| Color /<br>Chromaticity<br>Coordinates | Red | Rx | CIE 1931 | 0.559 | 0.589 | 0.619 | | 4 |
| | | Ry | | 0.307 | 0.337 | 0.367 | | |
| | Green | Gx | | 0.299 | 0.329 | 0.359 | | |
| | | Gy | | 0.558 | 0.588 | 0.618 | | |
| | Blue | Bx | | 0.126 | 0.156 | 0.186 | | |
| | | By | | 0.098 | 0.128 | 0.158 | | |
| | White | Wx | | 0.283 | 0.313 | 0.343 | | |
| | | Wy | | 0.299 | 0.329 | 0.359 | | |
| NTSC | | % | | - | 50 | - | | |

**Note 1**: 5 points position (Ref: Active area)
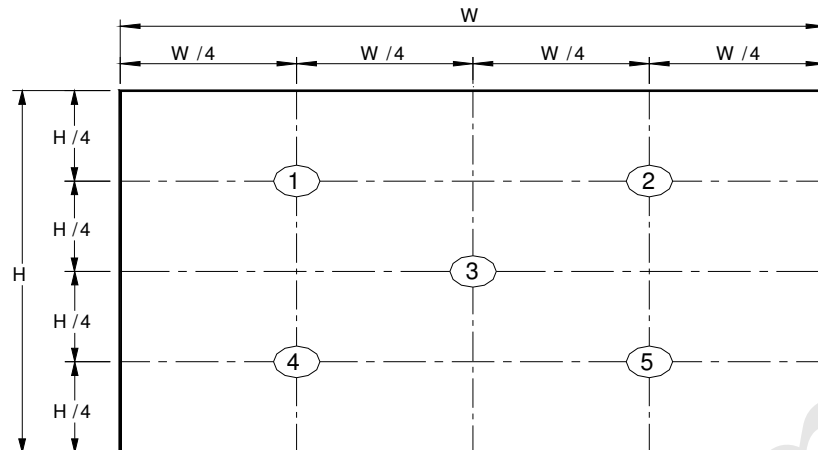


**Note 2**: 13 points position (Ref: Active area)
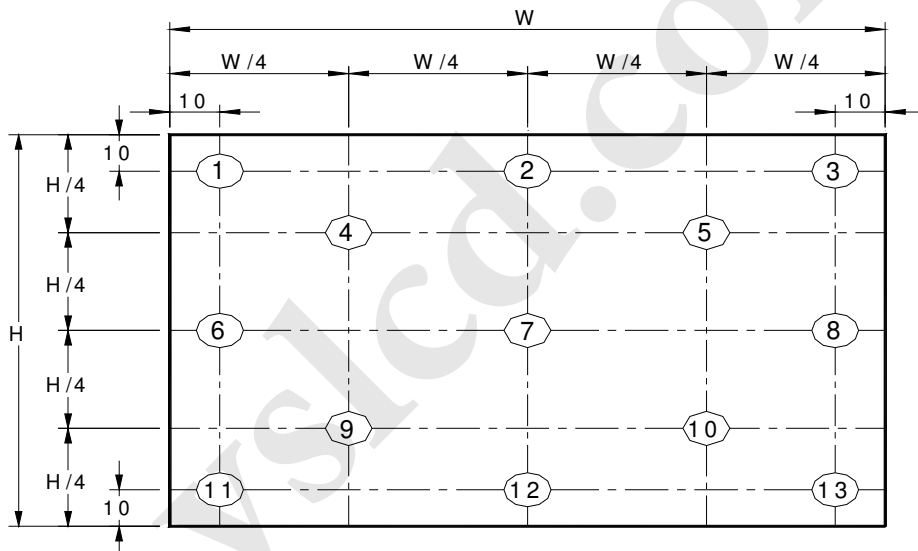


**Note 3**: The luminance uniformity of 5 or13 points is defined by dividing the maximum luminance values by the minimum test point luminance

$$\delta_{W5} = \frac{\text{Maximum Brightness of five points}}{\text{Minimum Brightness of five points}}$$

$$\delta_{W13} = \frac{\text{Maximum Brightness of thirteen points}}{\text{Minimum Brightness of thirteen points}}$$

**Note 4**: Measurement method

The LCD module should be stabilized at given temperature for 30 minutes to avoid abrupt temperature change during

measuring. In order to stabilize the luminance, the measurement should be executed after lighting Backlight for 30 minutes in a stable, windless and dark room, and it should be measured in the center of screen.

Photo detector

Field=2°

50 cm

LCD Panel

TFT-LCD Module

Center of the screen
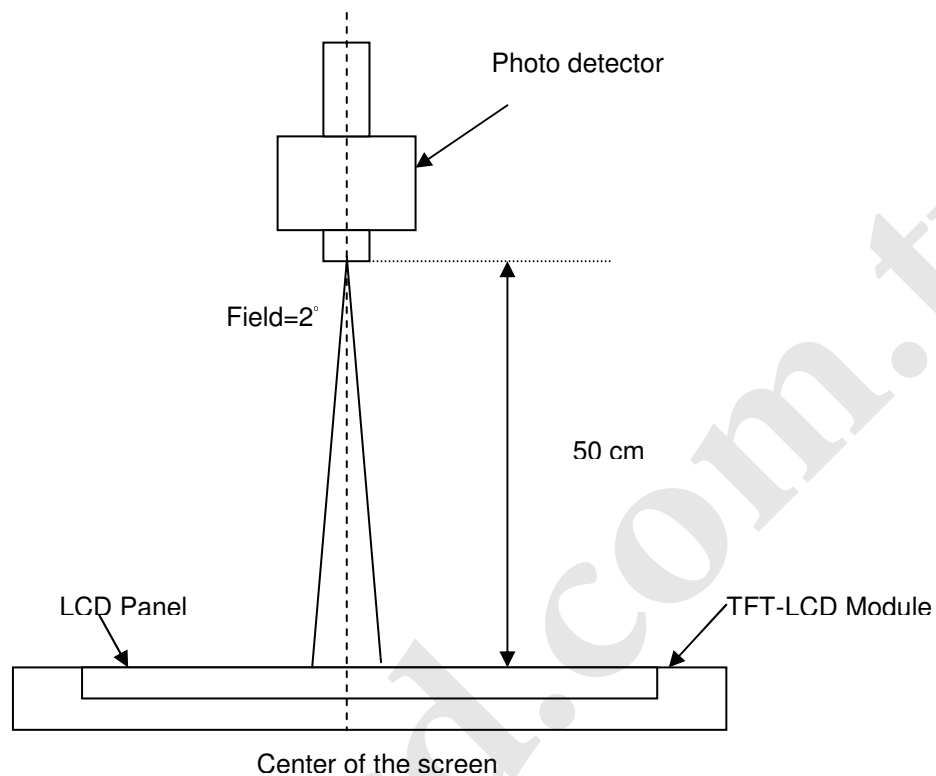
**Note 5**： Definition of Average Luminance of White ($Y_L$):

Measure the luminance of gray level 63 at 5 points，$Y_L$ = [L (1)+ L (2)+ L (3)+ L (4)+ L (5)] / 5

L (x) is corresponding to the luminance of the point X at Figure in Note (1).

**Note 6**： Definition of contrast ratio:

Contrast ratio is calculated with the following formula.

$$\text{Contrast ratio (CR)} = \frac{\text{Brightness on the "White" state}}{\text{Brightness on the "Black" state}}$$
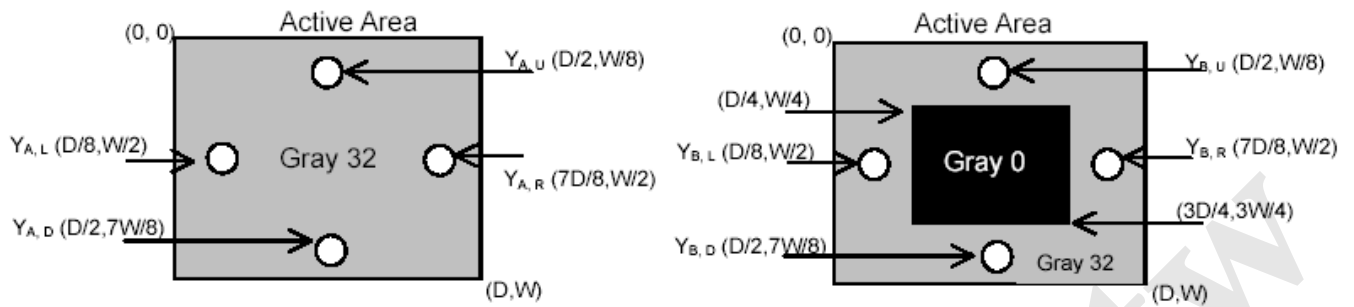
**Note 7**： Definition of Cross Talk (CT)

$$CT = | Y_B - Y_A | / Y_A \times 100 \ (\%)$$

Where

$Y_A$ = Luminance of measured location without gray level 0 pattern (cd/m2)

$Y_B$ = Luminance of measured location with gray level 0 pattern (cd/m2)

**Note 8**: Definition of response time:

The output signals of BM-7 or equivalent are measured when the input signals are changed from "Black" to "White" (falling time) and from "White" to "Black" (rising time), respectively. The response time interval between the 10% and 90% of amplitudes. Refer to figure as below.
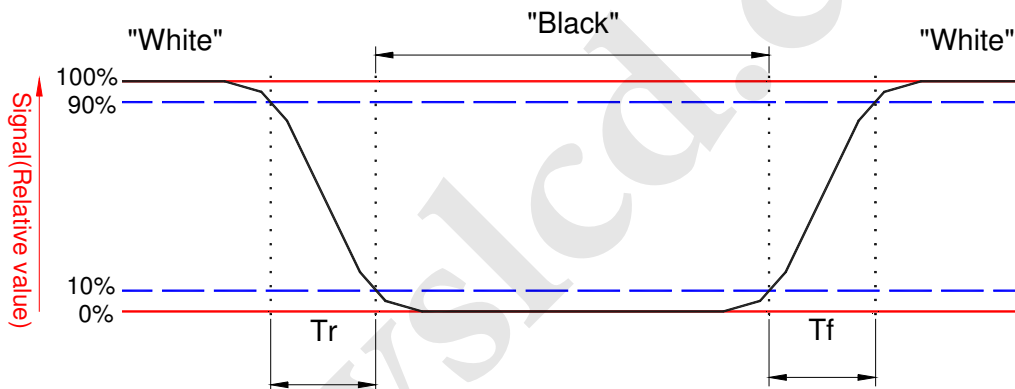
**Note 9**. Definition of viewing angle

Viewing angle is the measurement of contrast ratio $\geqq$ 10, at the screen center, over a 180° horizontal and 180° vertical range (off-normal viewing angles). The 180° viewing angle range is broken down as follows; 90° (θ) horizontal left and right and 90° (Φ) vertical, high (up) and low (down). The measurement direction is typically perpendicular to the display surface with the screen rotated about its center to develop the desired measurement viewing angle.
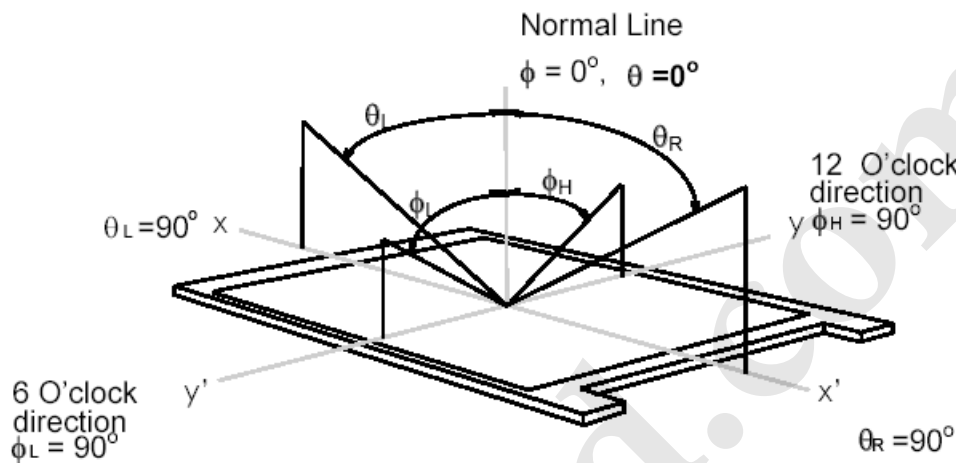
# 3. Functional Block Diagram

The following diagram shows the functional block of the 11.6 inches wide Color TFT/LCD 40 Pin one channel Module
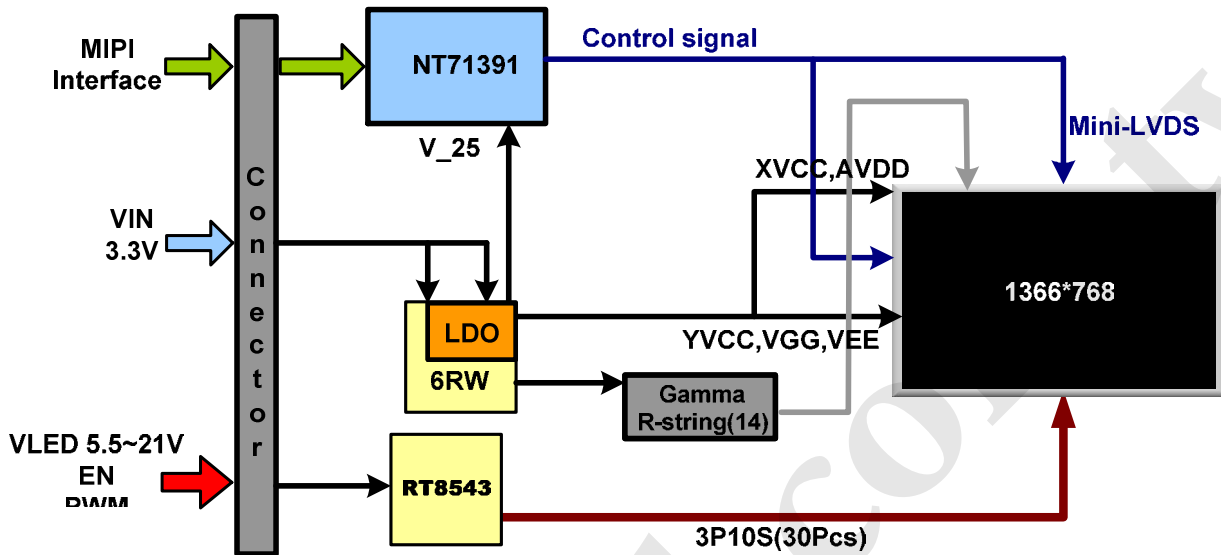
## 4. Absolute Maximum Ratings

An absolute maximum rating of the module is as following:

### 4.1 Absolute Ratings of TFT LCD Module

| Item | Symbol | Min | Max | Unit | Conditions |
|------|--------|-----|-----|------|------------|
| Logic/LCD Drive Voltage | Vin | -0.3 | +4.0 | [Volt] | Note 1,2 |

### 4.3 Absolute Ratings of Environment

| Item | Symbol | Min | Max | Unit | Conditions |
|------|--------|-----|-----|------|------------|
| Operating Temperature | TOP | 0 | 50 | [$^{o}$C] | Note 4 |
| Operation Humidity | HOP | 5 | 95 | [%RH] | Note 4 |
| Storage Temperature | TST | -20 | +60 | [$^{o}$C] | Note 4 |
| Storage Humidity | HST | 5 | 95 | [%RH] | Note 4 |

Note 1: At Ta (25℃ )

Note 2: Permanent damage to the device may occur if exceed maximum values

Note 3: LED specification refer to section 5.2

Note 4: For quality performance, please refer to AUO IIS (Incoming Inspection Standard).
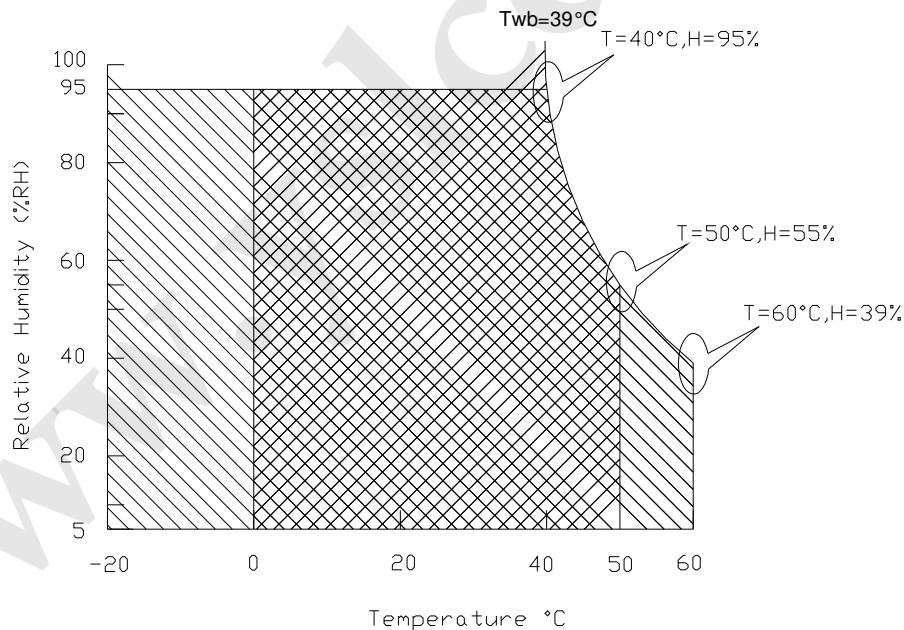
Operating Range    Storage Range

# 5. Electrical Characteristics

## 5.1 TFT LCD Module

### 5.1.1 Power Specification

Input power specifications are as follows;

The power specification are measured under 25℃ and frame frenquency under 60Hz

| Symble | Parameter | Min | Typ | Max | Units | Note |
|--------|-----------|-----|-----|-----|-------|------|
| VDD | Logic/LCD Drive Voltage | 3.0 | 3.3 | 3.6 | [Volt] | |
| PDD | VDD Power | - | - | 0.9 | [Watt] | Note 1 |
| IDD | IDD Current | - | - | 300 | [mA] | Note 1 |
| IRush | Inrush Current | - | - | 2000 | [mA] | Note 2 |
| VDDrp | Allowable Logic/LCD Drive Ripple Voltage | - | - | 100 | [mV] p-p | |

Note 1 : Maximum Measurement Condition：White Pattern at 3.3V driving voltage. ($P_{max}=V_{3.3} \times I_{white}$)

Note 2：Measure Condition
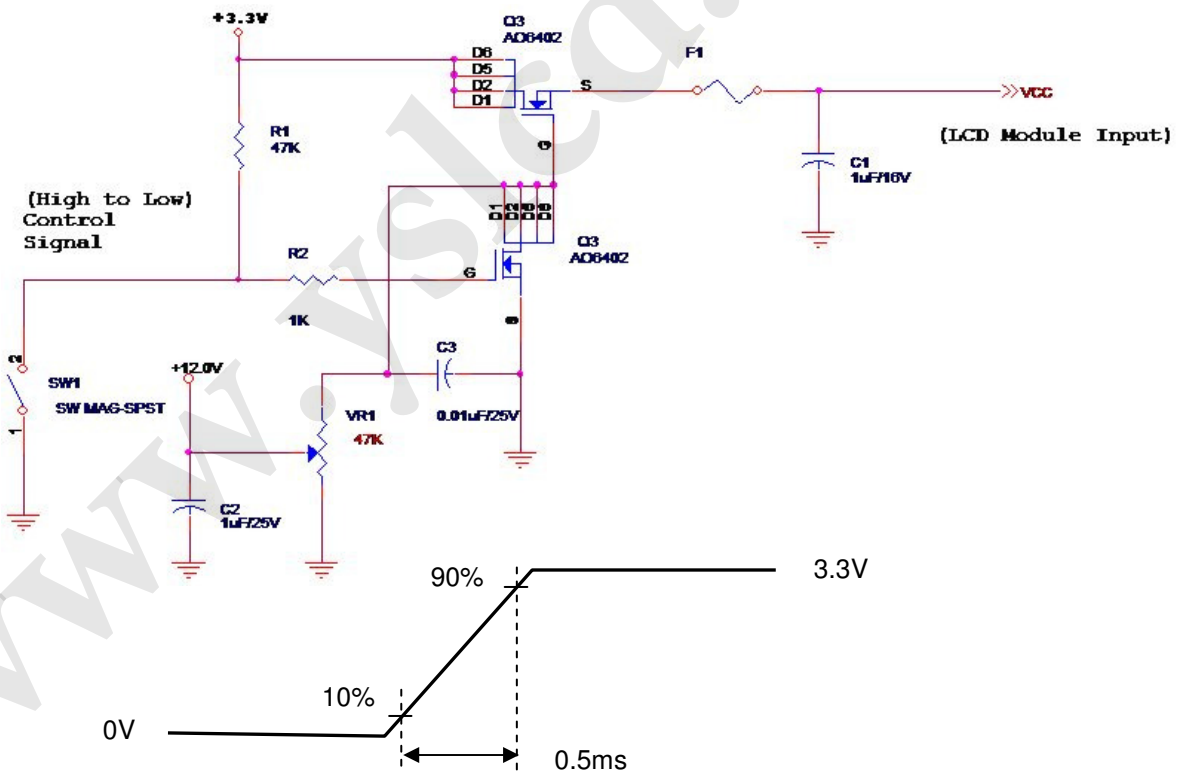


**Vin rising time**

**5.1.2 Signal Electrical Characteristics**

Input signals shall be low or High-impedance state when VDD is off.

MIPI DC/AC Characteristics are as follows;

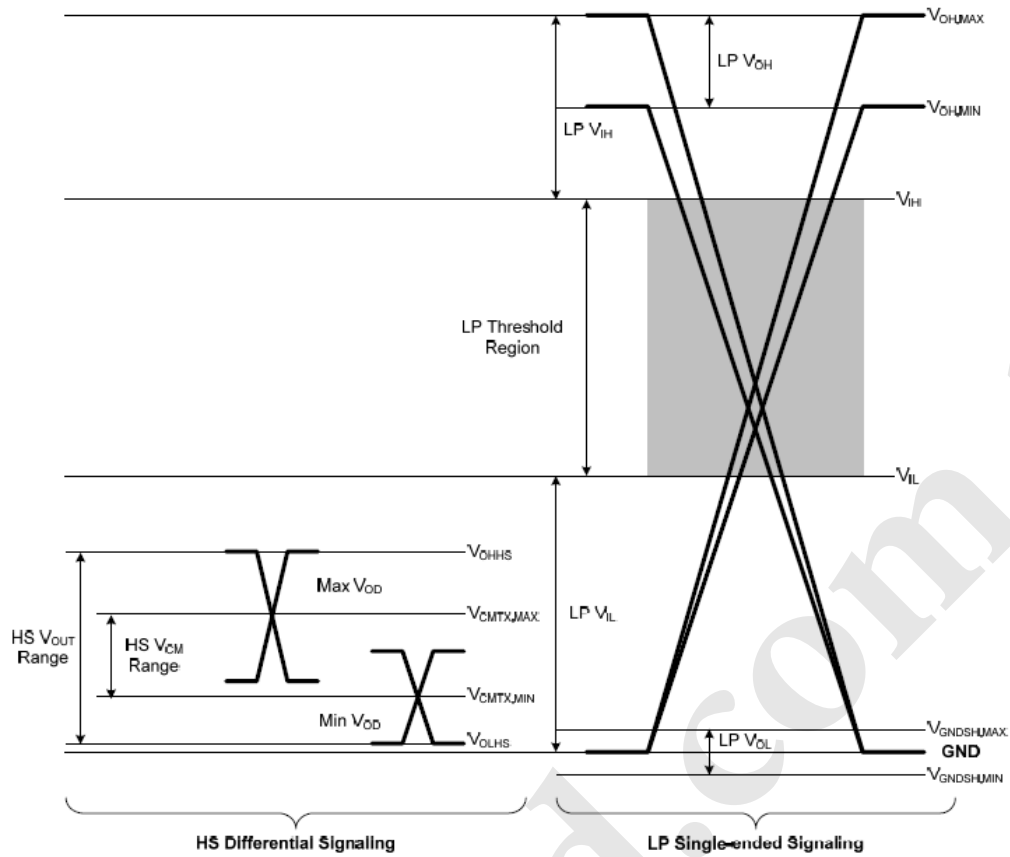| MIPI Receiver Differential Input (DC Characteristics) | | | | | |
|---|---|---|---|---|---|
| Symbol | Parameter | Min | Typ | Max | Unit |
| $BR_{MIPI}$ | Input data bit rate | 200 | - | 1000 | Mbps |
| $V_{CMRX}$ | Common-mode voltage(HS Rx mode) | 70 | - | 330 | mV |
| $V_{IDTH}$ | Differential input high threshold (HS Rx mode) | - | - | 70 | mV |
| $V_{IDTL}$ | Differential input low threshold (HS Rx mode) | -70 | - | - | mV |
| $|V_{IDM}|$ | Differential input voltage range (HS Rx mode) | 70 | - | 500 | mV |
| $V_{IHHS}$ | Single-end input high voltage (HS Rx mode) | - | - | 460 | mV |
| $V_{ILHS}$ | Single-end input low voltage (HS Rx mode) | -40 | - | - | mV |
| $Z_{ID}$ | Differential input impedance | 80 | 100 | 125 | $\Omega$ |
| $V_{IHLP}$ | Logic 1 input voltage (LP Rx mode) | 880 | | | mV |
| $V_{ILLP}$ | Logic 0 input voltage (LP Rx mode) | | | 550 | mV |
| $V_{OH}$ | Output high level (LP Tx mode) | 1.08 | 1.2 | 1.32 | V |
| $V_{OL}$ | Output low level (LP Tx mode) | -50 | | 50 | mV |

| MIPI Receiver Differential Input (AC Characteristics) | | | | | | |
|---|---|---|---|---|---|---|
| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
| $\Delta V_{CMRX(HF)}$ | Common-mode interference beyond 450MHz | | - | - | 100 | mV |
| $\Delta V_{CMRX(LF)}$ | Common-mode interference 50MHz ~ 450MHz | | -50 | - | 50 | mV |
| $C_{CM}$ | Common-mode termination | | - | - | 60 | pF |
| $UI_{INST}$ | UI instantaneous | | 1 | | 12.5 | ns |

HS RX Scheme
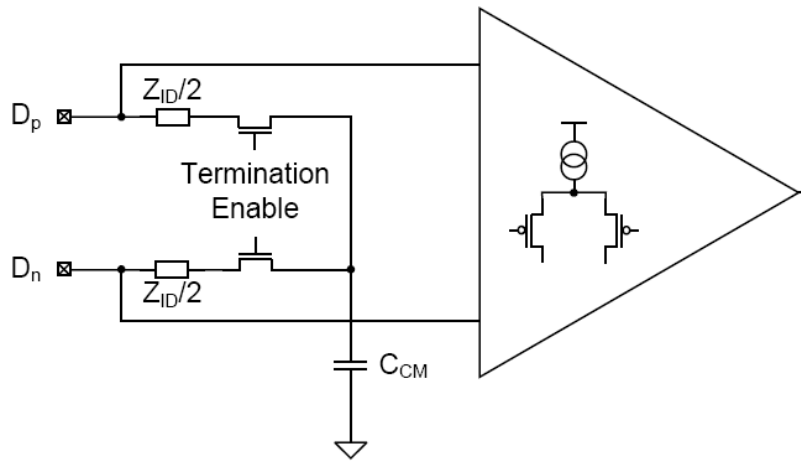
| Symbol | Parameter | Min | Typ | Max | Unit | Notes |
|---|---|---|---|---|---|---|
| $T_{SKEW[TX]}$ | Data to Clock Skew (mesured at transmitter) | -0.15 | | 0.15 | $UI_{INST}$ | 1 |
| $T_{SETUP[RX]}$ | Data to Clock Setup Time (receiver) | 0.15 | | | $UI_{INST}$ | 2 |
| $T_{HOLD[RX]}$ | Data to Clock Hold Time (receiver) | 0.15 | | | $UI_{INST}$ | 2 |

Note:

1. Total silicon and package delay budget of $0.3*UI_{INST}$

2. Total setup and hold window for receiver of $0.3*UI_{INST}$

High Speed Data Transmission: Data to Clock Timing
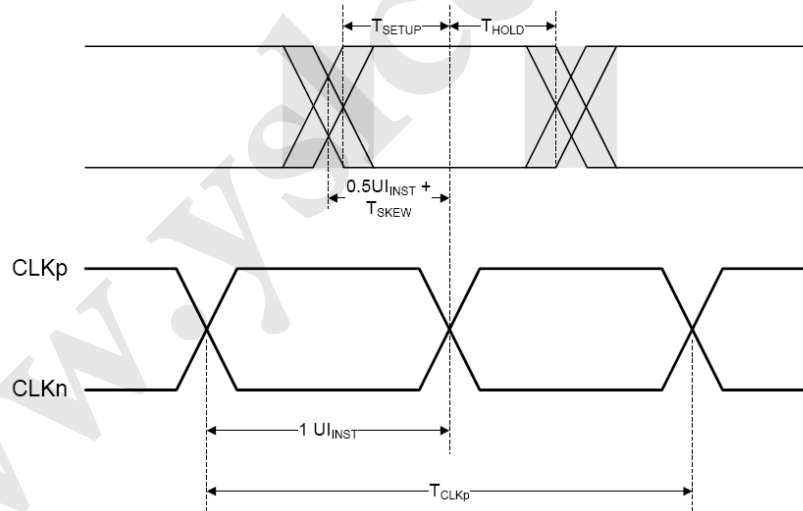


| LP Receiver AC Specifications | | | | | | |
|---|---|---|---|---|---|---|
| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
| $e_{SPIKE}$ | Input pulse rejection | | - | - | 300 | V · ps |
| $T_{MIN-RX}$ | Minimum pulse width response | | 50 | - | - | ns |

| | | | | | | |
|---|---|---|---|---|---|---|
| $V_{INT}$ | Peak interference amplitude | | - | - | 200 | mV |
| $f_{INT}$ | Interference frequency | | 450 | - | - | MHz |

Input Glitch Rejection of Low-Power Receivers
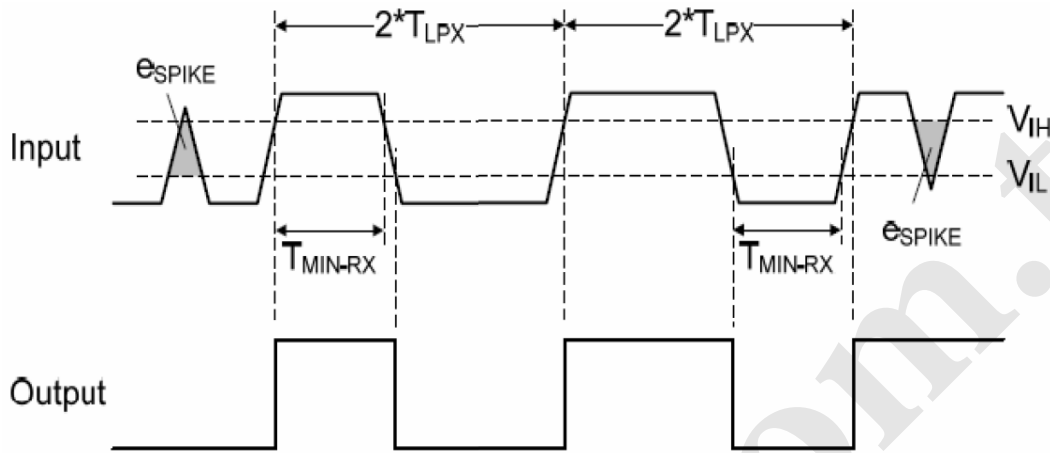


For MIPI data transmission from TX to TCON works properly in video mode, it is suggested that all of MIPI lanes status follow the scheme showed in below. When power is turned on, all lanes (include clock lane) are into LP-11 status first. When TX wants to start transmitting data to TCON, the clock lane is into HS and start toggling. Then data lanes are into HS and data are transmitted. After data transmissions are finished (ex. H-blanking, V-blanking), the data lanes are returned to LP-11, then clock lane, too. The transmission start from LP-11 and stop in LP-11 on all lanes (include clock lane) are the recommended proper operation sequence for MIPI video mode.
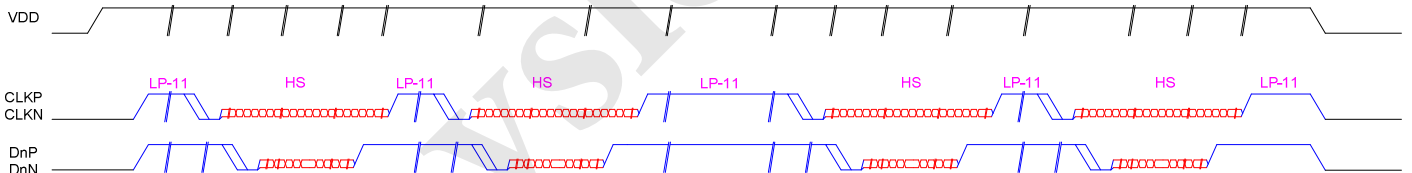


The timing definitions are listed in below,

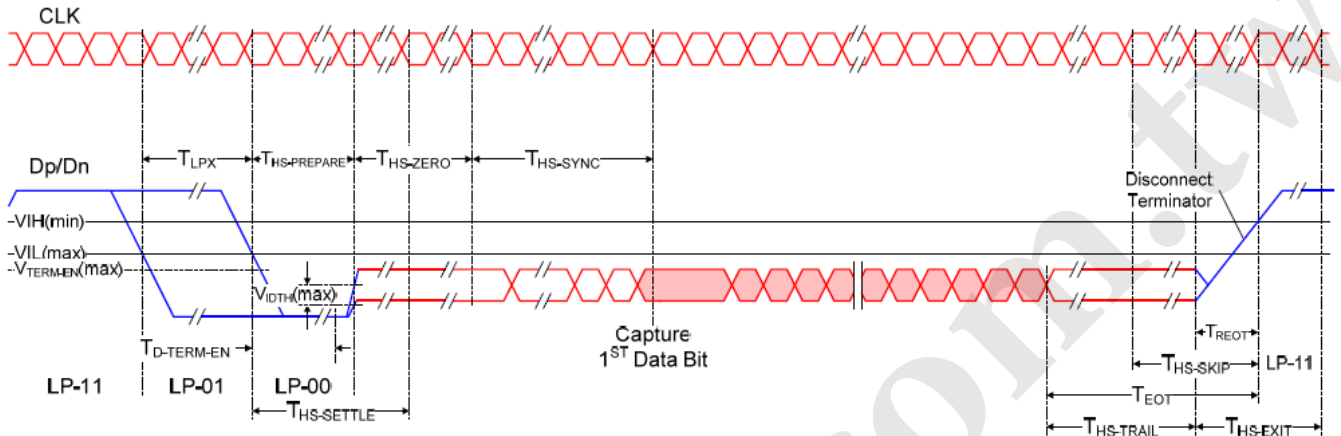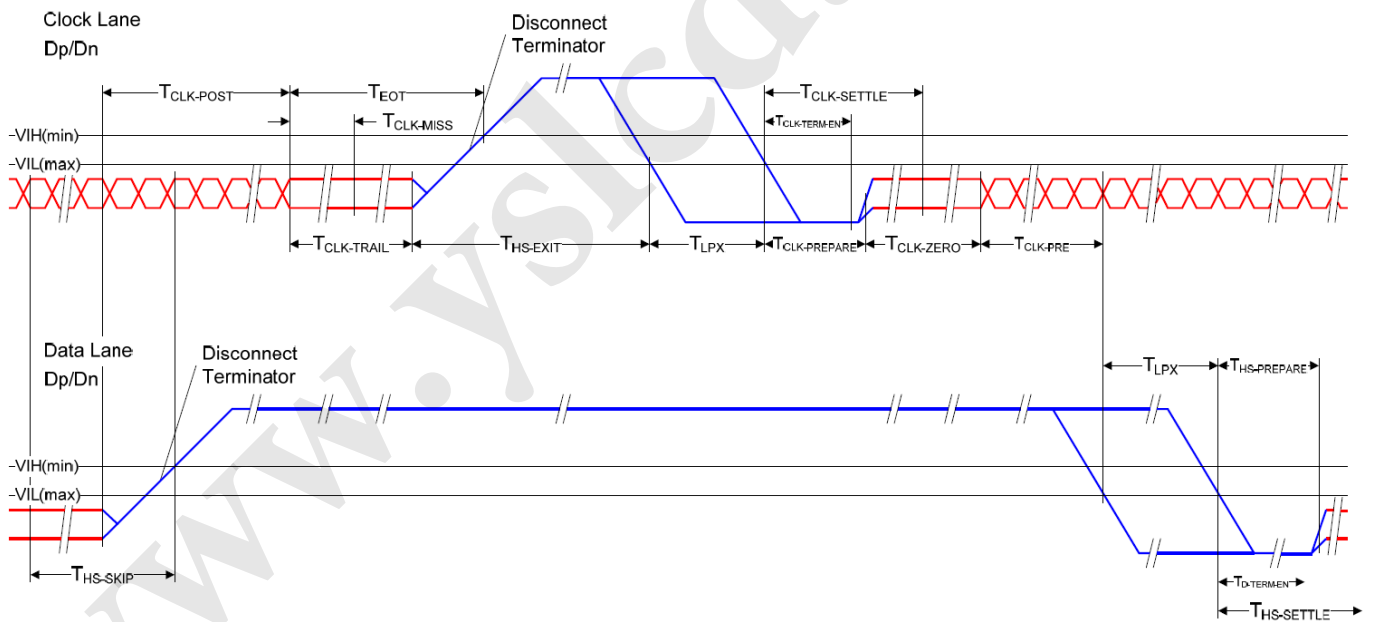| Parameter | Description | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| TCLK-MISS | Timeout for receiver to detect absence of Clock transitions and disable the Clock Lane HS-RX. | | | 60 | ns |
| TCLK-POST | Time that the transmitter continues to send HS clock after the last associated Data Lane has transitioned to LP Mode. Interval is defined as the period from the end of THS-TRAIL to the beginning of TCLK-TRAIL. | 60 ns + 52*UI | | | ns |
| TCLK-PRE | Time that the HS clock shall be driven by the transmitter prior to any associated Data Lane beginning the transition from LP to HS mode. | 8 | | | UI |

| | | | | | |
|---|---|---|---|---|---|
| TCLK-PREPARE | Time that the transmitter drives the Clock Lane LP-00 Line state immediately before the HS-0 Line state starting the HS transmission. | 38 | | 95 | ns |
| TCLK-SETTLE | Time interval during which the HS receiver shall ignore any Clock Lane HS transitions, starting from the beginning of TCLK-PREPARE. | 95 | | 300 | ns |
| TCLK-TERM-EN | Time for the Clock Lane receiver to enable the HS line termination, starting from the time point when Dn crosses VIL,MAX. | | | 38 | ns |
| TCLK-TRAIL | Time that the transmitter drives the HS-0 state after the last payload clock bit of a HS transmission burst. | 60 | | | ns |
| TCLK-PREPARE + TCLK-ZERO | TCLK-PREPARE + time that the transmitter drives the HS-0 state prior to starting the Clock. | 300 | | | ns |
| TD-TERM-EN | Time for the Data Lane receiver to enable the HS line termination, starting from the time point when Dn crosses VIL,MAX. | | | 35 ns + 4*UI | ns |
| TEOT | Transmitted time interval from the start of THS-TRAIL or TCLK-TRAIL, to the start of the LP-11 state following a HS burst. | | | 105 ns + 12*UI | ns |
| THS-EXIT | Time that the transmitter drives LP-11 following a HS burst. | 100 | | | ns |
| THS-SYNC | HS Sync-Sequence '00011101' period | | 8 | | UI |
| THS-PREPARE | Time that the transmitter drives the Data Lane LP-00 Line state immediately before the HS-0 Line state starting the HS transmission | 40 ns + 4*UI | | 85 ns + 6*UI | ns |
| THS-PREPARE + THS-ZERO | THS-PREPARE + time that the transmitter drives the HS-0 state prior to transmitting the Sync sequence. | 145 ns + 10*UI | | | ns |
| THS-SETTLE | Time interval during which the HS receiver shall ignore any Data Lane HS transitions, starting from the beginning of THS-PREPARE. | 85 ns + 6*UI | | 145 ns + 10*UI | ns |
| THS-SKIP | Time interval during which the HS-RX should ignore any transitions on the Data Lane, following a HS burst. The end point of the interval is defined as the beginning of the LP-11 state following the HS burst. | 40 | | 55 ns + 4*UI | ns |
| THS-TRAIL | Time that the transmitter drives the flipped differential state after last payload data bit of a HS transmission burst | 60 ns + 4*UI | | | ns |
| TLPX | Transmitted length of any Low-Power state period | 50 | | | ns |
| Ratio TLPX | Ratio of TLPX(MASTER)/TLPX(SLAVE) between Master and Slave side | 2/3 | | 3/2 | |
| TTA-GET | Time that the new transmitter drives the Bridge state (LP-00) after accepting control during a Link Turnaround. | | 5*TLPX | | ns |
| TTA-GO | Time that the transmitter drives the Bridge state (LP-00) before releasing control during a Link Turnaround. | | 4*TLPX | | ns |
| TTA-SURE | Time that the new transmitter waits after the LP-10 state before transmitting the Bridge state (LP-00) during a Link Turnaround. | TLPX | | 2*TLPX | ns |

Note:

1. The minimum value depends on the bit rate. Implementations should ensure proper operation for all the supported bit rates.

2. TLPX is an internal state machine timing reference. Externally measured values may differ slightly from the specified values due to asymmetrical rise and fall times.

High-Speed Data Transmission in Bursts



Switching the Clock Lane between Clock Transmission and Low-Power Mode



Turnaround Procedure

**5.2 Backlight Unit**

### 5.2.1 LED characteristics

| Parameter | Symbol | Min | Typ | Max | Units | Condition |
|---|---|---|---|---|---|---|
| Backlight Power Consumption | PLED | - | - | 2.31 | [Watt] | (Ta=25℃@400nits) |
| LED Life-Time | N/A | 10,000 | - | - | Hour | (Ta=25℃@400nit) Note1. |
| LED Forward Voltage | VF | 2.8 | 3.0 | 3.3 | [Volt] | (Ta=25℃) |
| LED Forward Voltage of every LED string | VF-string | - | 30 | 33 | [Volt] | (Ta=25℃) Note2. |
| LED Forward Current | IF | - | 20 | - | [mA] | (Ta=25℃) |

**Note 1.** The LED life-time define as the estimated time to 50% degradation of initial luminous.

**Note 2.** Every LED string consists of 10 pcs LED chip

**Note 3.** LED input Current 0.424A max / LED Forward Current 20mA per string, total 60mA / LED Forward Voltage 33V typ / LED Array 3parallel * 10series

**Note 4.** LED driver IC Vender - Richtek

# 6. Signal Interface Characteristic

## 6.1 Pixel Format Image

Following figure shows the relationship of the input signals and LCD pixel format.

## 6.2 The Input Data Format

Input Pixel Stream Format (1366RGB in 4 Lanes with RGB 8-8-8 format)

| LANE 0 | LPS | SoT | Data ID | R1 | G2 | B3 | - - - - | G1362 | B1363 | R1365 | G1366 | EoT | LPS |
| LANE 1 | LPS | SoT | Word Count (0~7) | G1 | B2 | R4 | - - - - | B1362 | R1364 | G1365 | B1366 | EoT | LPS |
| LANE 2 | LPS | SoT | Word Count (8~15) | B1 | R3 | G4 | - - - - | R1363 | G1364 | B1365 | Checksum (8~15) | EoT | LPS |
| LANE 3 | LPS | SoT | ECC | R2 | G3 | B4 | - - - - | G1363 | B1364 | R1366 | Checksum (8~15) | EoT | LPS |

LPS : Low Power State
SoT : Start of Transmission
EoT : End of Transmission
ECC : Error-Correcting Code

# 6.3 Integration Interface Requirement

## 6.3.1 MIPI Connector Description

Physical interface is described as for the connector on module.

These connectors are capable of accommodating the following signals and will be following components.

| Connector Name / Designation | For Signal Connector |
|---|---|
| Manufacturer | DDK |
| Type / Part Number | FF12-40A-R12BN-D3 |
| Mating Housing/Part Number | FPC Cable |

## 6.3.2 MIPI Pin Assignment

MIPI is a differential signal technology for LCD interface and high speed data transfer device.

| No. | Pin Name | I/O | Power Rail | Description |
|---|---|---|---|---|
| 1 | VDD | P | VDD | Power Supply +3.3V |
| 2 | VDD | P | VDD | Power Supply +3.3V |
| 3 | VDD | P | VDD | Power Supply +3.3V |
| 4 | NC | -- | -- | Not Connection |
| 5 | SDA | I/O | IOVDD | EDID Data Input |
| 6 | SCL | I/O | IOVDD | EDID Clock Input |
| 7 | GND | G | GND | Ground |
| 8 | GND | G | GND | Ground |
| 9 | NC | -- | -- | Not Connection |
| 10 | LEDPWM | I | IOVDD | Backlight LED driver PWM Input |
| 11 | LED_EN | I | IOVDD | LED Enable Input |
| 12 | NC | -- | -- | Not Connection |
| 13 | BIST | I | -- | LCD Panel Self Test Enable |
| 14 | NC | -- | -- | Not Connection |
| 15 | GND | G | GND | MDDI data positive signal |
| 16 | DSI_D2P/Rx-IN2P | I | MIPI | MIPI data pair 2 positive signal |
| 17 | DSI_D2N/Rx-IN2N | I | MIPI | MIPI data pair 2 negative signal |
| 18 | GND | G | GND | Ground |
| 19 | DSI_D1P/Rx-IN1P | I | MIPI | MIPI data pair 1 positive signal |
| 20 | DSI_D1N/Rx-IN1N | I | MIPI | MIPI data pair 1 negative signal |
| 21 | GND | G | GND | Ground |
| 22 | DSI_CLKP/Rx-CLKP | I | MIPI | MIPI Clock positive signal |
| 23 | DSI_CLKN/Rx-CLKN | I | MIPI | MIPI Clock negative signal |
| 24 | GND | G | GND | Ground |

| 25 | DSI_D0P/Rx-IN0P | I/O | MIPI | MIPI data pair 0 positive signal |
|----|-----------------|-----|------|----------------------------------|
| 26 | DSI_D0N/Rx-IN0N | I/O | MIPI | MIPI data pair 0 negative signal |
| 27 | GND | G | GND | Ground |
| 28 | DSI_D3P/Rx-IN3P | I | MIPI | MIPI data pair 3 positive signal |
| 29 | DSI_D3NRx-IN3N | I | MIPI | MIPI data pair 3 negative signal |
| 30 | GND | G | GND | Ground |
| 31 | NC | -- | -- | Not Connection |
| 32 | LED- | G | -- | LED Ground |
| 33 | LED- | G | -- | LED Ground |
| 34 | LED- | G | -- | LED Ground |
| 35 | LED- | G | -- | LED Ground |
| 36 | NC | -- | -- | Not Connection |
| 37 | LED+ | P | -- | LED Power Supply |
| 38 | LED+ | P | -- | LED Power Supply |
| 39 | LED+ | P | -- | LED Power Supply |
| 40 | LED+ | P | -- | LED Power Supply |

## 6.4 MIPI Interface Timing

### 6.4.1 Timing Characteristics
Basically, interface timings should match the 1366x768 /60Hz manufacturing guide line timing.

| Parameter | | Symbol | Min. | Typ. | Max. | Unit |
|-----------|---|--------|------|------|------|------|
| Frame Rate | | --- | --- | 60 | --- | Hz |
| Clock frequency | | $1/T_{Clock}$ | 67.3 | 70.7 | 80.5 | MHz |
| Vertical Section | Period | $T_V$ | 784 | 790 | 862 | $T_{Line}$ |
| | Active | $T_{VD}$ | | 768 | | |
| | Blanking | $T_{VB}$ | 16 | 22 | 94 | |
| Horizontal Section | Period | $T_H$ | 1430 | 1490 | 1557 | $T_{Clock}$ |
| | Active | $T_{HD}$ | | 1366 | | |
| | Blanking | $T_{HB}$ | 64 | 124 | 191 | |

Note : 1. DE mode only
    2. Clock frequency number is for reference, real setting value refer to EDID (Clock frequency 70.7MHz)

## 6.4.2 Timing diagram

**Input Timing Definition ( DE Mode )**

DOTCLK

$T_{CLOCK}$

Input Data

Invalid Data | Pixel 1 | Pixel 2 | Pixel 3 | Pixel N-1 | Pixel N | Invalid Data | Pixel 1

DE

$T_{HB}$ | $T_{HD}$

$T_H$

DE

$T_{VB}$ | $T_{VD}$

$T_V$
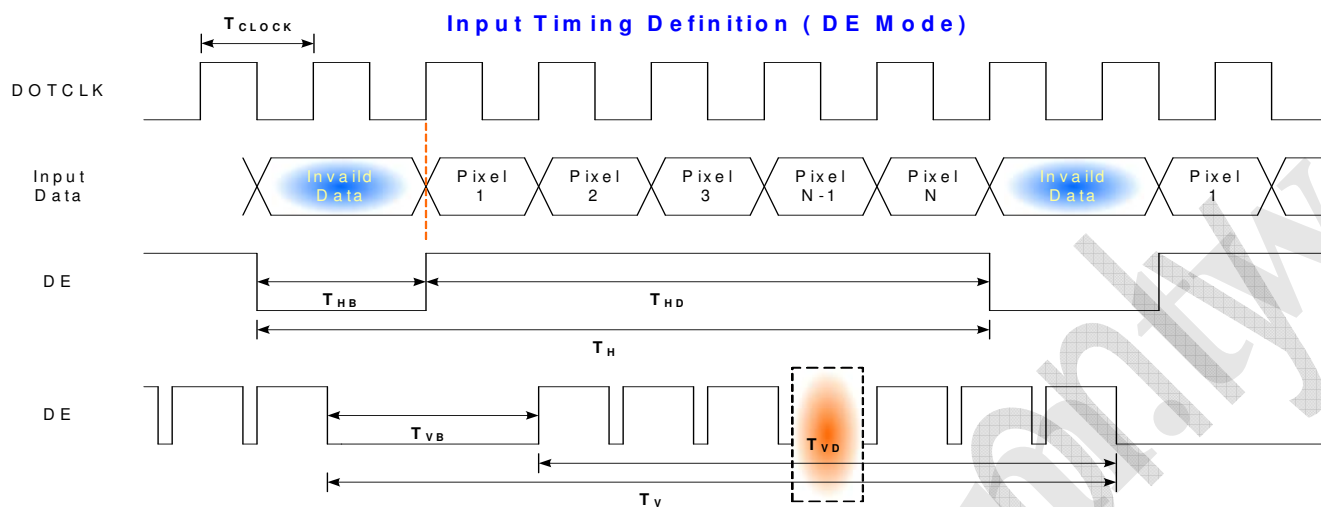
# 6.5 Power ON/OFF Sequence
Power on/off sequence is as follows. Interface signals and LED on/off sequence are also shown in the chart.

VIN
Power supply VDD(3.3V)

MIPI interface
(Data & Clock)

VEN
(LED Driver enable)

VPWM
(PWM for LED dimming)

VLED
(Backlight power supply)
(Hot Plug)
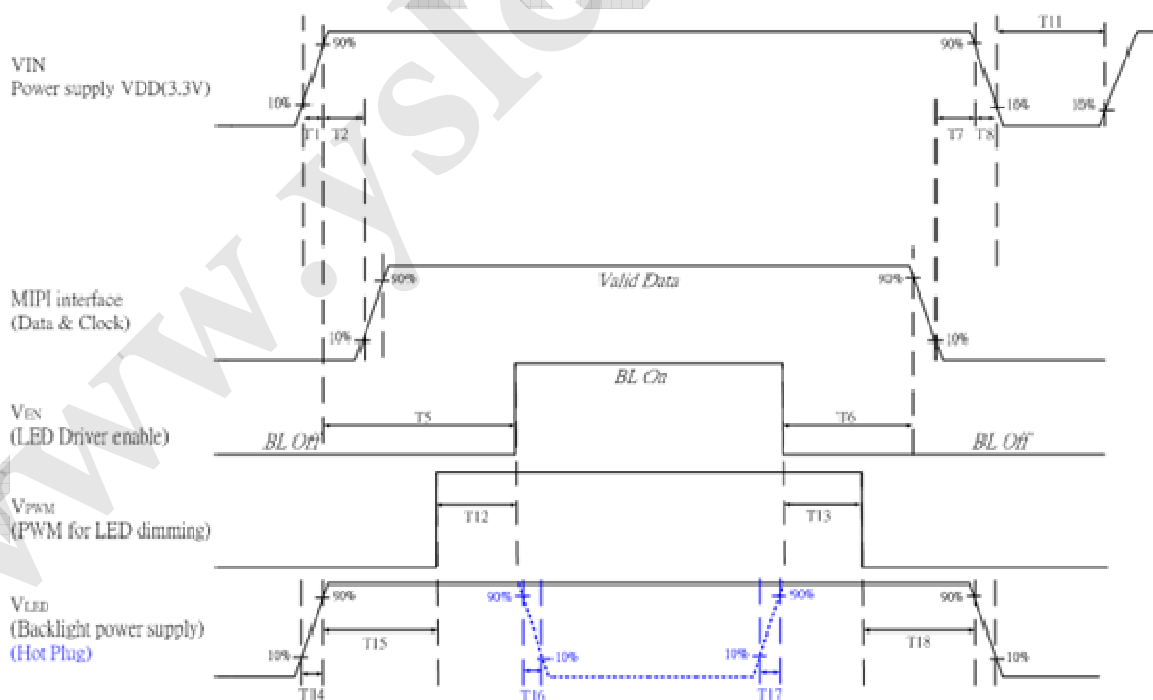
| Power Sequence Timing | | | |
|---|---|---|---|
| | Value | | |
| Parameter | Min. | Max. | Units |
| T1 | 0.5 | 10 | |
| T2 | 0 | 50 | |
| T5 | 200 | - | |
| T6 | 200 | - | |
| T7 | 0 | 50 | |
| T8 | 0 | 10 | |
| T11 | 500 | - | ms |
| T12 | 10 | - | |
| T13 | 10 | - | |
| T14 | 0.5 | 10 | |
| T15 | 10 | - | |
| T16 | 1* | - | |
| T17 | 1* | - | |
| T18 | 10 | - | |

Note : T12,T13,T15 value are recommended, T12,T13,T15 $\geq$ 0 could be acceptable

# 7. Panel Reliability Test

## 7.1 Vibration Test

**Test Spec:**

- Test method:   Non-Operation
- Acceleration:   1.5 G
- Frequency:   10 - 500Hz Random
- Sweep:   30 Minutes each Axis (X, Y, Z)

## 7.2 Shock Test

**Test Spec:**

- Test method:   Non-Operation
- Acceleration:   220 G , Half sine wave
- Active time:   2 ms
- Pulse:   X,Y,Z .one time for each side

## 7.3 Reliability Test

| Items | Required Condition | Note |
|---|---|---|
| Temperature Humidity Bias | Ta= 40℃, 90%RH, 300h | |
| High Temperature Operation | Ta= 50℃, Dry, 300h | |
| Low Temperature Operation | Ta= 0℃, 300h | |
| High Temperature Storage | Ta= 60℃, 300h | |
| Low Temperature Storage | Ta= -20℃, 300h | |
| Thermal Shock Test | Ta=-20℃ to 60℃, Duration at 30 min, 100 cycles | |
| ESD | Contact : ±8 KV<br>Air : ±15 KV | Note 1 |

**Note1:** According to EN 61000-4-2 , ESD class B: Some performance degradation allowed. No data lost

.   Self-recoverable. No hardware failures.

**Remark:** MTBF (Excluding the LED): 30,000 hours with a confidence level 90%

# 8. Mechanical Characteristics

## 8.1 LCM Outline Dimension

### 8.1.1 Standard Front View

## 8.1.2 Standard Rear View



BLU BARCODE AREA

SHIPPING LABEL

5.00

6.35

46.00

9.00

5.70

$8.30 \pm 1.00$ (S1)

$127.02 \pm 1.00$ (R1)
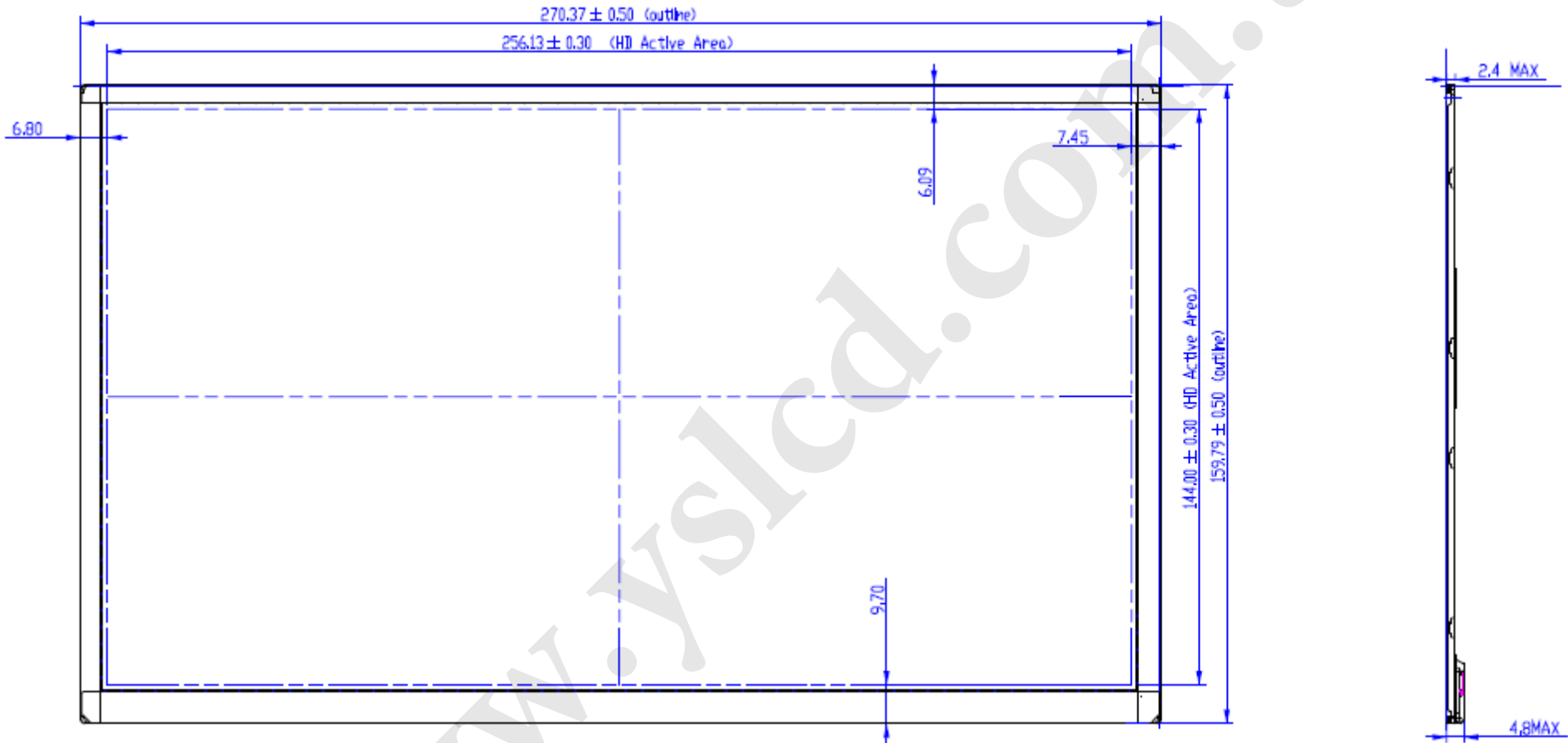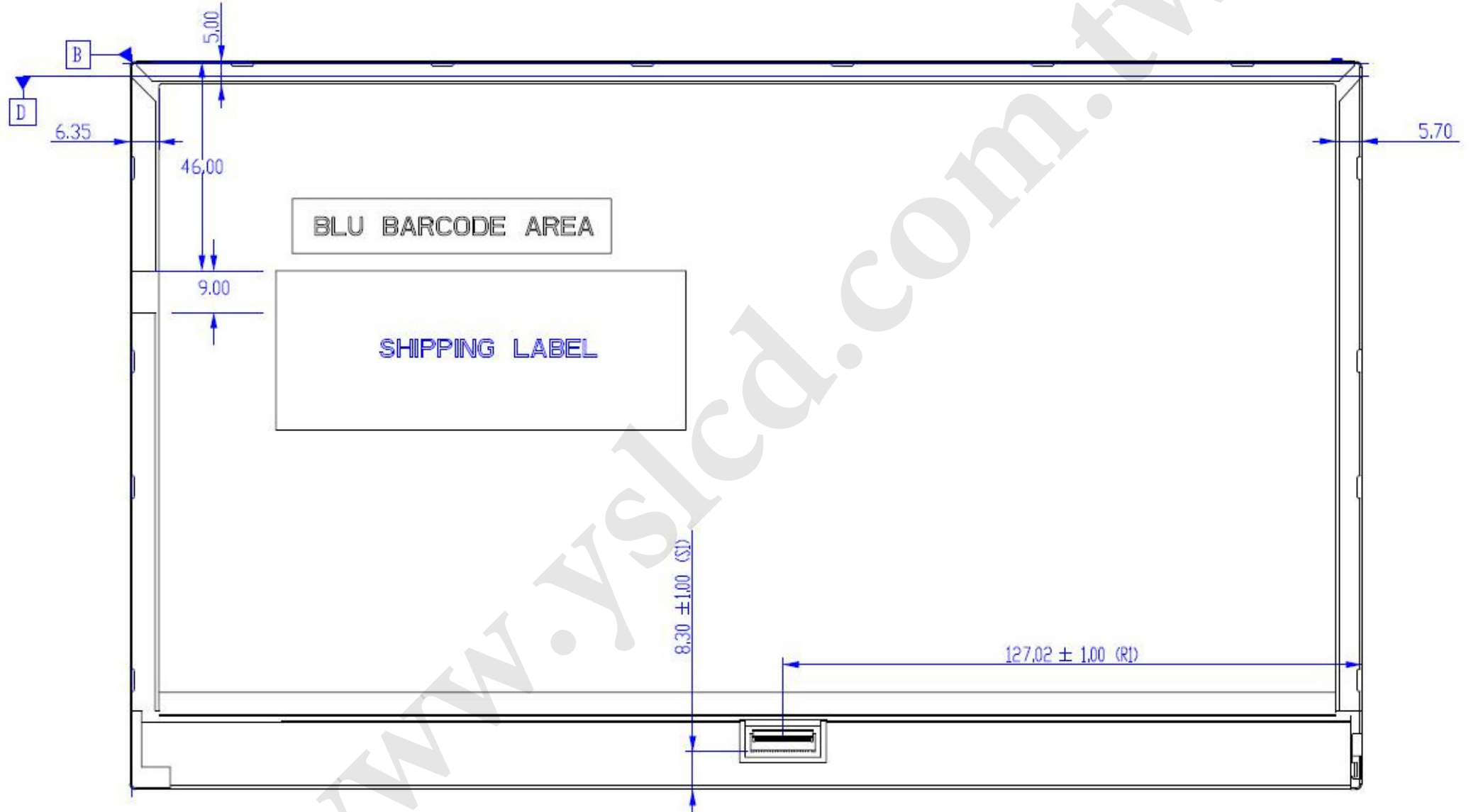
# 9. Shipping and Package

## 9.1 Shipping Label Format

### Shipping label

Manufactured 05/52
Model No: B116XAN03.1
AU Optronics
Made in China (S01)

H/W: 1A  F/W:1

* XXXXXXXXXXX-XXXXXX

cᴿᵁus
E204356

Pb

RoHS

15

### Carton Label

AU Optronics

QTY : 48   RoHS   Pb

MODEL NO : B116XAN03.1

PART NO : 97.11B20.101

CUSTOMER NO :

CARTON NO :

Made in China

****ZS0307−0822500037*

## 9.2 Carton Package
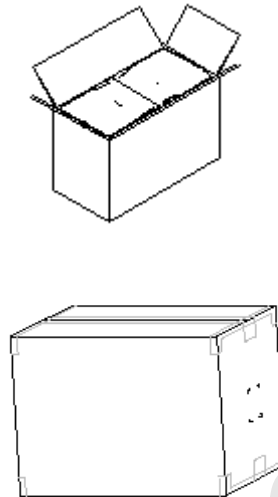


## 9.3 Shipping Package of Palletizing Sequence

# 10. Appendix

## 10.1 EDID Description

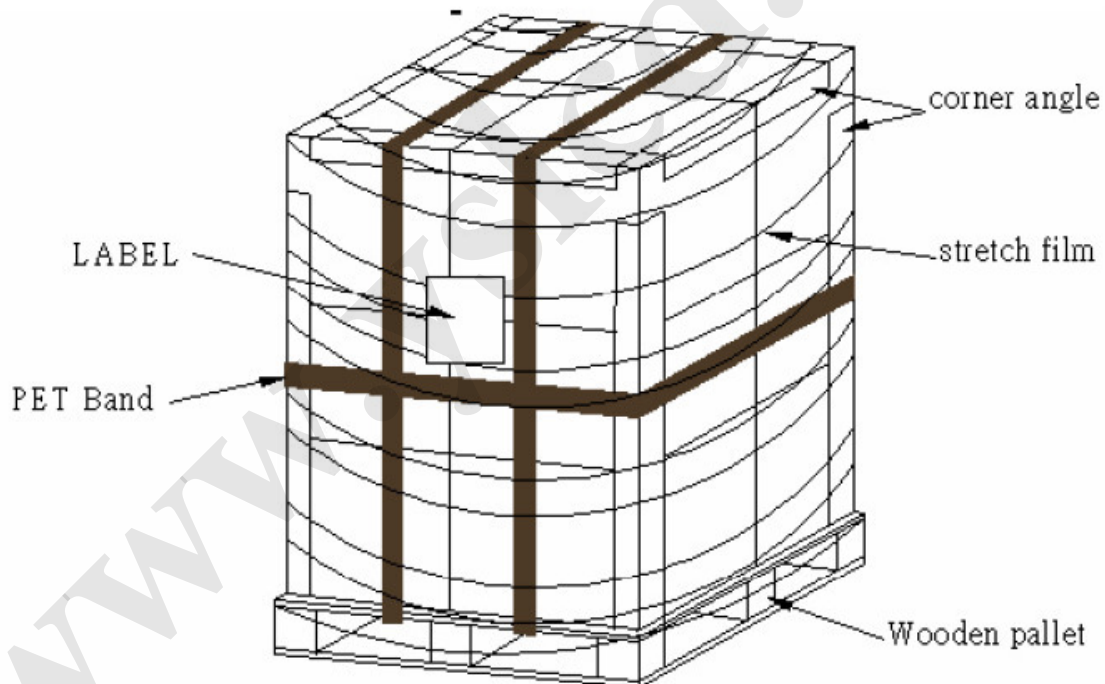| Address | FUNCTION | Value | Value | Value |
|---------|----------|-------|-------|-------|
| HEX | | HEX | BIN | DEC |
| 00 | Header | 00 | 00000000 | 0 |
| 01 | | FF | 11111111 | 255 |
| 02 | | FF | 11111111 | 255 |
| 03 | | FF | 11111111 | 255 |
| 04 | | FF | 11111111 | 255 |
| 05 | | FF | 11111111 | 255 |
| 06 | | FF | 11111111 | 255 |
| 07 | | 00 | 00000000 | 0 |
| 08 | EISA Manuf. Code LSB | 06 | 00000110 | 6 |
| 09 | Compressed ASCII | AF | 10101111 | 175 |
| 0A | Product Code | 5C | 01011100 | 92 |
| 0B | hex, LSB first | 31 | 00110001 | 49 |
| 0C | 32-bit ser # | 00 | 00000000 | 0 |
| 0D | | 00 | 00000000 | 0 |
| 0E | | 00 | 00000000 | 0 |
| 0F | | 00 | 00000000 | 0 |
| 10 | Week of manufacture | 00 | 00000000 | 0 |
| 11 | Year of manufacture | 16 | 00010110 | 22 |
| 12 | EDID Structure Ver. | 01 | 00000001 | 1 |
| 13 | EDID revision # | 04 | 00000100 | 4 |
| 14 | **Video input def.**   (digital I/P, non-TMDS, CRGB) | A0 | 10100000 | 160 |
| 15 | **Max H image size**     (rounded to cm) | 1A | 00011010 | 26 |
| 16 | **Max V image size**   (rounded to cm) | 0E | 00001110 | 14 |
| 17 | **Display Gamma**     (=(gamma*100)-100) | 78 | 01111000 | 120 |
| 18 | **Feature support**    (no DPMS, Active OFF, RGB, tmg Blk#1) | 02 | 00000010 | 2 |
| 19 | Red/green low bits **(Lower 2:2:2:2 bits)** | D6 | 11010110 | 214 |
| 1A | Blue/white low bits **(Lower 2:2:2:2 bits)** | 35 | 00110101 | 53 |
| 1B | Red x   **(Upper 8 bits)** | 96 | 10010110 | 150 |
| 1C | Red y/ highER 8 bits | 56 | 01010110 | 86 |
| 1D | Green x | 54 | 01010100 | 84 |
| 1E | Green y | 96 | 10010110 | 150 |
| 1F | Blue x | 28 | 00101000 | 40 |
| 20 | Blue y | 20 | 00100000 | 32 |
| 21 | White x | 50 | 01010000 | 80 |
| 22 | White y | 54 | 01010100 | 84 |
| 23 | Established timing 1 | 00 | 00000000 | 0 |
| 24 | Established timing 2 | 00 | 00000000 | 0 |
| 25 | Established timing 3 | 00 | 00000000 | 0 |
| 26 | Standard timing #1 | 01 | 00000001 | 1 |
| 27 | | 01 | 00000001 | 1 |
| 28 | Standard timing #2 | 01 | 00000001 | 1 |
| 29 | | 01 | 00000001 | 1 |
| 2A | Standard timing #3 | 01 | 00000001 | 1 |
| 2B | | 01 | 00000001 | 1 |

| | | | | |
|---|---|---|---|---|
| 2C | Standard timing #4 | 01 | 00000001 | 1 |
| 2D | | 01 | 00000001 | 1 |
| 2E | Standard timing #5 | 01 | 00000001 | 1 |
| 2F | | 01 | 00000001 | 1 |
| 30 | Standard timing #6 | 01 | 00000001 | 1 |
| 31 | | 01 | 00000001 | 1 |
| 32 | Standard timing #7 | 01 | 00000001 | 1 |
| 33 | | 01 | 00000001 | 1 |
| 34 | Standard timing #8 | 01 | 00000001 | 1 |
| 35 | | 01 | 00000001 | 1 |
| 36 | Pixel Clock/10000    LSB | 9E | 10011110 | 158 |
| 37 | Pixel Clock/10000    USB | 1B | 00011011 | 27 |
| 38 | Horz active    **Lower 8bits** | 56 | 01010110 | 86 |
| 39 | Horz blanking    **Lower 8bits** | 7C | 01111100 | 124 |
| 3A | HorzAct:HorzBlnk    **Upper 4:4 bits** | 50 | 01010000 | 80 |
| 3B | Vertical Active    **Lower 8bits** | 00 | 00000000 | 0 |
| 3C | Vertical Blanking    **Lower 8bits** | 16 | 00010110 | 22 |
| 3D | Vert Act : Vertical Blanking    **(upper 4:4 bit)** | 30 | 00110000 | 48 |
| 3E | HorzSync. Offset | 30 | 00110000 | 48 |
| 3F | HorzSync.Width | 20 | 00100000 | 32 |
| 40 | VertSync.Offset : VertSync.Width | 46 | 01000110 | 70 |
| 41 | Horz&Vert Sync Offset/Width **Upper 2bits** | 00 | 00000000 | 0 |
| 42 | Horizontal Image Size    **Lower 8bits** | 00 | 00000000 | 0 |
| 43 | Vertical Image Size    **Lower 8bits** | 90 | 10010000 | 144 |
| 44 | Horizontal & Vertical Image Size    **(upper 4:4 bits)** | 10 | 00010000 | 16 |
| 45 | Horizontal Border    *(zero for internal LCD)* | 00 | 00000000 | 0 |
| 46 | Vertical Border    *(zero for internal LCD)* | 00 | 00000000 | 0 |
| 47 | Signal *(non-intr, norm, no stero, sep sync, neg pol)* | 18 | 00011000 | 24 |
| 48 | Detailed timing/monitor | 00 | 00000000 | 0 |
| 49 | descriptor #2 | 00 | 00000000 | 0 |
| 4A | | 00 | 00000000 | 0 |
| 4B | | 0F | 00001111 | 15 |
| 4C | | 00 | 00000000 | 0 |
| 4D | | 00 | 00000000 | 0 |
| 4E | | 00 | 00000000 | 0 |
| 4F | | 00 | 00000000 | 0 |
| 50 | | 00 | 00000000 | 0 |
| 51 | | 00 | 00000000 | 0 |
| 52 | | 00 | 00000000 | 0 |
| 53 | | 00 | 00000000 | 0 |
| 54 | | 00 | 00000000 | 0 |
| 55 | | 00 | 00000000 | 0 |
| 56 | | 00 | 00000000 | 0 |
| 57 | | 00 | 00000000 | 0 |
| 58 | | 00 | 00000000 | 0 |
| 59 | | 20 | 00100000 | 32 |
| 5A | Detailed timing/monitor | 00 | 00000000 | 0 |
| 5B | descriptor #3 | 00 | 00000000 | 0 |
| 5C | | 00 | 00000000 | 0 |

| | | | | |
|---|---|---|---|---|
| 5D | | FE | 11111110 | 254 |
| 5E | | 00 | 00000000 | 0 |
| 5F | Manufacture | 41 | 01000001 | 65 |
| 60 | Manufacture | 55 | 01010101 | 85 |
| 61 | Manufacture | 4F | 01001111 | 79 |
| 62 | | 0A | 00001010 | 10 |
| 63 | | 20 | 00100000 | 32 |
| 64 | | 20 | 00100000 | 32 |
| 65 | | 20 | 00100000 | 32 |
| 66 | | 20 | 00100000 | 32 |
| 67 | | 20 | 00100000 | 32 |
| 68 | | 20 | 00100000 | 32 |
| 69 | | 20 | 00100000 | 32 |
| 6A | | 20 | 00100000 | 32 |
| 6B | | 20 | 00100000 | 32 |
| 6C | Detailed timing/monitor | 00 | 00000000 | 0 |
| 6D | descriptor #4 | 00 | 00000000 | 0 |
| 6E | | 00 | 00000000 | 0 |
| 6F | | FE | 11111110 | 254 |
| 70 | | 00 | 00000000 | 0 |
| 71 | Manufacture P/N | 42 | 01000010 | 66 |
| 72 | Manufacture P/N | 31 | 00110001 | 49 |
| 73 | Manufacture P/N | 31 | 00110001 | 49 |
| 74 | Manufacture P/N | 36 | 00110110 | 54 |
| 75 | Manufacture P/N | 58 | 01011000 | 88 |
| 76 | Manufacture P/N | 41 | 01000001 | 65 |
| 77 | Manufacture P/N | 4E | 01001110 | 78 |
| 78 | Manufacture P/N | 30 | 00110000 | 48 |
| 79 | Manufacture P/N | 33 | 00110011 | 51 |
| 7A | Manufacture P/N | 2E | 00101110 | 46 |
| 7B | Manufacture P/N | 31 | 00110001 | 49 |
| 7C | | 20 | 00100000 | 32 |
| 7D | | 0A | 00001010 | 10 |
| 7E | Extension Flag | 00 | 00000000 | 0 |
| 7F | Checksum | 34 | 00110100 | 52 |