




Product Specification

AU OPTRONICS CORPORATION

() Preliminary Specifications

(v) Final Specifications

Module	11.6"(11.58") FHD 16:9 Color TFT-LCD with LED Backlight design
Model Name	B116HAN03.1
Note ()	<i>LED Backlight with driving circuit design</i>

Customer

Date

Checked &
Approved
by

Date

Note: This Specification is subject to
change without notice.

Approved by

Date

Kevin KH Shen

07/26/2013

Prepared by

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07/26/2013

**MPBU Marketing Division
AU Optronics corporation**



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Record of Revision

Version and Date	Page	Old description	New Description	Remark
0.1 2012/9/24	All	First Edition for Customer		
0.2 2012/10/1	18	Update Pin Assignment		
	20	Update Timing Characteristics		
0.3 2012/10/1	19	Update Pin Assignment Drawing		
	20	Update Timing Characteristics		
	25, 26, 27	Update 2D-Drawings		
	28	Update Label Format		
	29	Update Packing Sequence		
	30	Update EDID		
0.4 2012/10/12	20	Update Clock Frequency		
0.5 2012/10/26	5	Update thickness to 4.94mm max/ Update pixel pitch to 0.1335 x 0.1335 mm/ Update power consumption		
	26	Update 2D drawing		
	28	Update Label Information		
	29	Update Carton Packing Information		
0.6 2012/11/14	5	Add 13 point Luminance Uniformity		
	6	Update LED current to 23mA Add Min brightness Update color coordinates		
	13	Update Power Specification		
	20	Update frame rate to 60Hz		
0.7 2012/11/20	25	Update 2D drawing		
0.8 2013/01/08	21		Update 6.4 Note description	
1.0 2013/02/19	23		Remove T19/20	
	29		Update Label	



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1.1 2013/3/18	7		Update Min value of Viewing angle and C/R	
	14	IDD current: 270 Note1: Black pattern	IDD current:300	
	17	LED life-time conditions is IF=19mA	LED life-time conditions is IF=23mA	
	21	Timing characteristics 1920 x 1080 / 60MHz	Timing characteristics 1920 x 1080 / 60Hz	



1. Handling Precautions

- 1) Since front polarizer is easily damaged, pay attention not to scratch it.
- 2) Be sure to turn off power supply when inserting or disconnecting from input connector.
- 3) Wipe off water drop immediately. Long contact with water may cause discoloration or spots.
- 4) When the panel surface is soiled, wipe it with absorbent cotton or other soft cloth.
- 5) Since the panel is made of glass, it may break or crack if dropped or bumped on hard surface.
- 6) Since CMOS LSI is used in this module, take care of static electricity and insure human earth when handling.
- 7) Do not open nor modify the Module Assembly.
- 8) Do not press the reflector sheet at the back of the module to any directions.
- 9) At the insertion or removal of the Signal Interface Connector, be sure not to rotate nor tilt the Interface Connector of the TFT Module.
- 11) After installation of the TFT Module into an enclosure (Notebook PC Bezel, for example), do not twist nor bend the TFT Module even momentary. At designing the enclosure, it should be taken into consideration that no bending/twisting forces are applied to the TFT Module from outside. Otherwise the TFT Module may be damaged.
- 12) Small amount of materials having no flammability grade is used in the LCD module. The LCD module should be supplied by power complied with requirements of Limited Power Source (IEC60950 or UL1950), or be applied exemption.
- 13) Disconnecting power supply before handling LCD modules, it can prevent electric shock, DO NOT TOUCH the electrode parts, cables, connectors and LED circuit part of TFT module that a LED light bar build in as a light source of back light unit. It can prevent electrostatic breakdown.



2. General Description

B116HAN03.1 is a Color Active Matrix Liquid Crystal Display composed of a TFT LCD panel, a driver circuit, and LED backlight system. The screen format is intended to support the 16:9 , 1920(H) x1080(V) screen and 16.7M colors (RGB 8-bits data driver) with LED backlight driving circuit. All input signals are eDP interface compatible.

B116HAN03.1 is designed for a display unit of notebook style personal computer and industrial machine.

2.1 General Specification

The following items are characteristics summary on the table at 25 °C condition:

Items	Unit	Specifications			
Screen Diagonal	[mm]	293.83 (11.6W")			
Active Area	[mm]	256.32(H) x 144.18(V)			
Pixels H x V		1920 x 3(RGB) x 1080			
Pixel Pitch	[mm]	0.1335 X 0.1335			
Pixel Format		R.G.B. Vertical Stripe			
Display Mode		Normally Black			
White Luminance (I _{LED} =23mA) (Note: I _{LED} is LED current)	[cd/m ²]	400 typ. (5 points average)			
Luminance Uniformity		1.25 max. (5 points) 1.5 max (13 points)			
Contrast Ratio		800 typ			
Response Time	[ms]	25 typ / 35 Max			
Nominal Input Voltage VDD	[Volt]	+3.3 typ.			
Power Consumption	[Watt]	4 max. (Include Logic and Blu power)			
Weight	[Grams]	170 max.(W/O digitizer)			
Physical Size (LCM only) without bracket	[mm]		Min.	Typ.	Max.
		Length		270.37	
		Width		159.79	
		Thickness	---		2.4/4.94
Electrical Interface		2 lane eDP			
Glass Thickness	[mm]	0.25			



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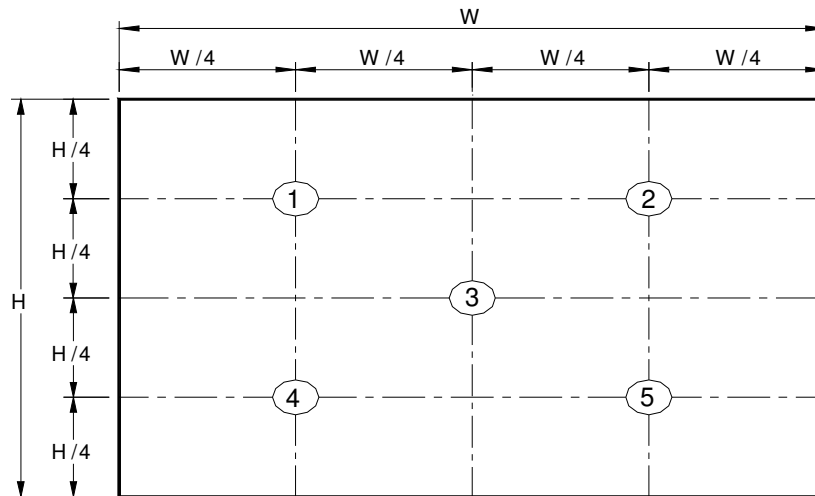
Surface Treatment(panel only)		Anti-Glare, Hardness 3H
Support Color		RGB 8-bit
Temperature Range Operating Storage (Non-Operating)	[°C] [°C]	0 to +50 -20 to +60
RoHS Compliance		RoHS Compliance

2.2 Optical Characteristics

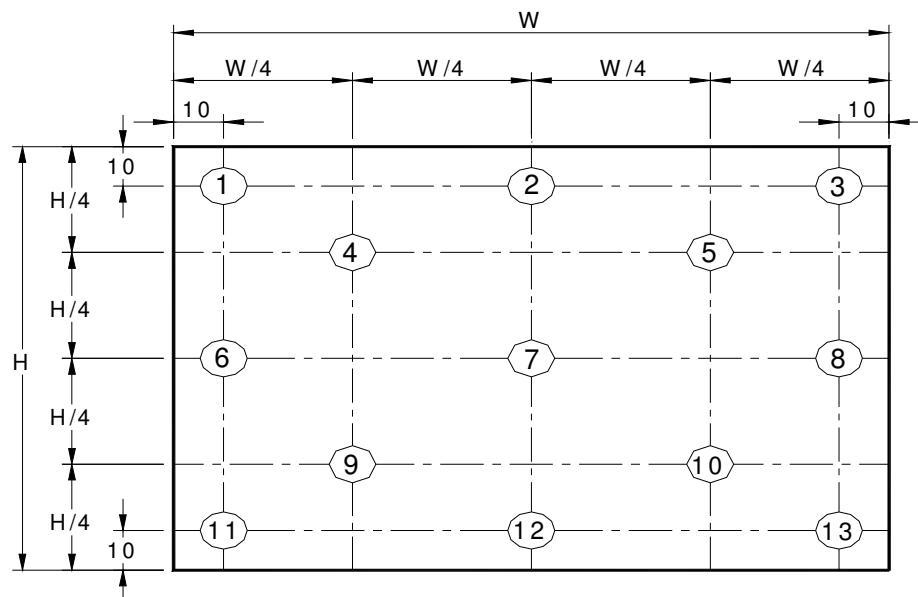
The optical characteristics are measured under stable conditions at 25°C (Room Temperature) :

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit	Note
White Luminance I_{LED} = 23mA		5 points average	340	400	---	cd/m ²	1, 4, 5.
Viewing Angle	θ_R θ_L	Horizontal (Right) CR = 10 (Left)	80 80	89 89	--- ---	degree	4, 9
		Vertical (Upper) CR = 10 (Lower)	80 80	89 89	--- ---		
	ψ_H ψ_L						
Luminance Uniformity	δ_{5P}	5 Points	---	---	1.25		1, 3, 4
Luminance Uniformity	δ_{13P}	13 Points	---	---	1.5		2, 3, 4
Contrast Ratio	CR		600	800	-		4, 6
Cross talk	%		---	---	4		4, 7
Response Time	T_{RT}	Rising + Falling	---	30	45	msec	4, 8
Color / Chromaticity Coordinates	Red	R_x	0.566	0.596	0.626		4
		R_y	0.316	0.346	0.376		
	Green	G_x	0.297	0.327	0.357		
		G_y	0.558	0.588	0.618		
	Blue	B_x	0.123	0.153	0.183		
		B_y	0.098	0.128	0.158		
	White	W_x	0.283	0.313	0.343		
		W_y	0.299	0.329	0.359		
	NTSC		-	52	-		

Note 1: 5 points position (Ref: Active area)



Note 2: 13 points position (Ref: Active area)



Note 3: The luminance uniformity of 5 or 13 points is defined by dividing the maximum luminance values by the minimum test point luminance

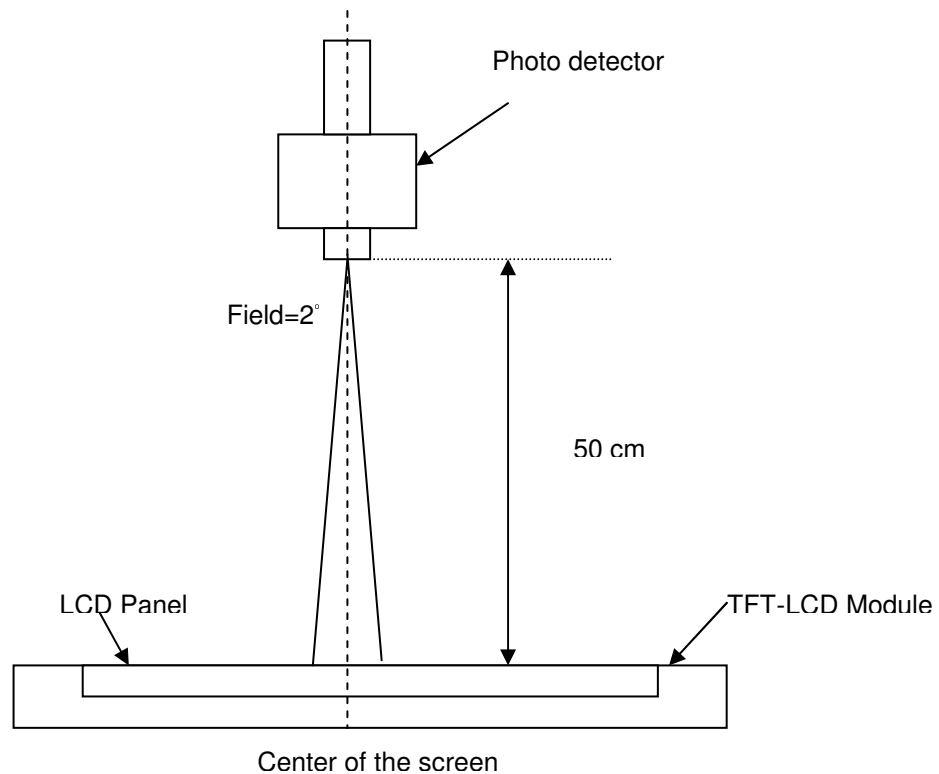
$$\delta_{W5} = \frac{\text{Maximum Brightness of five points}}{\text{Minimum Brightness of five points}}$$

$$\delta_{W13} = \frac{\text{Maximum Brightness of thirteen points}}{\text{Minimum Brightness of thirteen points}}$$

Note 4: Measurement method

The LCD module should be stabilized at given temperature for 30 minutes to avoid abrupt temperature change during measuring. In order to stabilize the luminance, the measurement

should be executed after lighting Backlight for 30 minutes in a stable, windless and dark room, and it should be measured in the center of screen.



Note 5 : Definition of Average Luminance of White (Y_L):

Measure the luminance of gray level 63 at 5 points · $Y_L = [L(1) + L(2) + L(3) + L(4) + L(5)] / 5$

$L(x)$ is corresponding to the luminance of the point X at Figure in Note (1).

Note 6 : Definition of contrast ratio:

Contrast ratio is calculated with the following formula.

$$\text{Contrast ratio (CR)} = \frac{\text{Brightness on the "White" state}}{\text{Brightness on the "Black" state}}$$

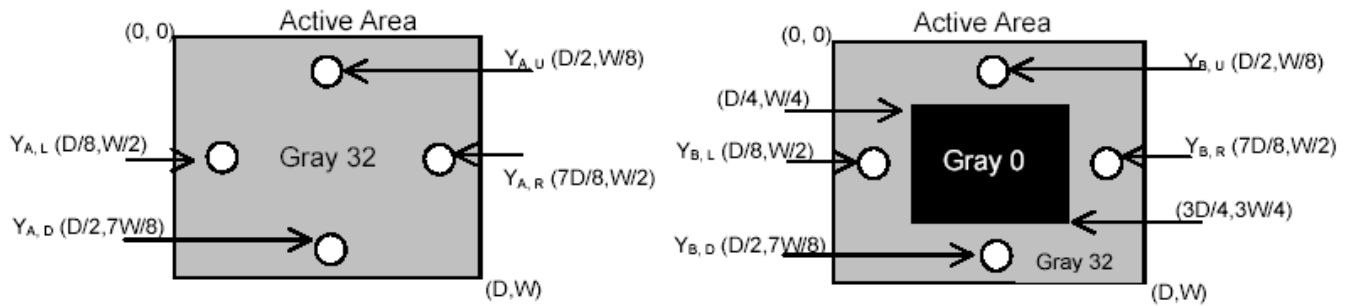
Note 7 : Definition of Cross Talk (CT)

$$CT = |Y_B - Y_A| / Y_A \times 100 (\%)$$

Where

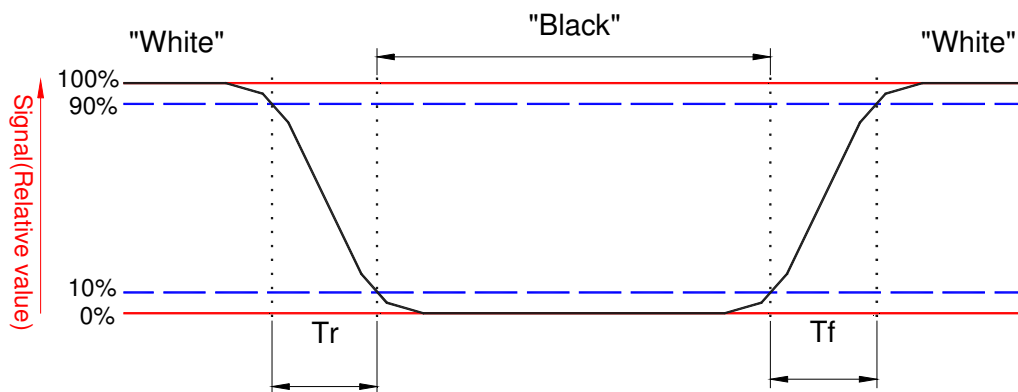
Y_A = Luminance of measured location without gray level 0 pattern (cd/m²)

Y_B = Luminance of measured location with gray level 0 pattern (cd/m²)



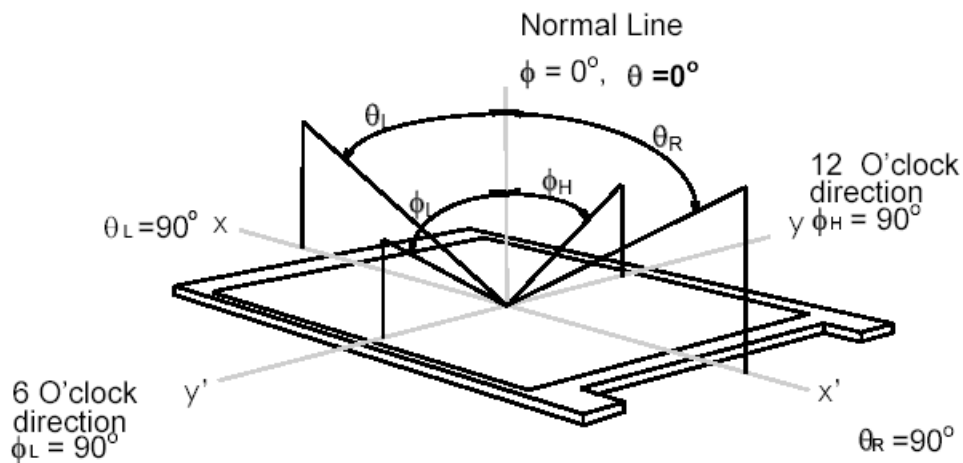
Note 8: Definition of response time:

The output signals of BM-7 or equivalent are measured when the input signals are changed from "Black" to "White" (falling time) and from "White" to "Black" (rising time), respectively. The response time interval between the 10% and 90% of amplitudes. Refer to figure as below.



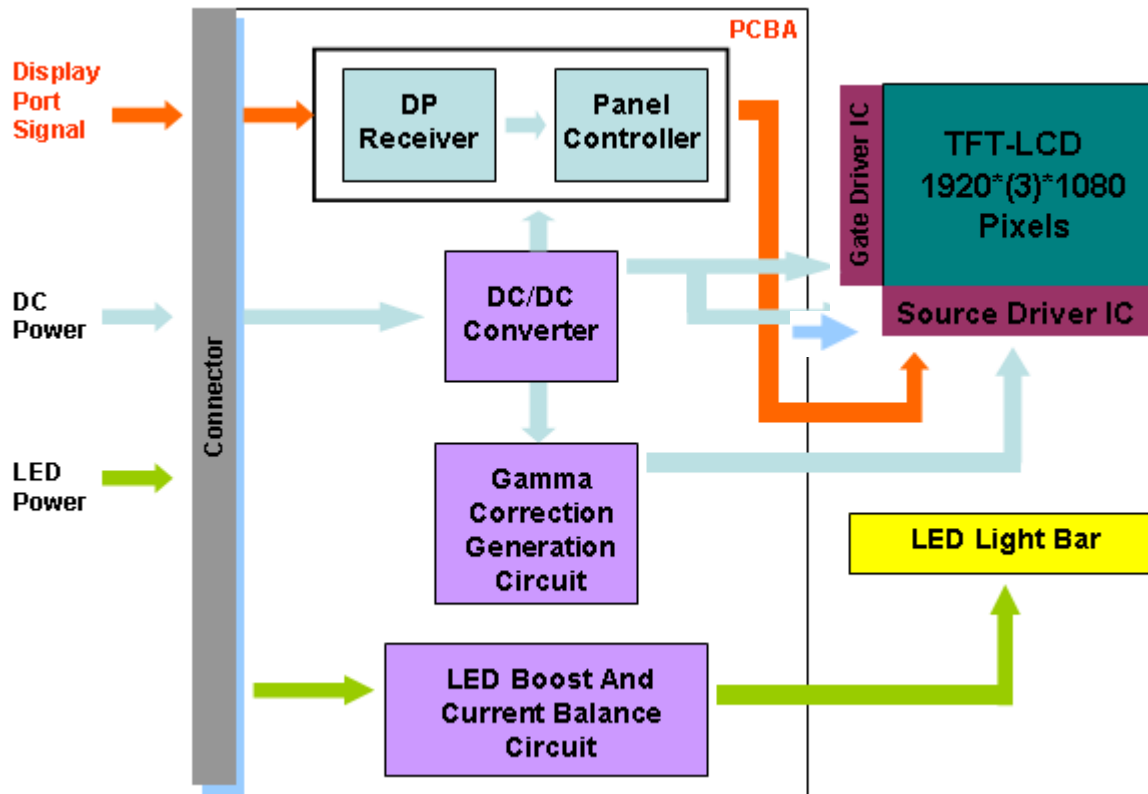
Note 9. Definition of viewing angle

Viewing angle is the measurement of contrast ratio ≥ 10 , at the screen center, over a 180° horizontal and 180° vertical range (off-normal viewing angles). The 180° viewing angle range is broken down as follows; 90° (θ) horizontal left and right and 90° (ϕ) vertical, high (up) and low (down). The measurement direction is typically perpendicular to the display surface with the screen rotated about its center to develop the desired measurement viewing angle.



3. Functional Block Diagram

The following diagram shows the functional block of the 11.6 inches wide Color TFT/LCD 40 Pin one channel Module



4. Absolute Maximum Ratings

An absolute maximum rating of the module is as following:

4.1 Absolute Ratings of TFT LCD Module

Item	Symbol	Min	Max	Unit	Conditions
Logic/LCD Drive	Vin	-0.3	+4.0	[Volt]	Note 1,2

4.2 Absolute Ratings of Environment

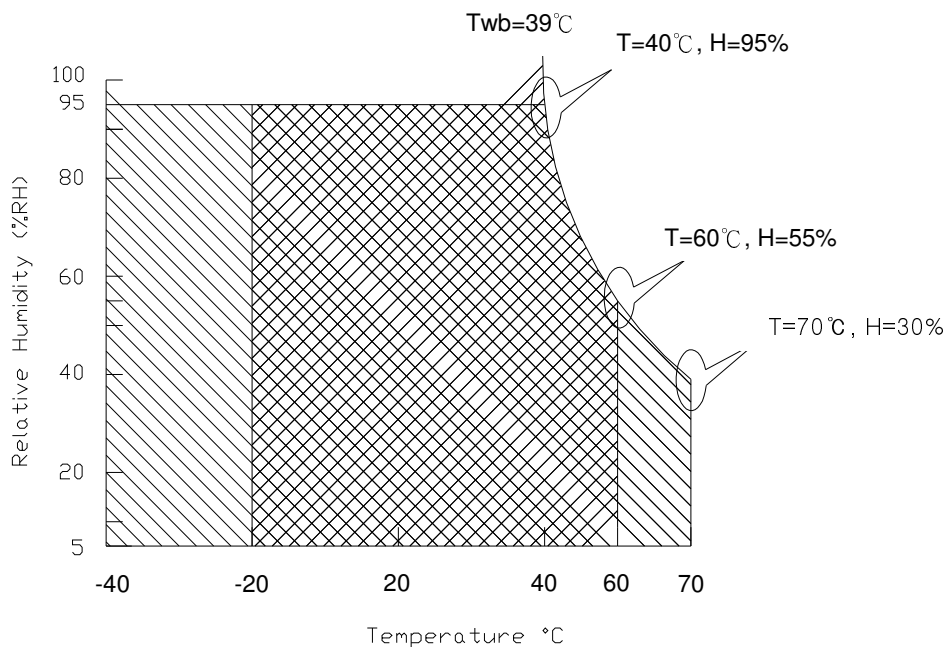
Item	Symbol	Min	Max	Unit	Conditions
Operating	TOP	0	+50	[°C]	Note 4
Operation Humidity	HOP	5	95	[%RH]	Note 4
Storage	TST	-20	+60	[°C]	Note 4
Storage Humidity	HST	5	95	[%RH]	Note 4

Note 1: At Ta (25°C)

Note 2: Permanent damage to the device may occur if exceed maximum values

Note 3: LED specification refer to section 5.2

Note 4: For quality performance, please refer to AUO IIS (Incoming Inspection Standard).



Operating Range 

Storage Range  + 

5. Electrical Characteristics

5.1 TFT LCD Module

5.1.1 Power Specification

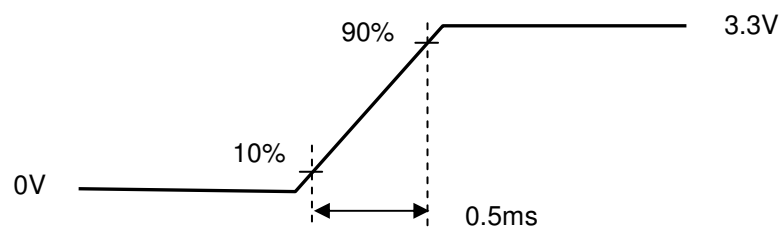
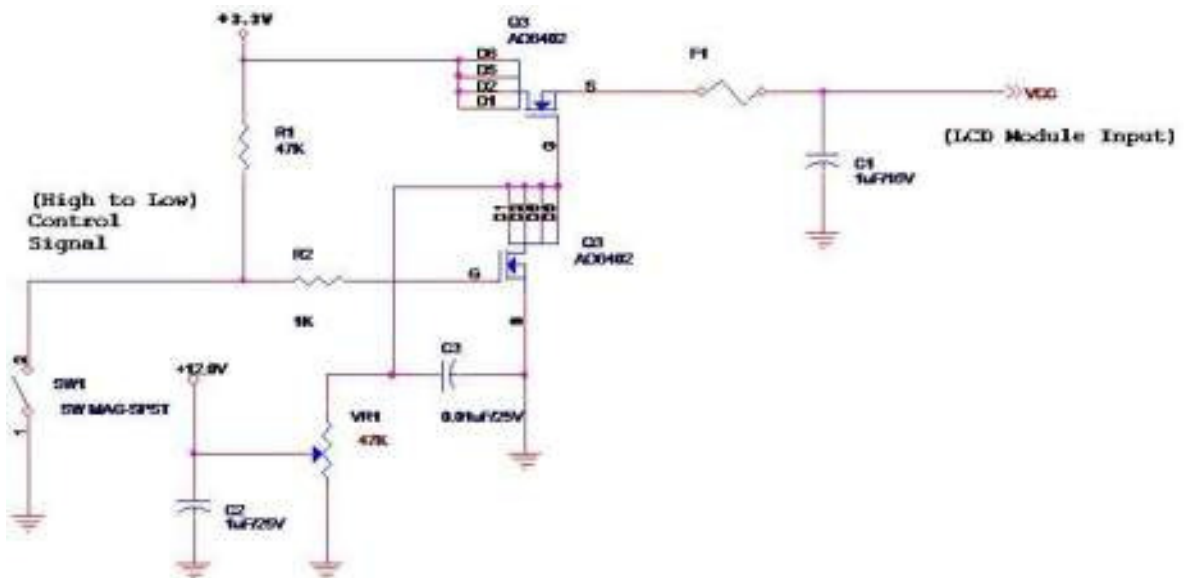
Input power specifications are as follows;

The power specification are measured under 25°C and frame frequency under 60Hz

Symble	Parameter	Min	Typ	Max	Units	Note
VDD	Logic/LCD Drive Voltage	3.0	3.3	3.6	[Volt]	
PDD	VDD Power	-	-	1	[Watt]	Note 1
IDD	IDD Current	-	-	300	[mA]	Note 1
IRush	Inrush Current	-	-	2000	[mA]	Note 2
VDDrp	Allowable Logic/LCD Drive Ripple Voltage	-	-	100	[mV] p-p	

Note 1 : Maximum Measurement Condition : White Pattern at 3.3V driving voltage. ($P_{max}=V_{3.3} \times I_{White}$)

Note 2 : Measure Condition



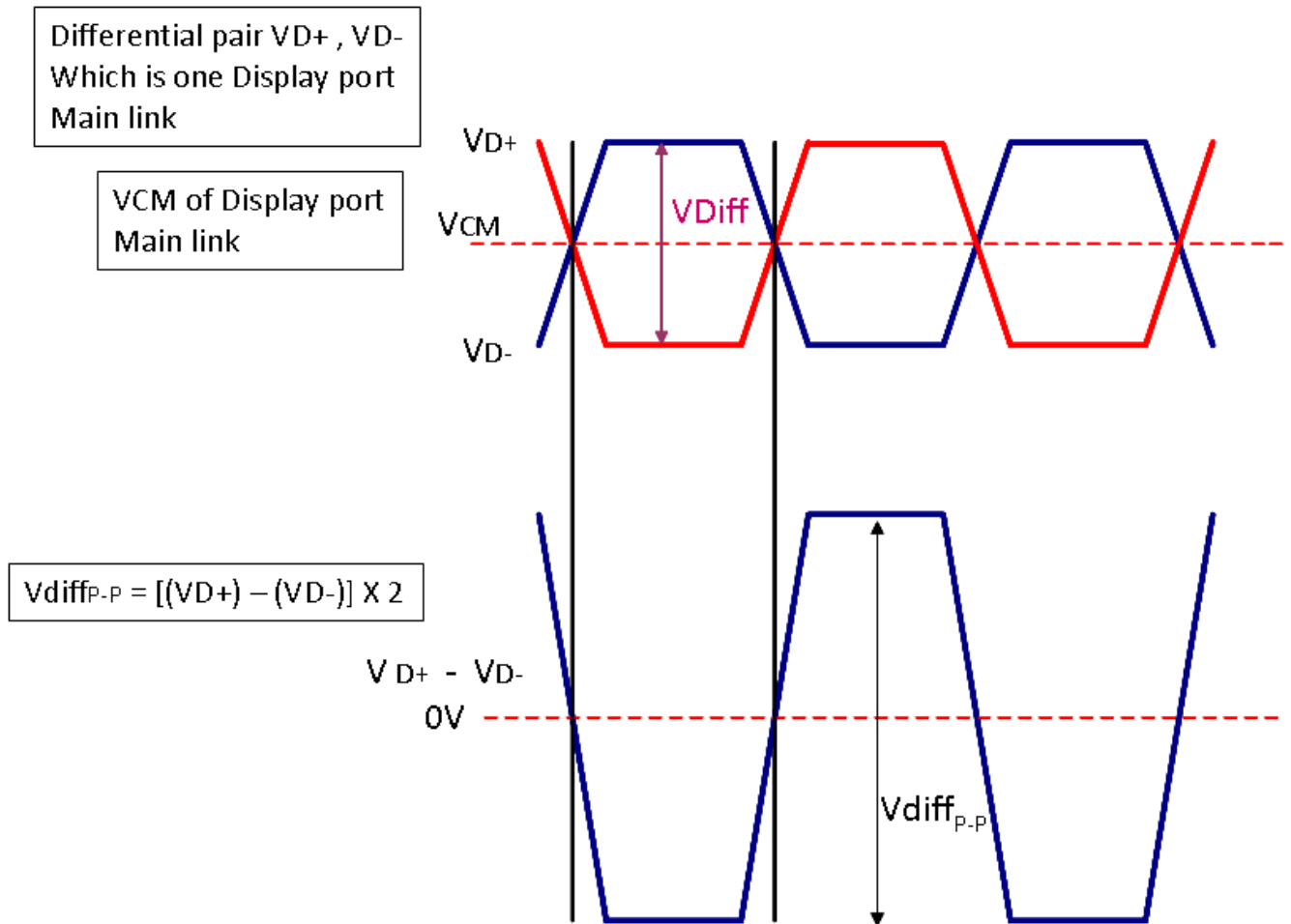
Vin rising time

5.1.2 Signal Electrical Characteristics

Input signals shall be low or High-impedance state when VDD is off.

Signal electrical characteristics are as follows;

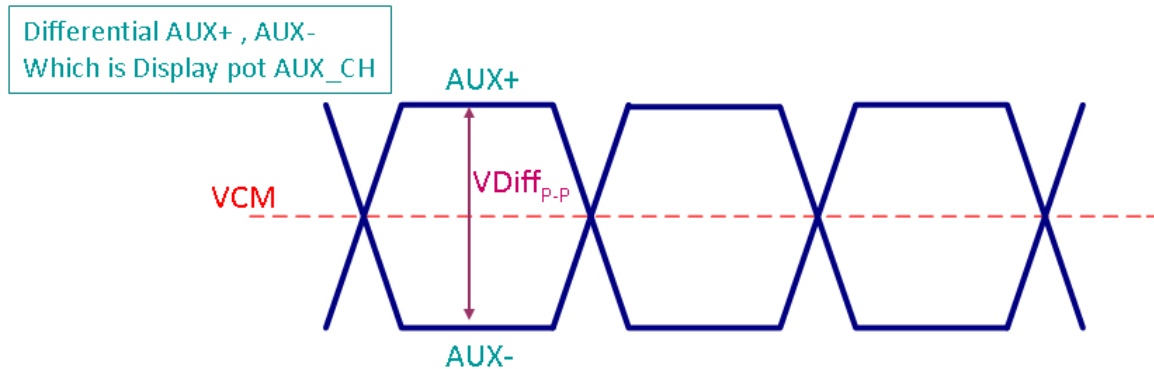
Display Port main link signal:



Display port main link					
		Min	Typ	Max	unit
VCM	RX input DC Common Mode Voltage		0		V
$V_{Diff_{P-P}}$	Peak-to-peak Voltage at a receiving Device	120		1320	mV

Follow as VESA display port standard V1.1a.

Display Port AUX_CH signal:



Display port AUX_CH					
		Min	Typ	Max	unit
VCM	AUX DC Common Mode Voltage		0		V
VDiff _{p-p}	AUX Peak-to-peak Voltage at a receiving Device	0.4	0.6	0.8	V

Follow as VESA display port standard V1.1a.

Display Port VHPD signal:

Display Port VHPD					
		Min	Typ	Max	unit
VHPD	HPD voltage	2.25		3.6	V

Follow as VESA display port standard V1.1a.



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5.3 Backlight Unit

5.3.1 LED characteristics

Parameter	Symbol	Min	Typ	Max	Unit	Condition
Backlight Power Consumption	PLED	-	-	2.65	[Watt]	(Ta=25°C), Note 1 Vin =12V
LED Life-Time	N/A	10,000	-	-	Hour	(Ta=25°C), Note 2 If=23mA

Note 1: Calculator value for reference $P_{LED} = V_F$ (Normal Distribution) * I_F (Normal Distribution) / Efficiency

Note 2: The LED life-time define as the estimated time to 50% degradation of initial luminous.

5.3.2 Backlight input signal characteristics

Parameter	Symbol	Min	Typ	Max	Units	Remark
LED Power Supply	VLED	7	12.0	21.0	[Volt]	Define as Connector Interface (Ta=25°C)
PWM Logic Input High Level	VPWM_EN	2.5	3.3	5.5	[Volt]	
PWM Logic Input Low Level		-	-	0.8	[Volt]	
PWM Input Frequency	FPWM Duty	200	6K	15K	Hz	
PWM Duty Ratio		5	--	100	%	

6.1 Pixel Format Image

	1										1920									
1st Line	R	G	B											R	G	B	R	G	B	
	
	
	
	
	
	
	
	
	
1080th Line	R	G	B	R	G	B								R	G	B	R	G	B	

6.2 Integration Interface Requirement

6.2.1 Connector Description

Physical interface is described as for the connector on module.

These connectors are capable of accommodating the following signals and will be following components.

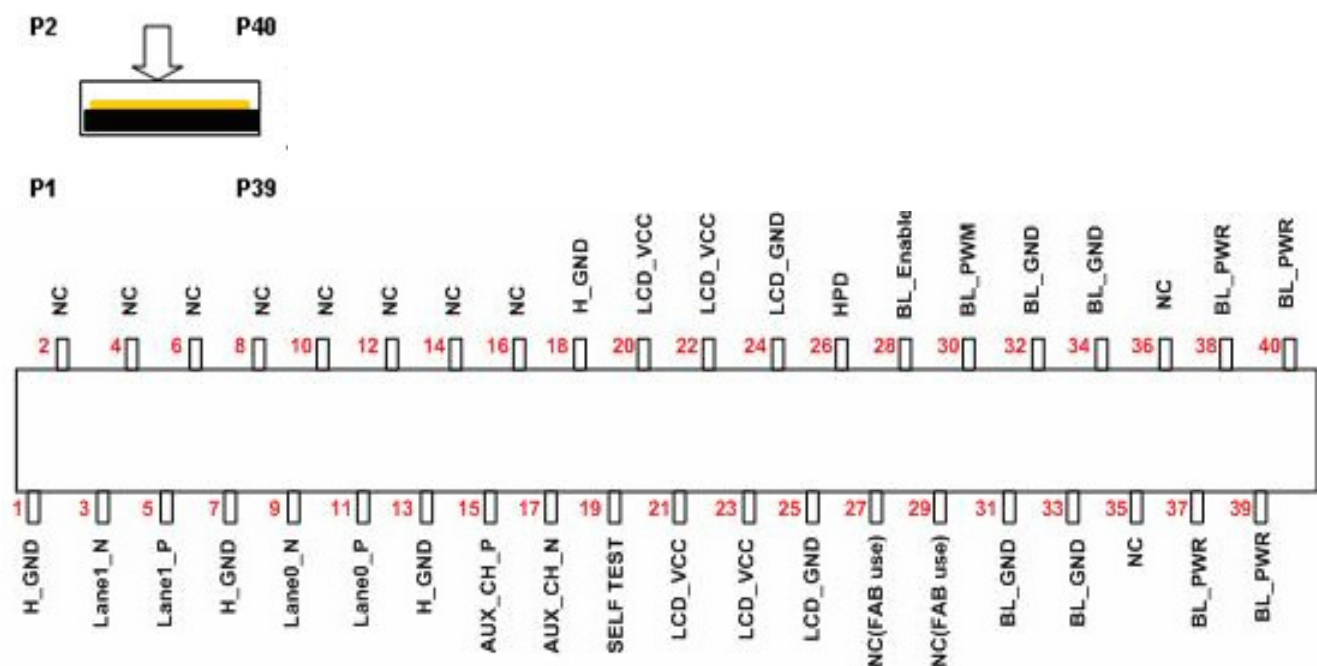
Connector Name / Designation	For Signal Connector
Manufacturer	DDK
Type / Part Number	FF12-40A-R12BN-D3
ting Housing/Part Number	FPC Cable

6.2.2 Pin Assignment

eDP lane is a differential signal technology for LCD interface and high speed data transfer device.

PIN NO	Symbol	Function
P1	H_GND	High Speed Ground
P2	NC	No Connect
P3	Lane1_N	Comp Signal Link Lane 1
P4	NC	No Connect
P5	Lane1_P	True Signal Link Lane 1
P6	NC	No Connect
P7	H_GND	High Speed Ground
P8	NC	No Connect
P9	Lane0_N	Comp Signal Link Lane 0
P10	NC	No Connect
P11	Lane0_P	True Signal Link Lane 0
P12	NC	No Connect
P13	H_GND	High Speed Ground
P14	NC	No Connect
P15	AUX_CH_P	True Signal Auxiliary Ch.
P16	NC	No Connect
P17	AUX_CH_N	Comp Signal Auxiliary Ch.
P18	H_GND	High Speed Ground
P19	LCD_Self_Test	LCD Panel Self Test Enable
P20	LCD_VCC	LCD logic and driver power

P21	LCD_VCC	LCD logic and driver power
P22	LCD_VCC	LCD logic and driver power
P23	LCD_VCC	LCD logic and driver power
P24	LCD_GND	LCD_ground
P25	LCD_GND	LCD_ground
P26	HPD	HPD signale pin
P27	NC	AUO FAB use EDID_DATA
P28	BL_Enable	LED driver IC enable
P29	NC	AUO FAB use EDID_CLK
P30	BL_PWM	LED driver IC PWM
P31	BL_GND	Backlight_ground
P32	BL_GND	Backlight_ground
P33	BL_GND	Backlight_ground
P34	BL_GND	Backlight_ground
P35	NC	No Connect
P36	NC	No Connect
P37	BL_PWR	Backlight power (5.5V~21V)
P38	BL_PWR	Backlight power (5.5V~21V)
P39	BL_PWR	Backlight power (5.5V~21V)
P40	BL_PWR	Backlight power (5.5V~21V)



6.4 Interface Timing

6.4.1 Timing Characteristics

Basically, interface timings should match the 1920 x 1080 /60 Hz manufacturing guide line timing.

Parameter		Symbol	Min.	Typ.	Max.	Unit
Frame Rate		---	50	60	---	Hz
Clock frequency		1/ T _{Clock}		141.4		MHz
Vertical Section	Period	T _V	1084	1118	1380	T _{Line}
	Active	T _{VD}	1080			
	Blanking	T _{VB}	4	38	300	
Horizontal Section	Period	T _H	2000	2108	2320	T _{Clock}
	Active	T _{HD}	1920			
	Blanking	T _{HB}	80	188	400	

Note1 : The above is as optimized setting

Note2 : DE mode only

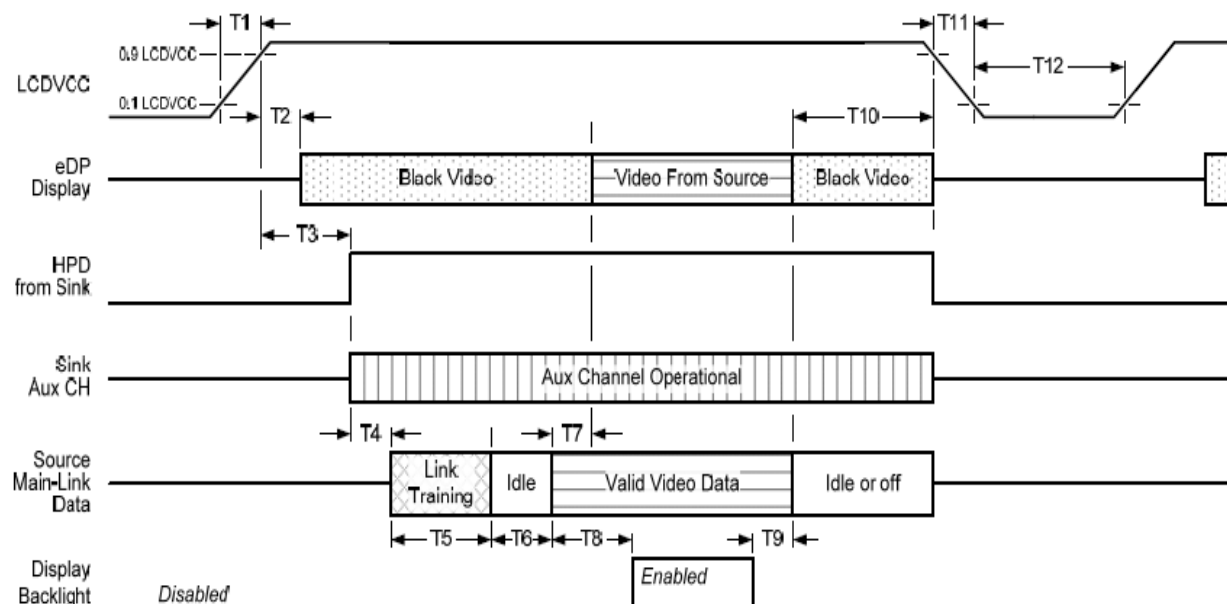
Note3 : The maximum clock frequency = $[(1920 + B) * (1080 + A) * 60] < 160\text{MHz}$

Note4 : Clock frequency number is for reference, real setting value refer to EDID (Clock frequency 141.4 MHz)

6.5 Power On Sequence

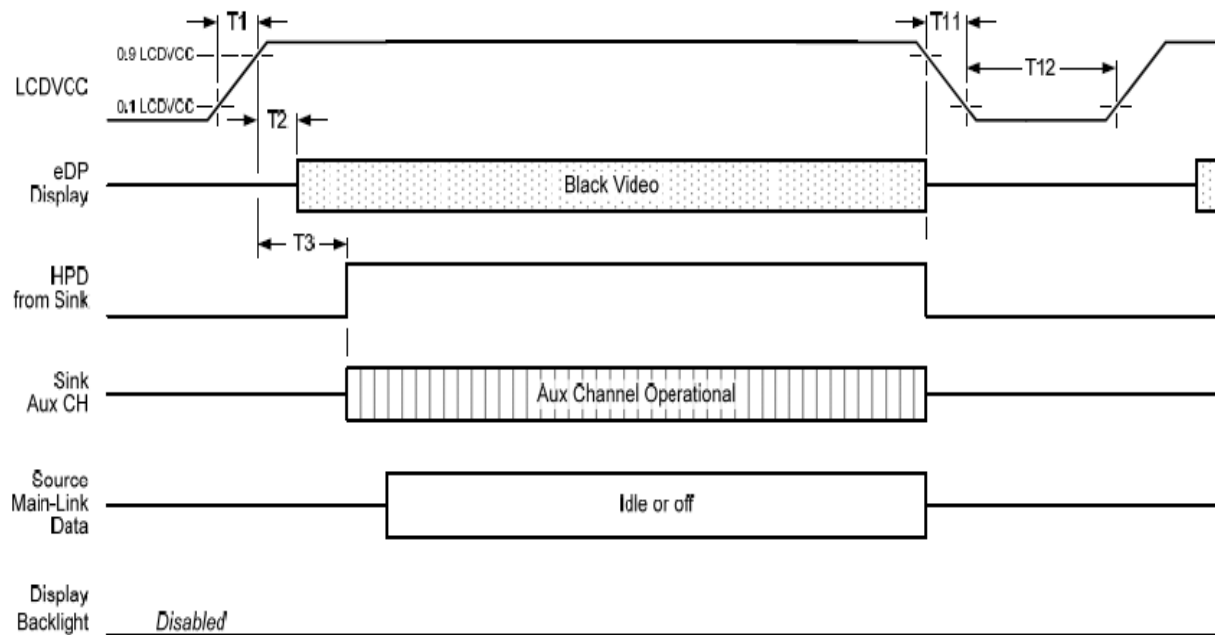
Power on/off sequence is as follows. Interface signals and LED on/off sequence are also shown in the chart.

Display Port panel power sequence:



Display port interface power up/down sequence, normal system operation

Display Port AUX_CH transaction only:



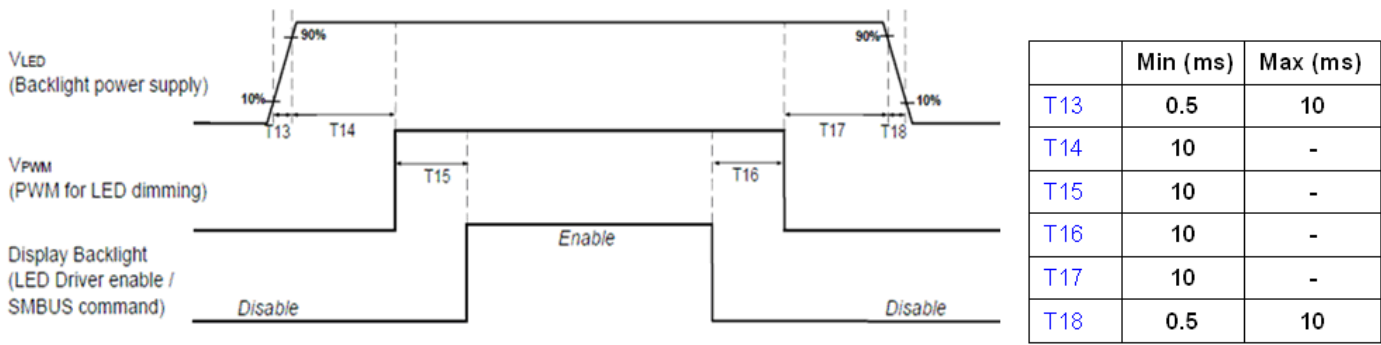
Display port interface power up/down sequence, AUX_CH transaction only

Display Port panel power sequence timing parameter:

Timing parameter	Description	Reqd. by	Limits			Notes
			Min.	Typ.	Max.	
T1	power rail rise time, 10% to 90%	source	0.5ms		10ms	
T2	delay from LCDVDD to black video generation	sink	0ms		200ms	prevents display noise until valid video data is received from the source
T3	delay from LCDVDD to HPD high	sink	0ms		200ms	sink AUX_CH must be operational upon HPD high.
T4	delay from HPD high to link training initialization	source				allows for source to read link capability and initialize.
T5	link training duration	source				dependant on source link to read training protocol.
T6	link idle	source				Min accounts for required BS-Idle pattern. Max allows for source frame synchronization.
T7	delay from valid video data from source to video on display	sink	0ms		50ms	max allows sink validate video data and timing.
T8	delay from valid video data from source to backlight enable	source				source must assure display video is stable.
T9	delay from backlight disable to end of valid video data	source				source must assure backlight is no longer illuminated.
T10	delay from end of valid video data from source to power off	source	0ms		500ms	
T11	power rail fall time, 90% to 10%	source			10ms	
T12	power off time	source	500ms			

- Note 1: The sink must include the ability to generate black video autonomously. The sink must automatically enable black video under the following conditions:
- upon LCDVDD power on (within T2 max)-when the "Novideostream_Flag" (VB-ID Bit 3) is received from the source (at the end of T9).
 - when no main link data, or invalid video data, is received from the source. Black video must be displayed within 64ms (typ) from the start of either condition. Video data can be deemed invalid based on MSA and timing information, for example.
- Note 2: The sink may implement the ability to disable the black video function, as described in Note 1, above, for system development and debugging purpose.
- Note 3: The sink must support AUX_CH polling by the source immediately following LCDVDD power on without causing damage to the sink device (the source can re-try if the sink is not ready). The sink must be able to respond to an AUX_CH transaction with the time specified within T3 max.

Display Port panel B/L power sequence timing parameter:



7. Panel Reliability Test

7.1 Vibration Test

Test Spec:

- Test method: Non-Operation
- Acceleration: 1.5 G
- Frequency: 10 - 500Hz Random
- Sweep: 30 Minutes each Axis (X, Y, Z)

7.2 Shock Test

Test Spec:

- Test method: Non-Operation
- Acceleration: 220 G , Half sine wave
- Active time: 2 ms
- Pulse: X,Y,Z .one time for each side

7.3 Reliability Test

Items	Required Condition	Note
Temperature Humidity Bias	Ta= 40°C , 90%RH, 300h	
High Temperature Operation	Ta= 50°C , Dry, 300h	
Low Temperature Operation	Ta= 0°C , 300h	
High Temperature Storage	Ta= 60°C , 300h	
Low Temperature Storage	Ta= -20°C , 300h	
Thermal Shock Test	Ta=-20°C to 60°C , Duration at 30 min, 100 cycles	
ESD	Contact : ±8 KV Air : ±15 KV	Note 1

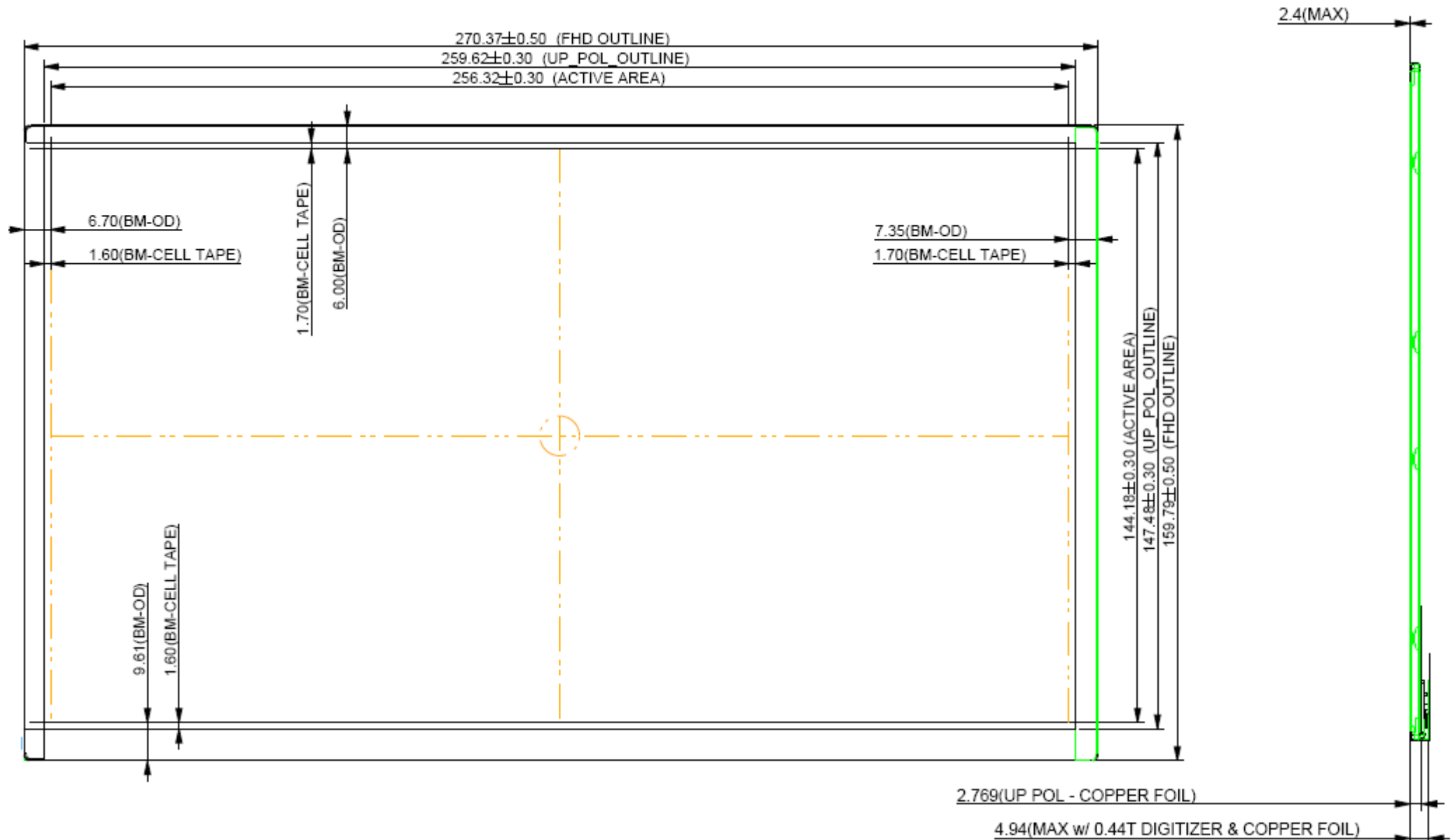
Note1: According to EN 61000-4-2 , ESD class B: Some performance degradation allowed.
Self-recoverable.

No data lost, No hardware failures.

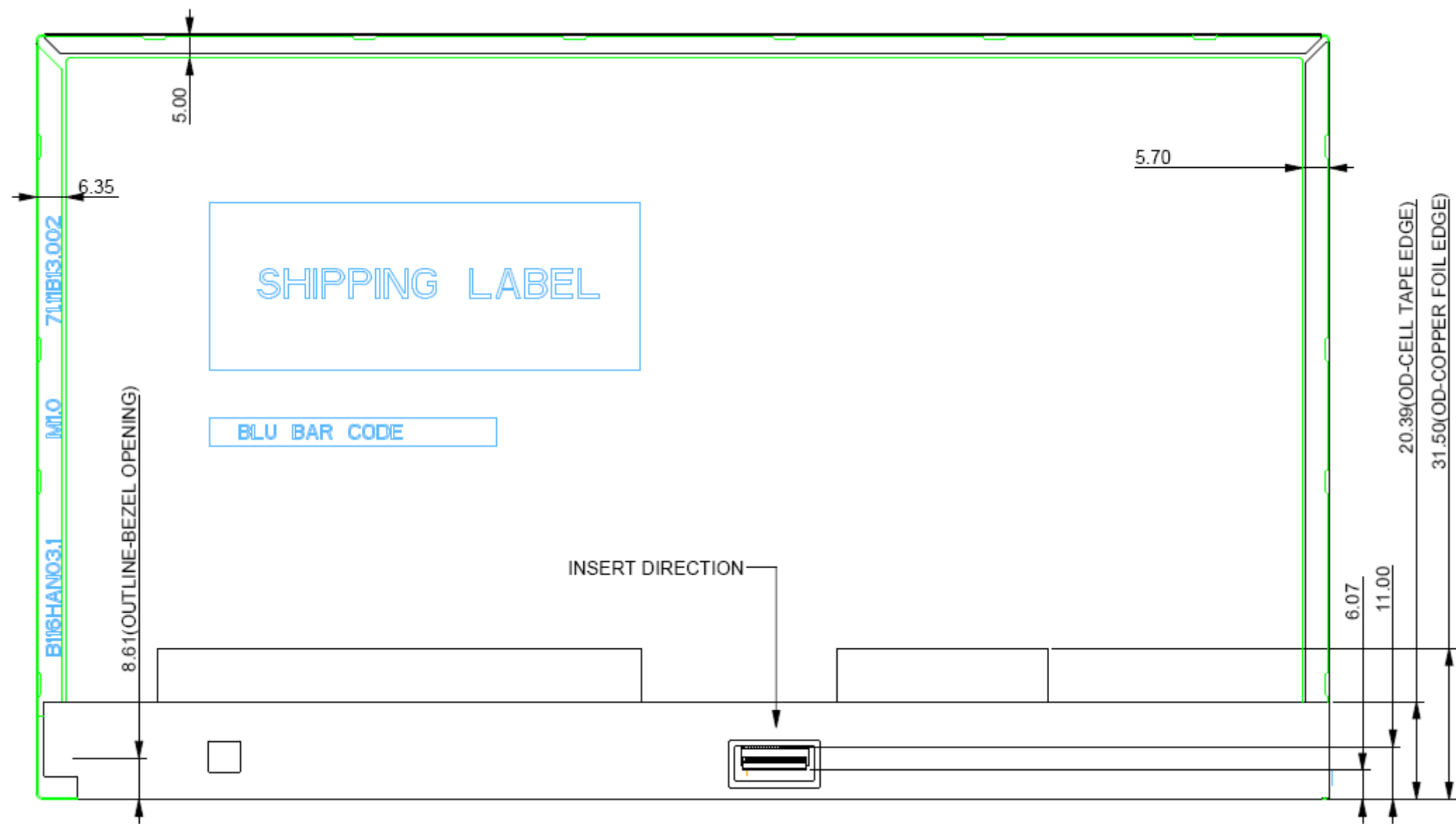
Remark: MTBF (Excluding the LED): 30,000 hours with a confidence level 90%

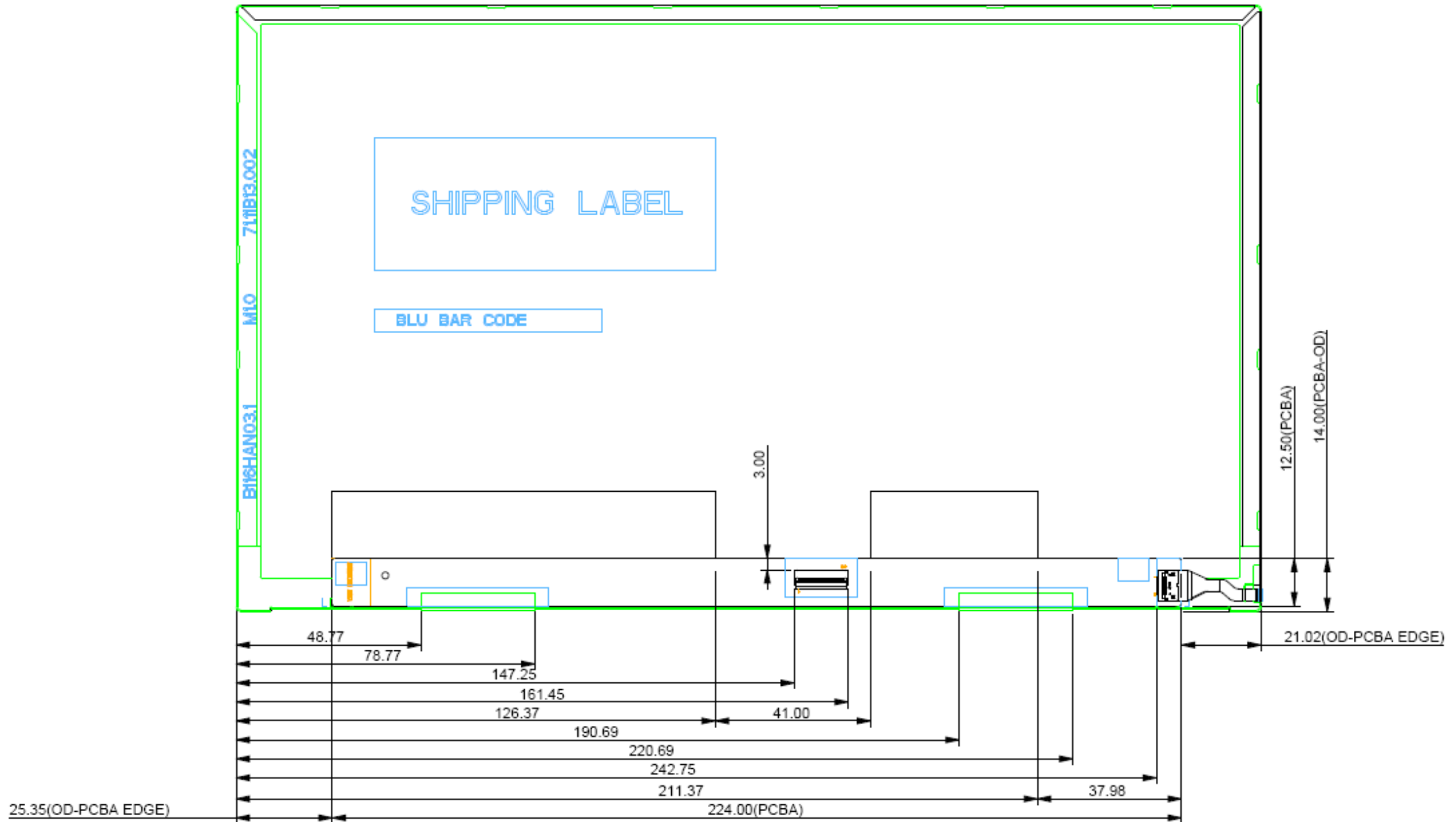
8. Mechanical Characteristics

8.1.1 Standard Front View



8.1.2 Standard Back View





9. Shipping and Package

9.1 Shipping Label Format

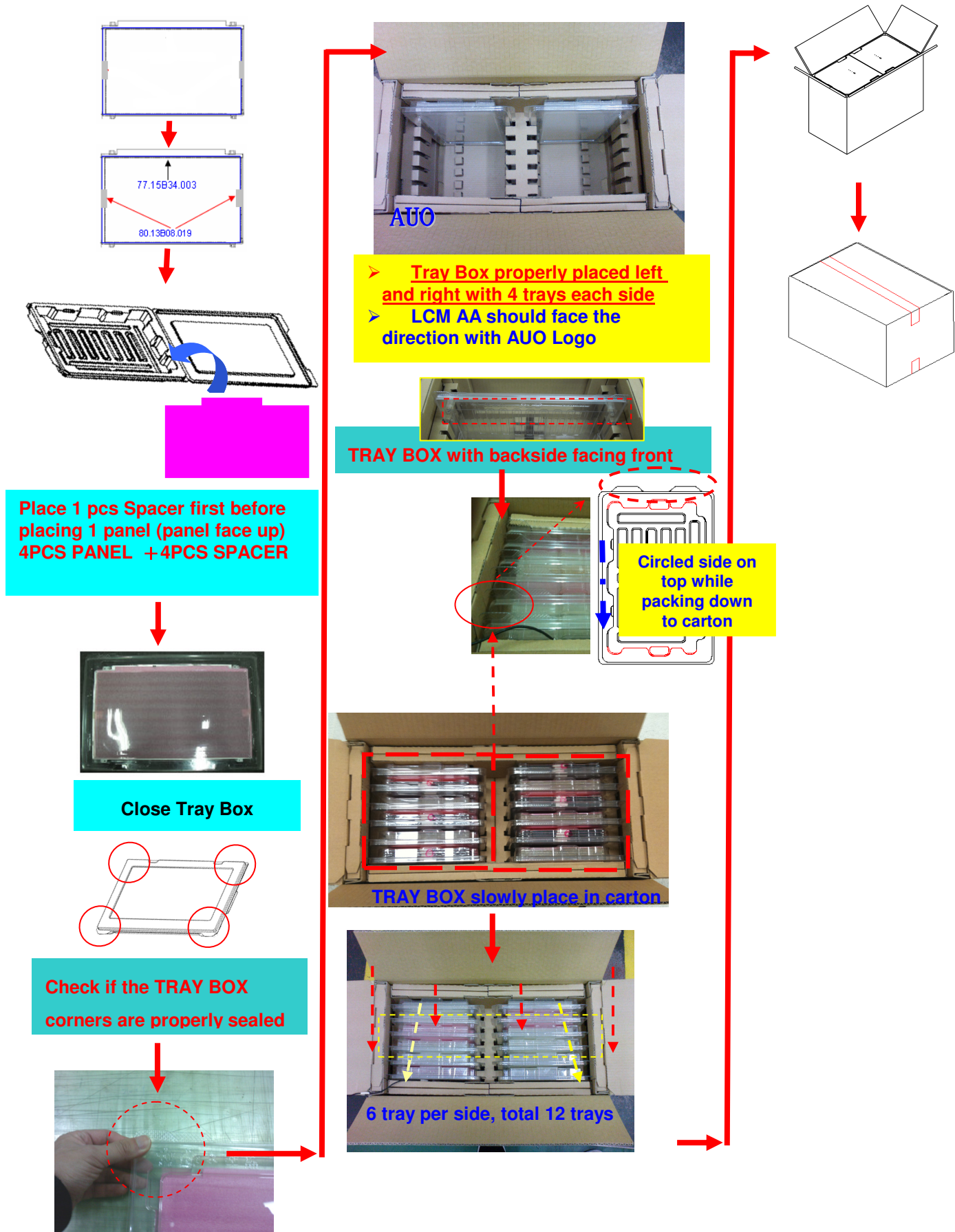
Shipping label

 *XXXXXXXXXXXXX.XXXXXX	Manufactured MM/WWV Model No: B116HAN03.1 AU Optronics Made in China (S01) H/W: 0A F/W:0	c  us  E204356  
 G33C0007R110		

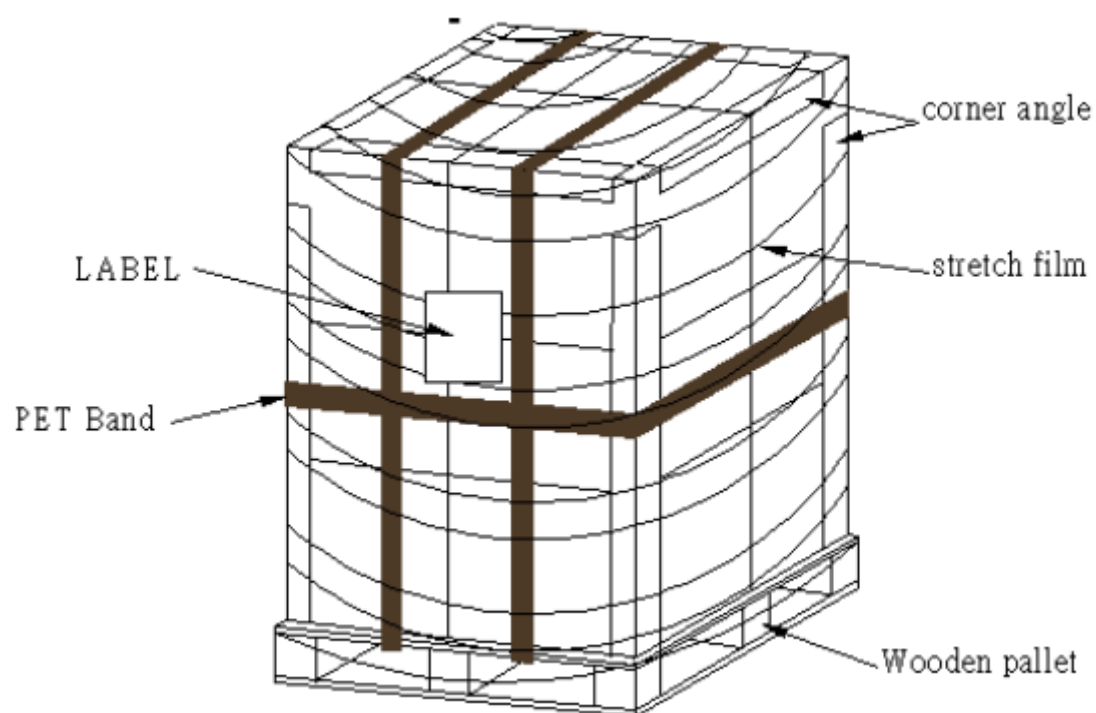
Carton Label

AU Optronics	QTY : 48	 
MODEL NO :	B116HAN03.1	
PART NO :	97.11B13.110	
CUSTOMER NO :	G33C0007R110	
CARTON NO :		
Made in China	****ZS0307-0822500037*	

9.2 Carton Package



9.3 Shipping Package of Palletizing Sequence



10. Appendix

10.1 EDID Description

Address	FUNCTION	Value	Value	Value	Note
HEX		HEX	BIN	DEC	
00	Header	00	00000000	0	
01		FF	11111111	255	
02		FF	11111111	255	
03		FF	11111111	255	
04		FF	11111111	255	
05		FF	11111111	255	
06		FF	11111111	255	
07		00	00000000	0	
08	EISA Manuf. Code LSB	06	00000110	6	
09	Compressed ASCII	AF	10101111	175	
0A	Product Code	5D	01011101	93	
0B	hex, LSB first	31	00110001	49	
0C	32-bit ser #	00	00000000	0	
0D		00	00000000	0	
0E		00	00000000	0	
0F		00	00000000	0	
10	Week of manufacture	14	00010100	20	
11	Year of manufacture	16	00010110	22	
12	EDID Structure Ver.	01	00000001	1	
13	EDID revision #	03	00000011	3	
14	Video input def. (<i>digital I/P, non-TMDS, CRGB</i>)	80	10000000	128	
15	Max H image size (<i>rounded to cm</i>)	1A	00011010	26	
16	Max V image size (<i>rounded to cm</i>)	0E	00001110	14	
17	Display Gamma (<i>=(gamma*100)-100</i>)	78	01111000	120	
18	Feature support (<i>no DPMS, Active OFF, RGB, tmq Blk#1</i>)	0A	00001010	10	
19	Red/green low bits (Lower 2:2:2:2 bits)	A4	10100100	164	
1A	Blue/white low bits (Lower 2:2:2:2 bits)	15	00010101	21	
1B	Red x (Upper 8 bits)	9E	10011110	158	
1C	Red y/ highER 8 bits	55	01010101	85	
1D	Green x	4E	01001110	78	
1E	Green y	9B	10011011	155	
1F	Blue x	26	00100110	38	
20	Blue y	0F	00001111	15	
21	White x	50	01010000	80	
22	White y	54	01010100	84	
23	Established timing 1	00	00000000	0	
24	Established timing 2	00	00000000	0	
25	Established timing 3	00	00000000	0	
26	Standard timing #1	01	00000001	1	
27		01	00000001	1	
28	Standard timing #2	01	00000001	1	
29		01	00000001	1	
2A	Standard timing #3	01	00000001	1	
2B		01	00000001	1	
2C	Standard timing #4	01	00000001	1	
2D		01	00000001	1	
2E	Standard timing #5	01	00000001	1	
2F		01	00000001	1	
30	Standard timing #6	01	00000001	1	
31		01	00000001	1	
32	Standard timing #7	01	00000001	1	
33		01	00000001	1	
34	Standard timing #8	01	00000001	1	
35		01	00000001	1	
36	Pixel Clock/10000 LSB	3D	00111101	61	
37	Pixel Clock/10000 USB	37	00110111	55	
38	Horz active Lower 8bits	80	10000000	128	
39	Horz blanking Lower 8bits	BC	10111100	188	
3A	HorzAct:HorzBlnk Upper 4:4 bits	70	01110000	112	
3B	Vertical Active Lower 8bits	38	00111000	56	
3C	Vertical Blanking Lower 8bits	26	00100110	38	
3D	Vert Act : Vertical Blanking (upper 4:4 bit)	40	01000000	64	
3E	HorzSync. Offset	3A	00111010	58	
3F	HorzSync.Width	2A	00101010	42	
40	VertSync.Offset : VertSync.Width	8E	10001110	142	
41	Horz&Vert Sync Offset/Width Upper 2bits	00	00000000	0	
42	Horizontal Image Size Lower 8bits	00	00000000	0	
43	Vertical Image Size Lower 8bits	90	10010000	144	
44	Horizontal & Vertical Image Size (upper 4:4 bits)	10	00010000	16	

45	Horizontal Border (zero for internal LCD)	00	00000000	0	
46	Vertical Border (zero for internal LCD)	00	00000000	0	
47	Signal (non-intr, norm, no stero, sep sync, neg pol)	18	00011000	24	
48	Detailed timing/monitor	00	00000000	0	
49	descriptor #2	00	00000000	0	
4A		00	00000000	0	
4B		0F	00001111	15	
4C		00	00000000	0	
4D		00	00000000	0	
4E		00	00000000	0	
4F		00	00000000	0	
50		00	00000000	0	
51		00	00000000	0	
52		00	00000000	0	
53		00	00000000	0	
54		00	00000000	0	
55		00	00000000	0	
56		00	00000000	0	
57		00	00000000	0	
58		00	00000000	0	
59		20	00100000	32	
5A	Detailed timing/monitor	00	00000000	0	
5B	descriptor #3	00	00000000	0	
5C		00	00000000	0	
5D		FE	11111110	254	
5E		00	00000000	0	
5F	Manufacture	41	01000001	65	A
60	Manufacture	55	01010101	85	U
61	Manufacture	4F	01001111	79	O
62		0A	00001010	10	
63		20	00100000	32	
64		20	00100000	32	
65		20	00100000	32	
66		20	00100000	32	
67		20	00100000	32	
68		20	00100000	32	
69		20	00100000	32	
6A		20	00100000	32	
6B		20	00100000	32	
6C	Detailed timing/monitor	00	00000000	0	
6D	descriptor #4	00	00000000	0	
6E		00	00000000	0	
6F		FE	11111110	254	
70		00	00000000	0	
71	Manufacture P/N	42	01000010	66	B
72	Manufacture P/N	31	00110001	49	1
73	Manufacture P/N	31	00110001	49	1
74	Manufacture P/N	36	00110110	54	6
75	Manufacture P/N	48	01001000	72	H
76	Manufacture P/N	41	01000001	65	A
77	Manufacture P/N	4E	01001110	78	N
78	Manufacture P/N	30	00110000	48	0
79	Manufacture P/N	33	00110011	51	3
7A	Manufacture P/N	2E	00101110	46	.
7B	Manufacture P/N	31	00110001	49	1
7C		20	00100000	32	
7D		0A	00001010	10	
7E	Extension Flag	00	00000000	0	
7F	Checksum	AE	10101110	174	
			SUM	6144	
			SUM to HEX	1800	