MOS INTEGRATED CIRCUITS

M 120D

1024 BIT - NON VOLATILE RANDOM ACCESS MEMORY (NV-RAM)

- 256 x 4 ORGANIZATION
- OPTIMUM DATA RETENTION
- DESIGNED FOR APPLICATIONS REQUIRING 10^4 MODIFY OPERATIONS PER BIT
- 950 ns ACCESS TIME
- INTERNAL WORD MODIFY TIME LESS THAN 100 ms.
- "MODIFY END" OUTPUT LINE
- TTL COMPATIBLE: EASY CONNECTION TO ANY MICROPROCESSOR
- COMMON DATA INPUTS AND OUTPUTS
- ON CHIP LATCHES FOR ADDRESSES AND DATA
- POWER SUPPLIES $V_{DD} = 12V \pm 10\%$
  $V_{PP} = 25V \pm 5\%$
- STANDARD 18-PIN DUAL-IN-LINE PACKAGE

The M120D is a Non Volatile Random Access Memory (NV-RAM). The contents of every word (256 x 4 available on-chip) can be erased and written electrically and data is retained without power supply for 100 years (calculated from test results). SGS-ATES proprietary n-channel, Si-gate, double Polysilicon MOS Technology insures maximum reliability and data retention and allows any number of read operations. Thanks to an internal circuit taking care of the modify sequence, access times for both read and modify operations are short enough to allow use with most microprocessors. The M120D is mainly intended for applications where it is used in combination with a microprocessor. In these applications all the signals are supplied by the microcomputer I/O ports, and the access time required is always in the range of microseconds. The M120D is available in a standard 18-pin dual-in-line plastic or ceramic package (frit-seal).

ABSOLUTE MAXIMUM RATINGS

	Input or output voltages (except V_{DD} and V_{PP})	-0.5 to 15	V
V_{DD}	Supply voltage	-0.5 to 20	V
V_{PP}	Supply voltage	-0.5 to 28	V
P_{tot}	Total power dissipation	1	W
T_{stg}	Storage temperature range	-65 to 150	°C
T_{op}	Operating temperature range	0 to 70	°C

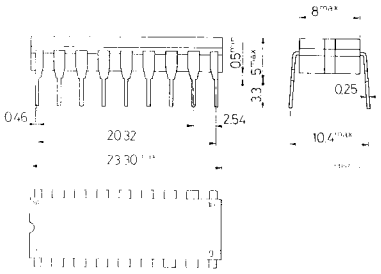
Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operating conditions of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ORDERING NUMBERS: M120D F1 for dual in-line ceramic package (frit seal)
M120D B1 for dual in-line plastic package

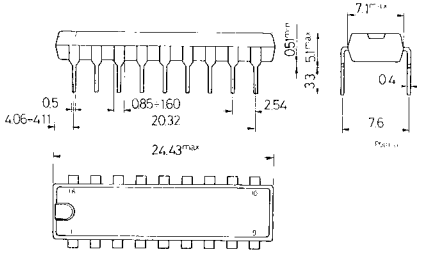
M 120D

MECHANICAL DATA (dimensions in mm)

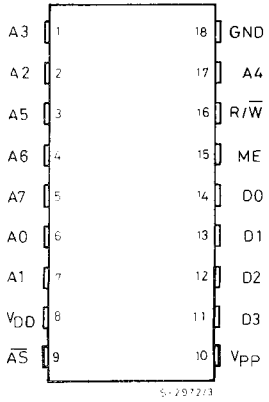
Dual in-line ceramic package, frit-seal



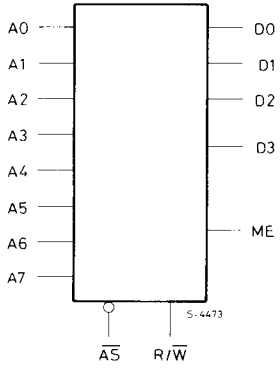
Dual in-line plastic package



PIN CONNECTIONS



LOGIC DIAGRAM



PIN NAMES

D0–D3	DATA INPUTS/OUTPUTS (OPEN DRAIN)
A0–A7	ADDRESS INPUTS
$\overline{AS}$	ADDRESS STROBE INPUT
R/$\overline{W}$	READ/WRITE INPUT
ME	MODIFY END OUTPUT (OPEN DRAIN)
V_{PP}	POWER (+25V)
V_{DD}	POWER (+12V)
GND	GROUND

DC AND OPERATING CHARACTERISTICS (T_{amb} = 0°C to 70°C, V_{DD} = +12V ± 10%, V_{PP} = +25V ± 5%)

Parameter		Test conditions	Values			Unit
			Min.	Typ.*	Max.	
I_{DD1}	Average V_{DD} supply current				35	mA
I_{PP1}	Average V_{PP} supply current				25	mA
I_{DD2}	Standby V_{DD} supply current	$\overline{AS}$ @ V_{IH}			25	mA
I_{PP2}	Standby V_{PP} supply current	$\overline{AS}$ @ V_{IH}			15	mA
V_{IH}	Input high voltage		2.4	5		V
V_{IL}	Input low voltage		-0.3	0	0.6	V
V_{OL}	Output low voltage	I_{OL} = 1.6 mA			0.4	V
I_{LI}	Input leakage current				10	µA
I_{LO}	Output leakage current				10	µA

* Typical values are at +25°C and nominal voltages.

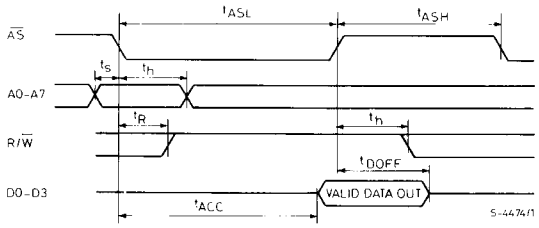
AC CHARACTERISTICS

Parameter		Values			Unit
		Min.	Typ.	Max.	
t_s	Set-up time	100			ns
t_h	Hold time	250			ns
t_{ASL}	$\overline{AS}$ active time	950			ns
t_{ASH}	$\overline{AS}$ inactive time	500			ns
t_R	$\overline{AS}$ ↓ to R/$\overline{W}$ ↑ (Read)			100	ns
t_{ACC}	Access time from $\overline{AS}$ ↓			950	ns
t_{DOFF}	Data output turn-off delay			350	ns
t_M	Modify time (1) from R/$\overline{W}$ ↑			100	ms
t_{WHE}	$\overline{AS}$ ↓ to R/$\overline{W}$ ↓ (Early write) (2) (3)			200	ns
t_{WE}	$\overline{AS}$ ↓ to R/$\overline{W}$ ↑ (Early Write)	950		100K	ns
t_{MHE}	ME turn-on delay from $\overline{AS}$ ↓ (Early Write)			950	ns
t_{AS}	R/$\overline{W}$ ↓ to $\overline{AS}$ ↑ rising edge (Read/Write)	500			ns
t_{WH}	$\overline{AS}$ ↓ to R/$\overline{W}$ ↓ (Read/Write)	250			ns
t_{WL}	R/$\overline{W}$ Low time (Read/Write)	700		100K	ns
t_{DF}	Data Float from $\overline{AS}$ ↓ (Read/Write)	200			ns
t_{MH}	ME turn-on delay from R/$\overline{W}$ ↓ (Read/Write)			650	ns

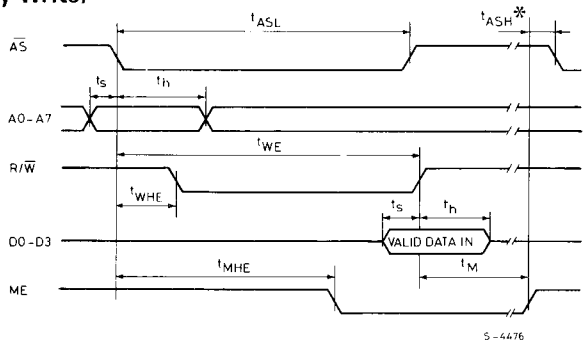
Notes:
1) See description of operation.
2) If $t_{WHE} \leqslant t_{WHE\ max}$ then D_{OUT} remains floating and there is no conflict between D_{OUT} and D_{IN}.
3) t_{WHE} can be < 0.

TIMING WAVEFORMS

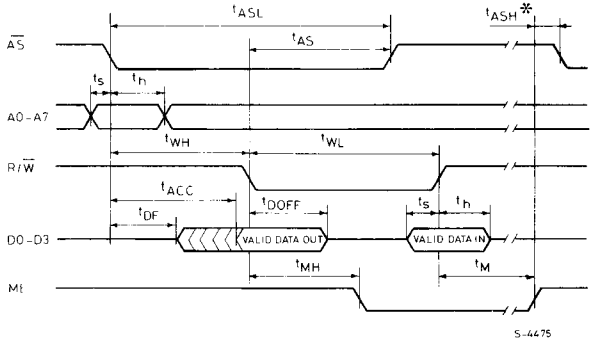
Read Cycle



Modify Cycle (Early Write)



Modify Cycle (Read/Write)



* The first falling edge of $\overline{AS}$ following the end of a modify cycle must occur at least t_{ASH} after the positive edge of ME.

DESCRIPTION OF OPERATION

M120D operation is controlled by the Address Strobe ($\overline{AS}$) control input (active low), which also performs the device selection function.
The device is deselected (Stand-by Mode) by a high level on $\overline{AS}$ input.
The falling edge of $\overline{AS}$ latches Address lines (A0 ÷ A7) contents into the chip and starts both read and modify cycles.
If R/$\overline{W}$ remains high while $\overline{AS}$ is active a **Read Cycle** occurs. The contents of the addressed memory location will be available on the Data lines (D0 ÷ D3) after an access time (t_{ACC}) from the leading edge of $\overline{AS}$. The trailing edge of $\overline{AS}$ three-states data lines after t_{DOFF} delay.
If R/$\overline{W}$ is or becomes low while $\overline{AS}$ is active a **Modify Cycle** starts.
Depending on timing relationships between the $\overline{AS}$ and R/$\overline{W}$ leading edges, there are two possible modify sequences.
An **Early Write** Modify cycle will be initiated if a falling edge of R/$\overline{W}$ occurs before the falling edge of $\overline{AS}$ or if a maximum of t_{WHE} occurs *after* the falling edge of $\overline{AS}$.
All timing relationships are related to the falling edge of $\overline{AS}$ and Data lines are not driven by the M120D thus avoiding any possible bus contention in this mode.
If R/$\overline{W}$ falling edge occurs a minimum of t_{WH} after the $\overline{AS}$ falling edge a **Read/Write** Modify Cycle procedes. Most timing relationships are in this case related to the R/$\overline{W}$ falling edge. Because until R/$\overline{W}$ becomes active, the M120D assumes a read cycle is in process, the device will output addressed location contents on Data lines according to t_{DF}, t_{ACC} and t_{WH} timing specifications.
This allows a read/write operation to be performed but might also cause contention on data lines. However if set-up time requirements are satisfied, the M120D will operate properly since it floats data lines before latching data input.

INTERNAL MODIFY OPERATION AND "ME" OUTPUT

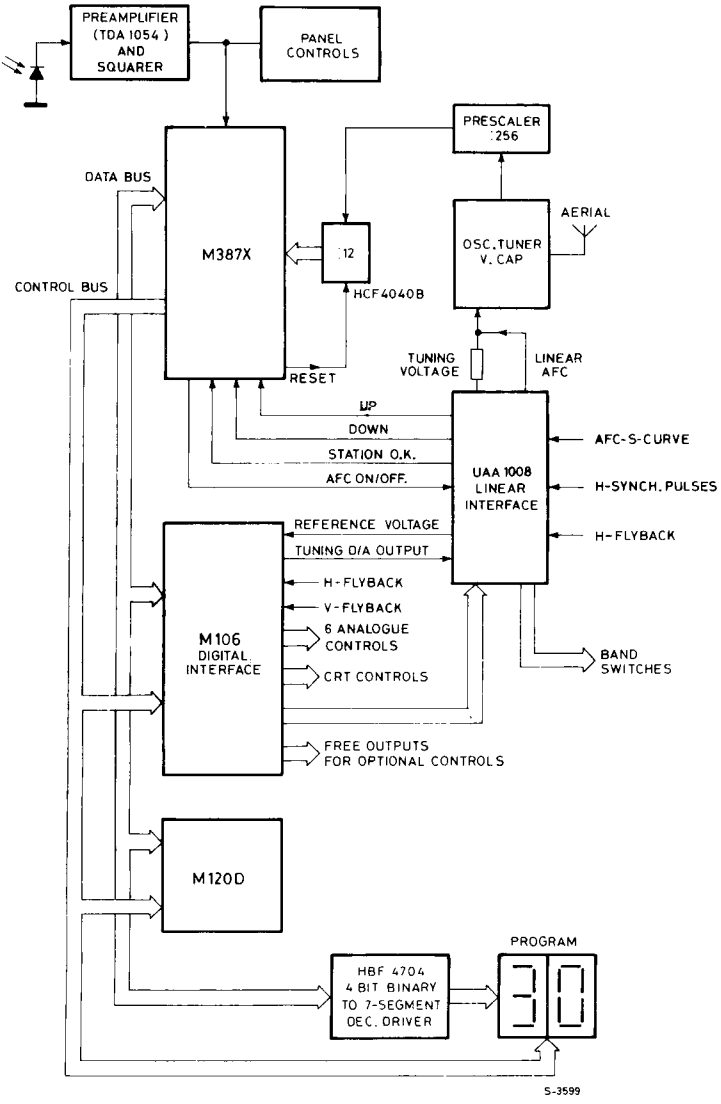
At the rising edge of R/$\overline{W}$ in a modify cycle the contents of data lines are latched and the internal modify cycle starts.
The ME output, which indicates Modify Cycle End, goes false (low) after a delay of either t_{MHE} from the $\overline{AS}$ leading edge (Early Write Modify Cycle) or t_{MH} from the R/$\overline{W}$ falling edge (Read/Write Modify Cycle). As long as ME is false the device is internally disconnected from buses and control lines, data outputs are floating and no further external operation will be acknowledged by M120D.
During internal modify cycle an on-chip circuitry performs a bit by bit comparison between "old" and "new" data word and according to this result writes, erases or leaves unchanged each single bit of the addressed location.
At modify completion (t_M) ME line becomes true again and M120D is again available for external access.
The M120D has been designed to meet applications requiring up to 10^4 modify operations with $T_M \leqslant 100$ msec. T_M is about 1 ms for the first modify operations and increases with the number of modify operations.
T_M is relative to each bit of the device so that, if not all the memory size is required, the overall life can be extended simply using a new section of the memory when t_M for the used section is above 100 msec.
If "old" and "new" data are equal then modify time is shorter than 100 μsec.

POWER-UP AND POWER-DOWN

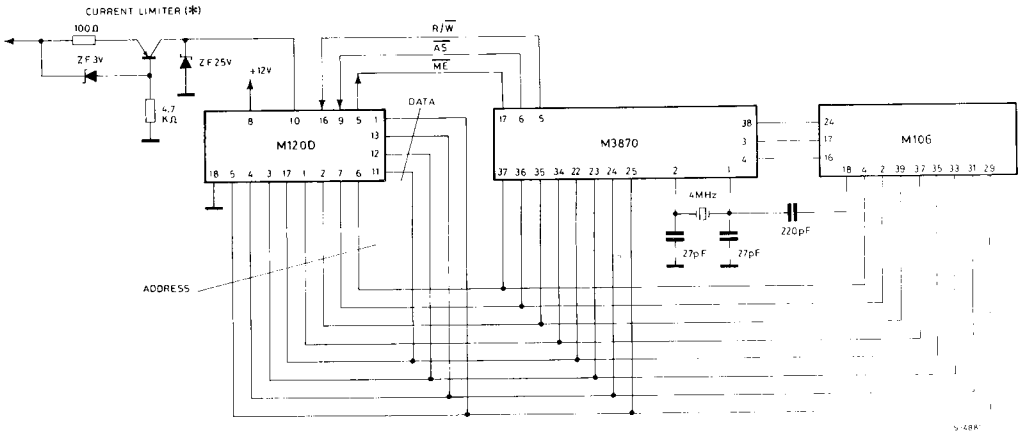
In order to avoid a spurious modify cycle, care should be taken during the power up sequence to ensure that $\overline{AS}$ and R/$\overline{W}$ are at the non-active (high) level before V_{DD} and V_{PP} reach half their operating value.
The opposite sequence should be followed during the power-down.
Power-up and power-down sequences can start arbitrarily with either V_{DD} or V_{PP}.

TYPICAL APPLICATION

Frequency synthesis digital tuning system



I.C. connections for the frequency synthesis application



(*) This circuit is necessary when Vpp maximum rating can be exceeded, even if for short periods as voltage spikes.