

MOS FIELD EFFECT POWER TRANSISTORS

2SK1756/2SK1757

SWITCHING

N-CHANNEL POWER MOS FET

INDUSTRIAL USE

DESCRIPTION

The 2SK1756/2SK1757 is N-channel MOS Field Effect Transistor designed for high voltage switching applications.

FEATURES

- Low On-state Resistance
 $R_{DS(on)} = 0.5/0.6 \Omega \text{ MAX. (} V_{GS} = 10 \text{ V, } I_D = 8 \text{ A)}$
- Low C_{iss} $C_{iss} = 1500 \text{ pF TYP.}$
- Built-in G-S Gate Protection Diode
- High Avalanche Capability Ratings

QUALITY GRADE

Standard

Please refer to "Quality grade on NEC Semiconductor Devices" (Document number IEI-1209) published by NEC Corporation to know the specification of quality grade on the devices and its recommended applications.

ABSOLUTE MAXIMUM RATINGS ($T_a = 25^\circ\text{C}$)

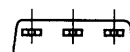
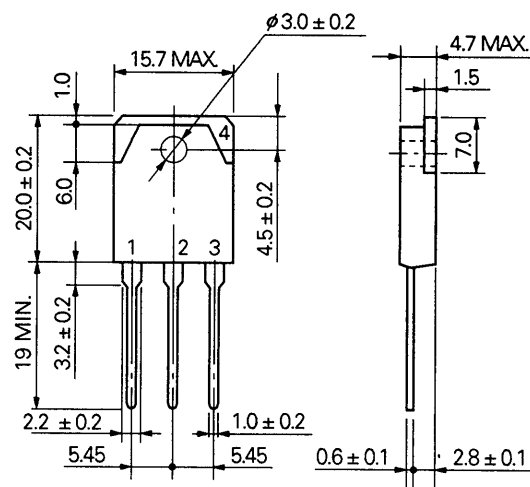
Drain to Source Voltage	V_{DSS}	450/500	V
Gate to Source Voltage	V_{GSS}	± 30	V
Drain Current (DC)	$I_{D(DC)}$	± 15	A
Drain Current (pulse)	$I_{D(pulse)}^*$	± 60	A
Total Power Dissipation ($T_c = 25^\circ\text{C}$)	P_T	120	W
Channel Temperature	T_{ch}	150	$^\circ\text{C}$
Storage Temperature	T_{stg}	-55 to $+150$	$^\circ\text{C}$
Single Avalanche Current	I_{AS}^{**}	22.5	A
Single Avalanche Energy	E_{AS}^{**}	362	mJ

* $PW \leq 10 \mu\text{s}$, Duty Cycle $\leq 1\%$

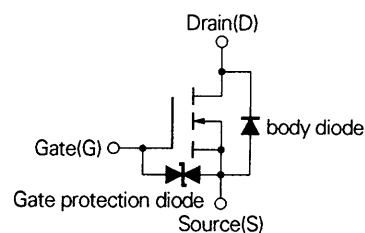
** Starting $T_{ch} = 25^\circ\text{C}$, $R_g = 25 \Omega$, $V_{GS} = 20 \text{ V} \rightarrow 0$

PACKAGE DIMENSIONS

(in millimeters)



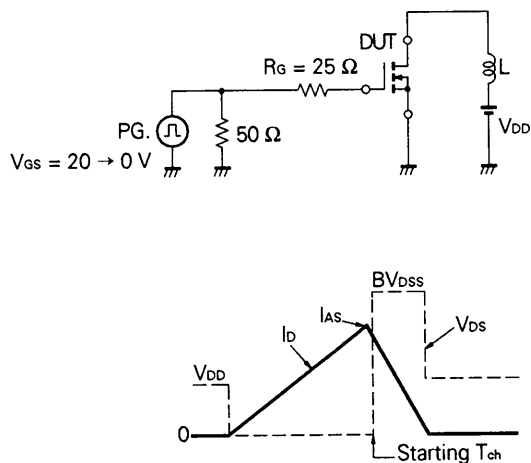
1. Gate
2. Drain
3. Source
4. Fin (Drain)



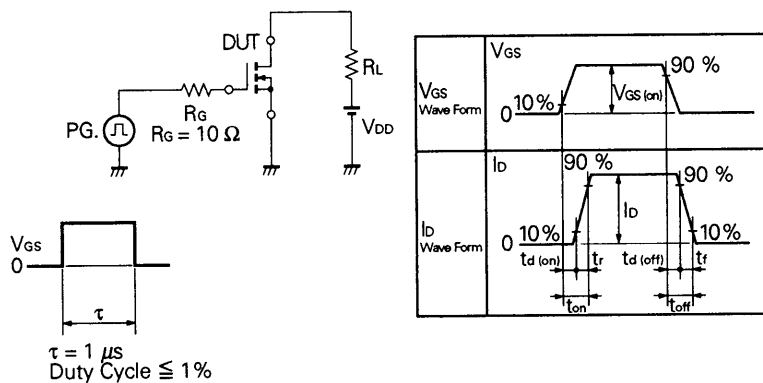
ELECTRICAL CHARACTERISTICS (T_a = 25 °C)

CHARACTERISTIC	SYMBOL	MIN.	TYP.	MAX.	UNIT	TEST CONDITION
Drain to Source On-state Resistance (2SK1756)	R _{DS(on)}		0.4	0.5	Ω	V _{GS} = 10 V, I _D = 8 A
Drain to Source On-state Resistance (2SK1757)	R _{DS(on)}		0.5	0.6	Ω	
Gate to Source Cutoff Voltage	V _{GS(off)}	2.5		3.5	V	V _{DS} = 10 V, I _D = 1 mA
Forward Transfer Admittance	y _{fs}	5.0	6.8		S	V _{DS} = 10 V, I _D = 8 A
Drain Leakage Current (2SK1756/1757)	I _{DSS}			100	μA	V _{DS} = 450/500 V, V _{GS} = 0
Gate to Source Leakage Current	I _{GSS}			±10	μA	V _{GS} = ±30 V, V _{DS} = 0
Input Capacitance	C _{iss}		1 500		pF	V _{DS} = 10 V V _{GS} = 0 f = 1 MHz
Output Capacitance	C _{oss}		480		pF	
Reverse Transfer Capacitance	C _{rss}		200		pF	
Turn-On Delay Time	t _{d(on)}		25		ns	V _{GS} = 10 V V _{DD} = 150 V I _D = 8 A, R _G = 10 Ω R _L = 18.8 Ω
Rise Time	t _r		55		ns	
Turn-Off Delay Time	t _{d(off)}		90		ns	
Fall Time	t _f		30		ns	
Total Gate Charge	Q _G		50		nC	V _{GS} = 10 V I _D = 15 A V _{DD} = 400 V
Gate to Source Charge	Q _{GS}		10		nC	
Gate to Drain Charge	Q _{GD}		30		nC	
Diode Forward Voltage	V _{F(S-D)}		1.0		V	I _D = 15 A, V _{GS} = 0
Reverse Recovery Time	t _{rr}		520		ns	I _D = 15 A, V _{GS} = 0 di/dt = 50 A/μs
Reverse Recovery Charge	Q _{rr}		8.3		μC	

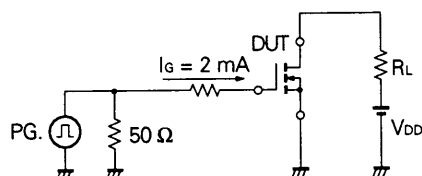
Test Circuit 1: Avalanche Capability



Test Circuit 2: Switching Time

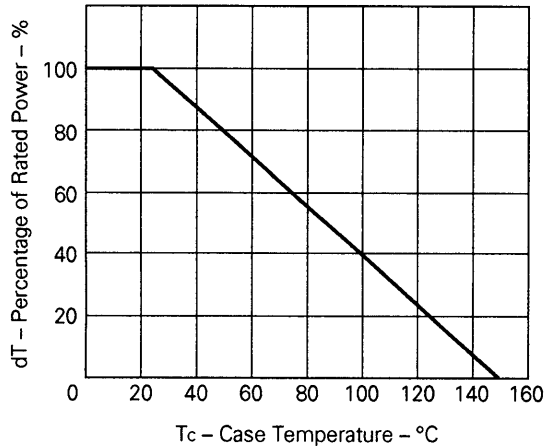


Test Circuit 3: Gate Charge

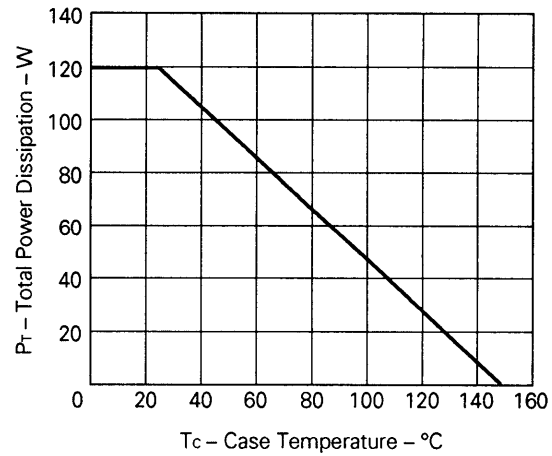


TYPICAL CHARACTERISTICS ($T_a = 25^\circ\text{C}$)

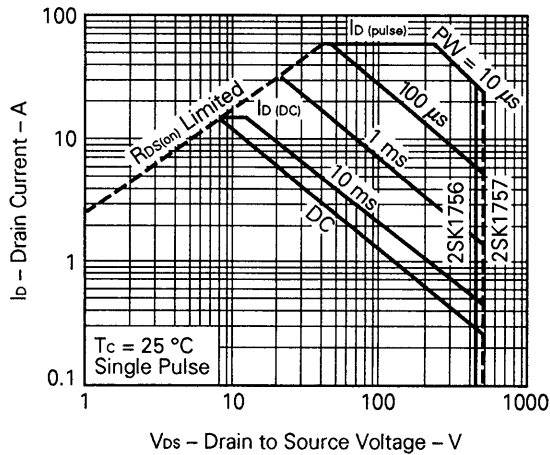
DERATING FACTOR OF FORWARD BIAS
SAFE OPERATING AREA



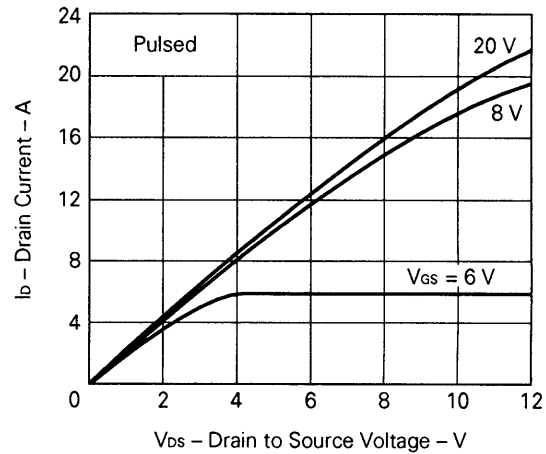
TOTAL POWER DISSIPATION vs.
CASE TEMPERATURE



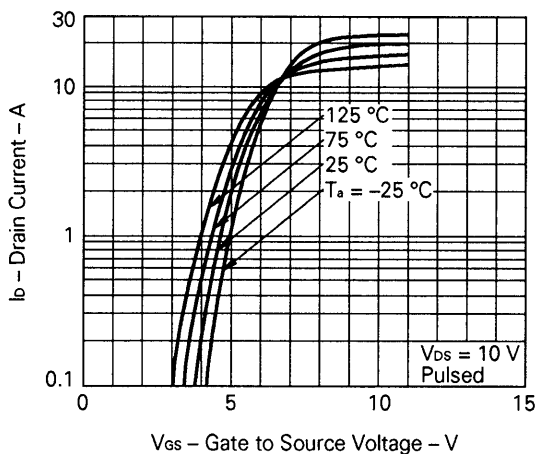
FORWARD BIAS SAFE OPERATING AREA



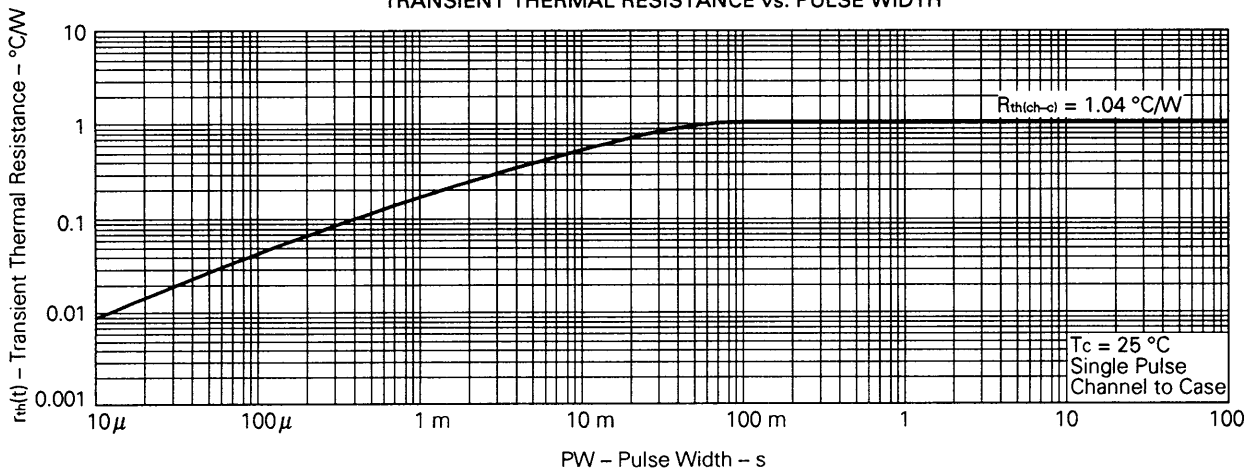
DRAIN CURRENT vs.
DRAIN TO SOURCE VOLTAGE



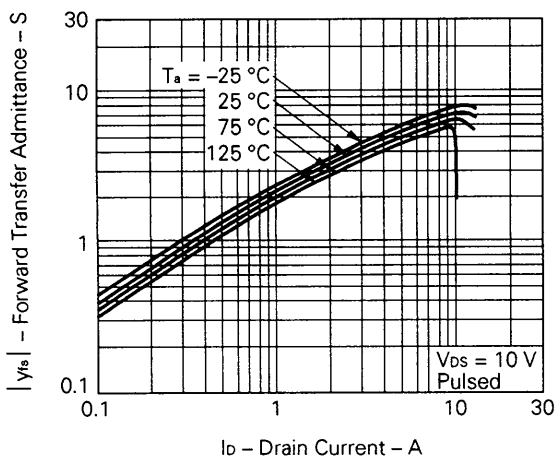
TRANSFER CHARACTERISTICS



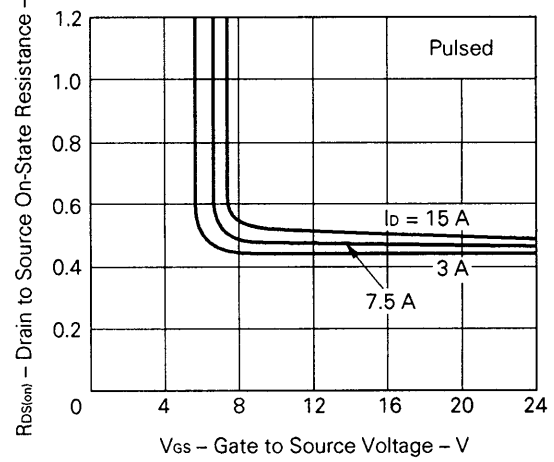
TRANSIENT THERMAL RESISTANCE vs. PULSE WIDTH



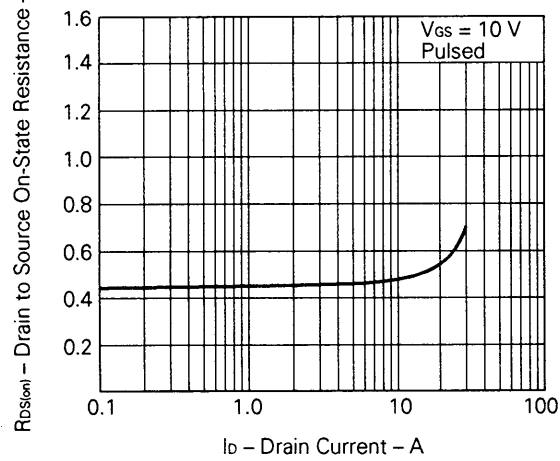
FORWARD TRANSFER ADMITTANCE vs. DRAIN CURRENT



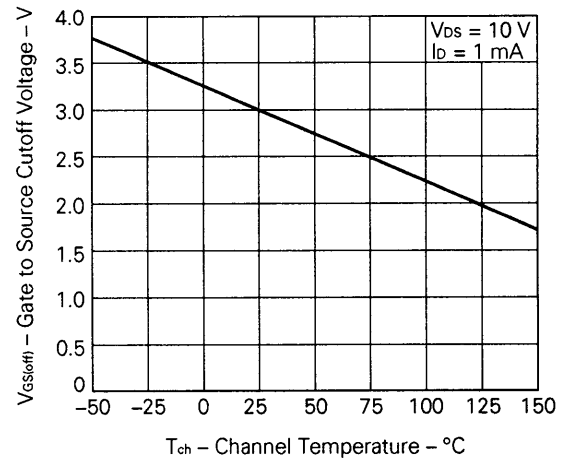
DRAIN TO SOURCE ON-STATE RESISTANCE vs. GATE TO SOURCE VOLTAGE

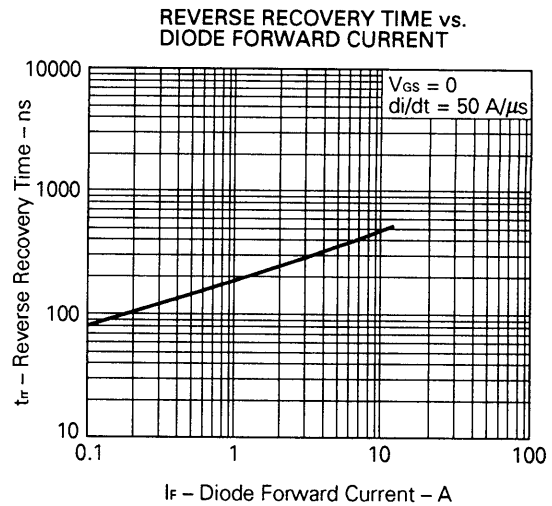
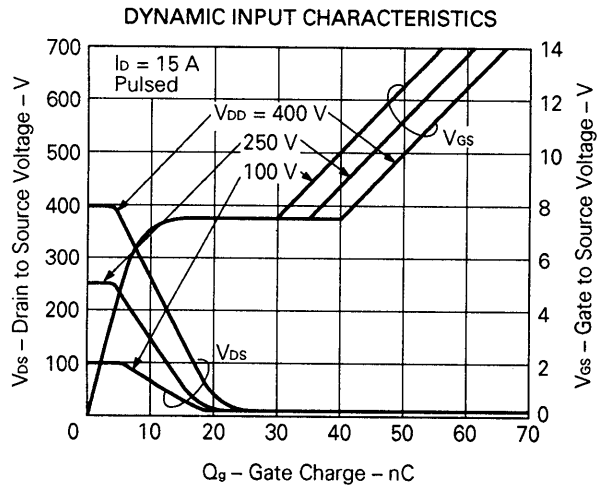
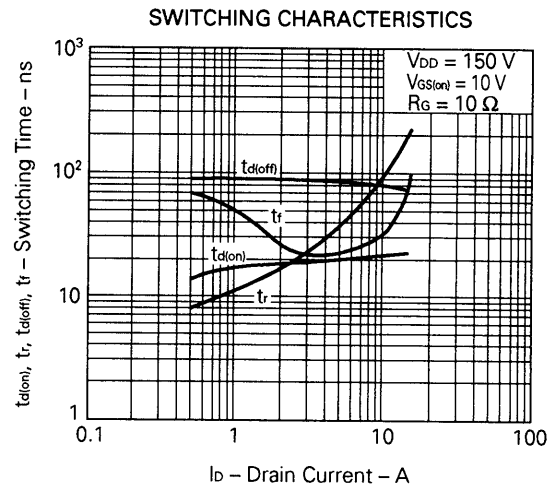
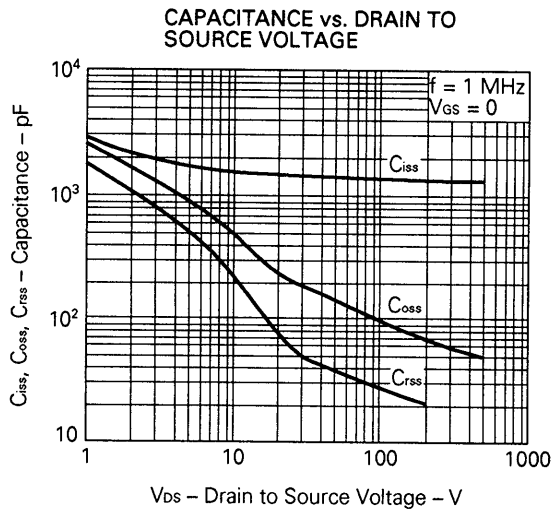
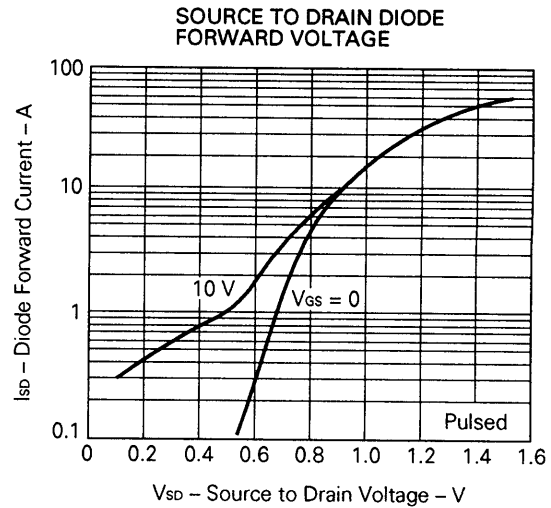
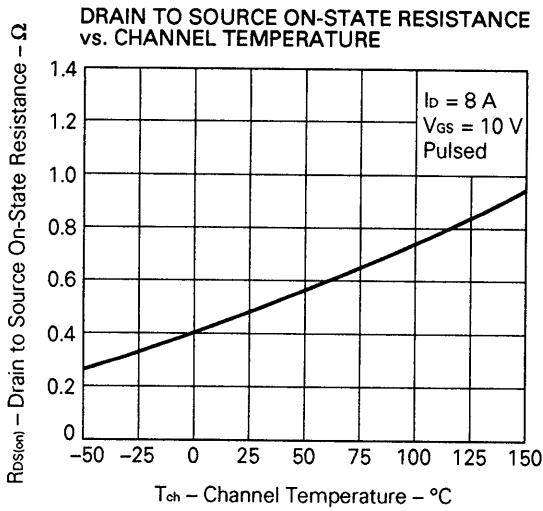


DRAIN TO SOURCE ON-STATE RESISTANCE vs. DRAIN CURRENT

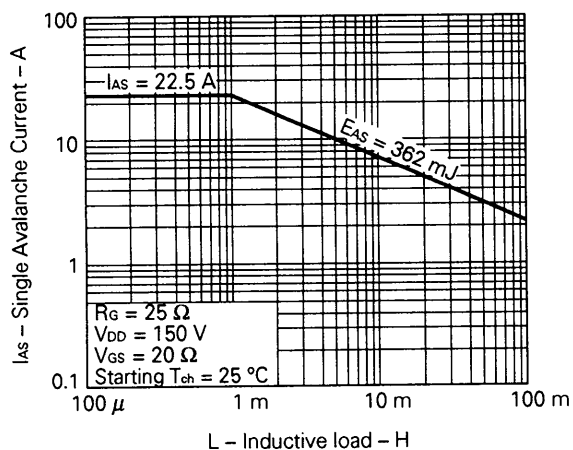


GATE TO SOURCE CUTOFF VOLTAGE vs. CHANNEL TEMPERATURE





SINGLE AVALANCHE CURRENT vs.
INDUCTIVE LOAD



SINGLE AVALANCHE ENERGY vs.
STARTING CHANNEL TEMPERATURE

