(V) Preliminary Specification
( ) Final Specification

Module	**11.6” (11.56”) HD 16:9 Color TFT-LCD**
Model Name	**B116XW05 V006**
Note	***Without Backlight and LED driving circuit design***

Customer	**Date**
Checked & Approved by	**Date**
Note: This Specification is subject to change without notice.	

Approved by	**Date**
Ch Lin	05/27/2011
Prepared by	**Date**
Jonken Fan	05/27/2011
NBBU Marketing Division **AU Optronics corporation**	

Contents

Record of Revision

Version and Date	Page	Old description	New Description	Remark
1 2011/05/27 0.1	All	First Edition for Customer		

1. Handling Precautions

1) Since front polarizer is easily damaged, pay attention not to scratch it.
2) Be sure to turn off power supply when inserting or disconnecting from input connector.
3) Wipe off water drop immediately. Long contact with water may cause discoloration or spots.
4) When the panel surface is soiled, wipe it with absorbent cotton or other soft cloth.
5) Since the panel is made of glass, it may break or crack if dropped or bumped on hard surface.
6) Since CMOS LSI is used in this module, take care of static electricity and insure human earth when handling.
7) Do not open nor modify the Module Assembly.
8) Do not press the reflector sheet at the back of the module to any directions.
9) At the insertion or removal of the Signal Interface Connector, be sure not to rotate nor tilt the Interface Connector of the TFT Module.
11) After installation of the TFT Module into an enclosure (Notebook PC Bezel, for example), do not twist nor bend the TFT Module even momentary. At designing the enclosure, it should be taken into consideration that no bending/twisting forces are applied to the TFT Module from outside. Otherwise the TFT Module may be damaged.
12) Small amount of materials having no flammability grade is used in the LCD module. The LCD module should be supplied by power complied with requirements of Limited Power Source (IEC60950 or UL1950), or be applied exemption.
13) Disconnecting power supply before handling LCD modules, it can prevent electric shock, DO NOT TOUCH the electrode parts, cables, connectors and LED circuit part of TFT module that a LED light bar build in as a light source of back light unit. It can prevent electronic breakdown.

2. General Description

B116XW05 V006 is a Color Active Matrix Liquid Crystal Display composed of a TFT LCD panel. The screen format is intended to support the 16:9 HD, 1366(H) x768(V) screen and 262k colors (RGB 6-bits data driver) without backlight and LED driving circuit. All input signals are eDP interface compatible.

B116XW05 V006 is designed for a display unit of notebook style personal computer and industrial machine.

2.1 General Specification

The following items are characteristics summary on the table at 25 ℃ condition:

Items	Unit	Specifications
Screen Diagonal	[mm]	11.568”
Active Area	[mm]	256.12 x 144.00
Pixels H x V		1366 x 3(RGB) x 768
Pixel Pitch	[mm]	0.1875(V) x 3 x 0.0625(H) mm
Pixel Format		1366 (RGB stripe, H) x 768 (V)
Display Mode		Normally White
Transmittance	%	5.3 % typ. / 5.0 % min.
Response Time	[ms]	16 typ. / 20 Max.
Nominal Input Voltage VDD	[Volt]	+3.3 typ.
Power Consumption	[Watt]	1W max. (Logic)
Weight	[Grams]	100 max.
Electrical Interface		1 channel RVDS
Glass Thickness	[mm]	0.3
Top polarizer		Glossy Surface, 3H Hard Coating, WV
Bottom polarizer		AG, 40% Haze WV
Support Color		262K colors (RGB 6-bit)
Temperature Range Operating Storage (Non-Operating)	 [^{o}C] [^{o}C]	 0 to +50 -20 to +60
RoHS Compliance		RoHS Compliance

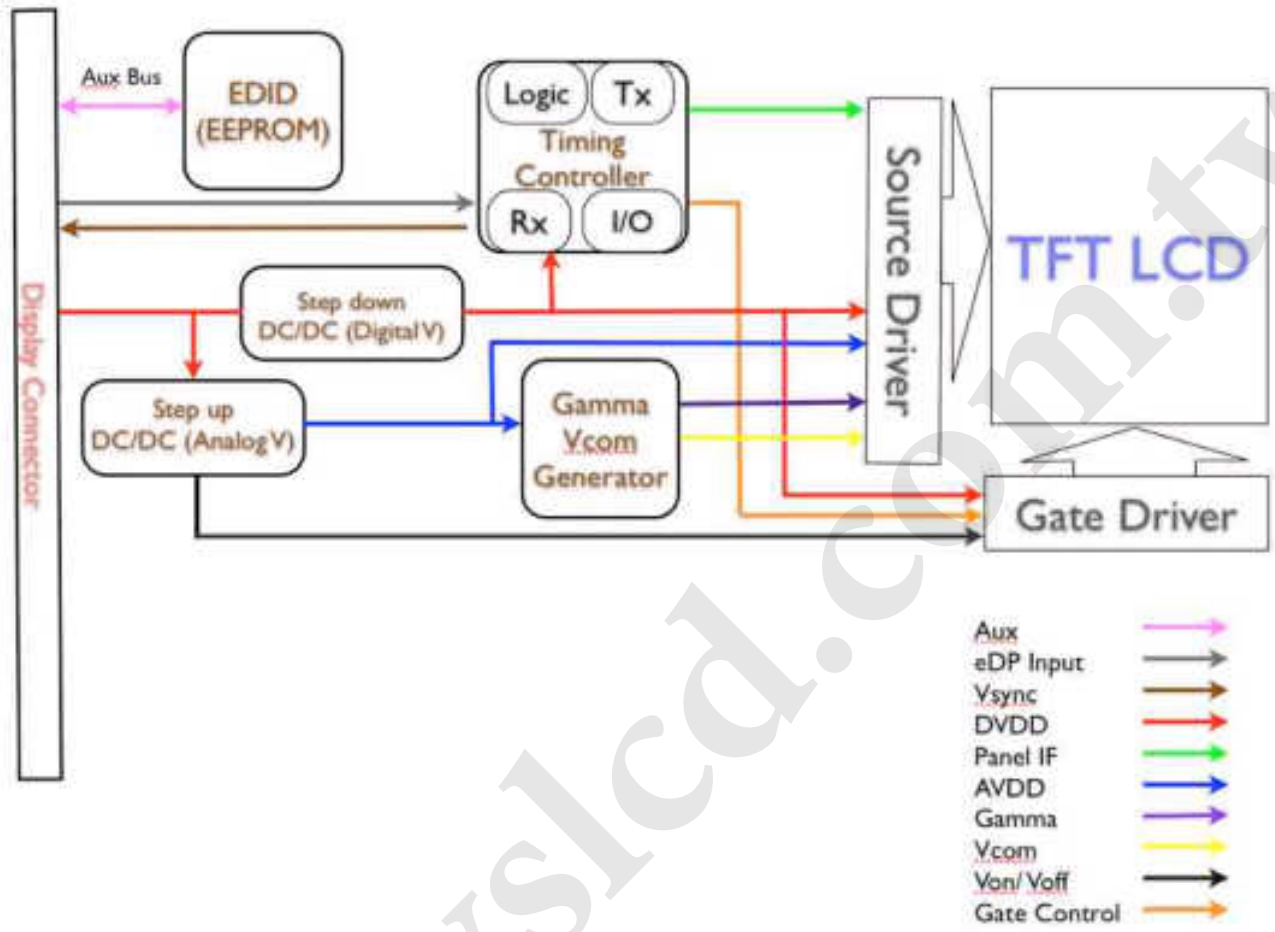
2.2 Optical Characteristics

The optical characteristics are measured under stable conditions at 25℃ (Room Temperature) :

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit	Note
Viewing Angle	θ_R	Horizontal (Right) CR = 10	65	70	-	degree	
	θ_L	(Left)	65	70	-		
	ϕ_H	Vertical (Upper) CR = 10	50	60	-	degree	
	ϕ_L	(Lower)	50	60	-		
Contrast Ratio	CR		500	700	-		
Cross talk	%		-	-	4	%	
Response Time	T_{RT}	Rising + Falling	-	16	20		
NTSC	%	42		45	-		

3. Functional Block Diagram

The following diagram shows the functional block of the 11.6 inches wide Color TFT/LCD 30 Pin one channel Module



4. Absolute Maximum Ratings

An absolute maximum rating of the module is as following:

4.1 Absolute Ratings of TFT LCD Module

Item	Symbol	Min	Max	Unit	Conditions
Logic/LCD Drive Voltage	Vin	-0.3	+4.0	[Volt]	Note 1,2

4.2 Absolute Ratings of Environment

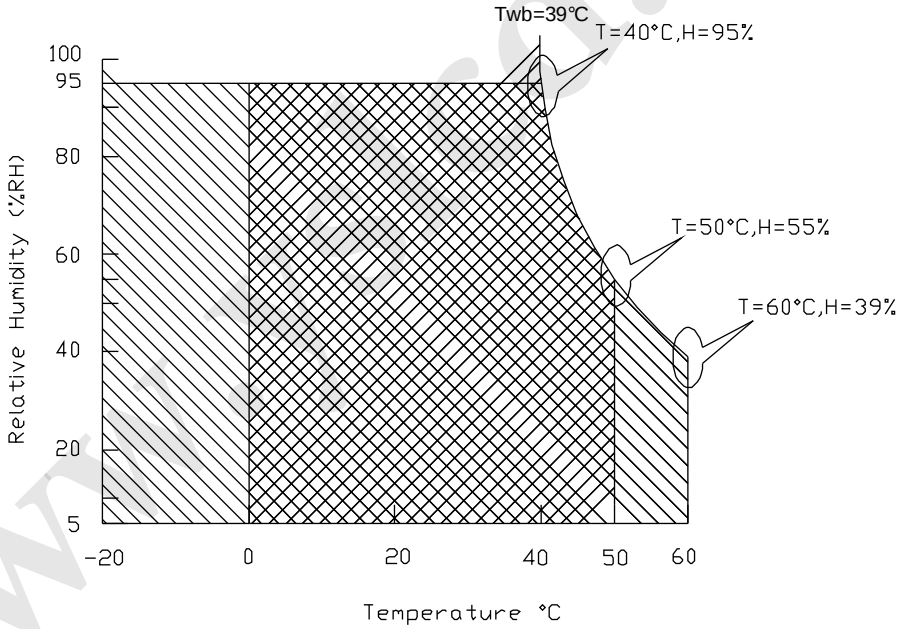
Item	Symbol	Min	Max	Unit	Conditions
Operating Temperature	TOP	0	+50	[°C]	Note 4
Operation Humidity	HOP	5	95	[%RH]	Note 4
Storage Temperature	TST	-20	+60	[°C]	Note 4
Storage Humidity	HST	5	95	[%RH]	Note 4

Note 1: At Ta (25℃)

Note 2: Permanent damage to the device may occur if exceed maximum values

Note 3: LED specification refer to section 5.2

Note 4: For quality performance, please refer to AUO IIS (Incoming Inspection Standard).



Operating Range Storage Range +

5. Electrical Characteristics

5.1 TFT LCD Module

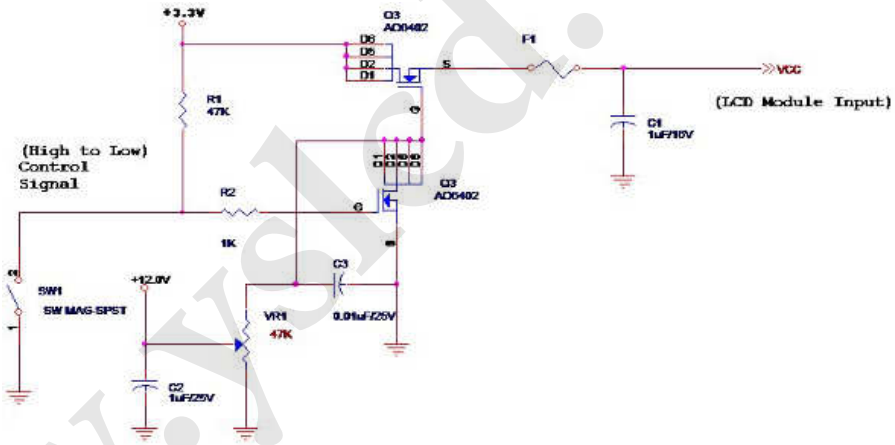
5.1.1 Power Specification

Input power specifications are as follows; The power specification are measured under 25℃ and frame frenquency under 60Hz

Symble	Parameter	Min	Typ	Max	Units	Note
VDD	Logic/LCD Drive Voltage	3.0	3.3	3.6	[Volt]	
PDD	VDD Power	-	-	1	[Watt]	Note 1
IDD	IDD Current	-	-	333	[mA]	Note 1
IRush	Inrush Current	-	-	1500	[mA]	Note 2
VDDrp	Allowable Logic/LCD Drive Ripple Voltage	-	-	330	[mV] p-p	

Note 1 : Maximum Measurement Condition : Black Pattern at 3.3V driving voltage. ($P_{max}=V_{3.3} \times I_{black}$)

Note 2 : Measure Condition

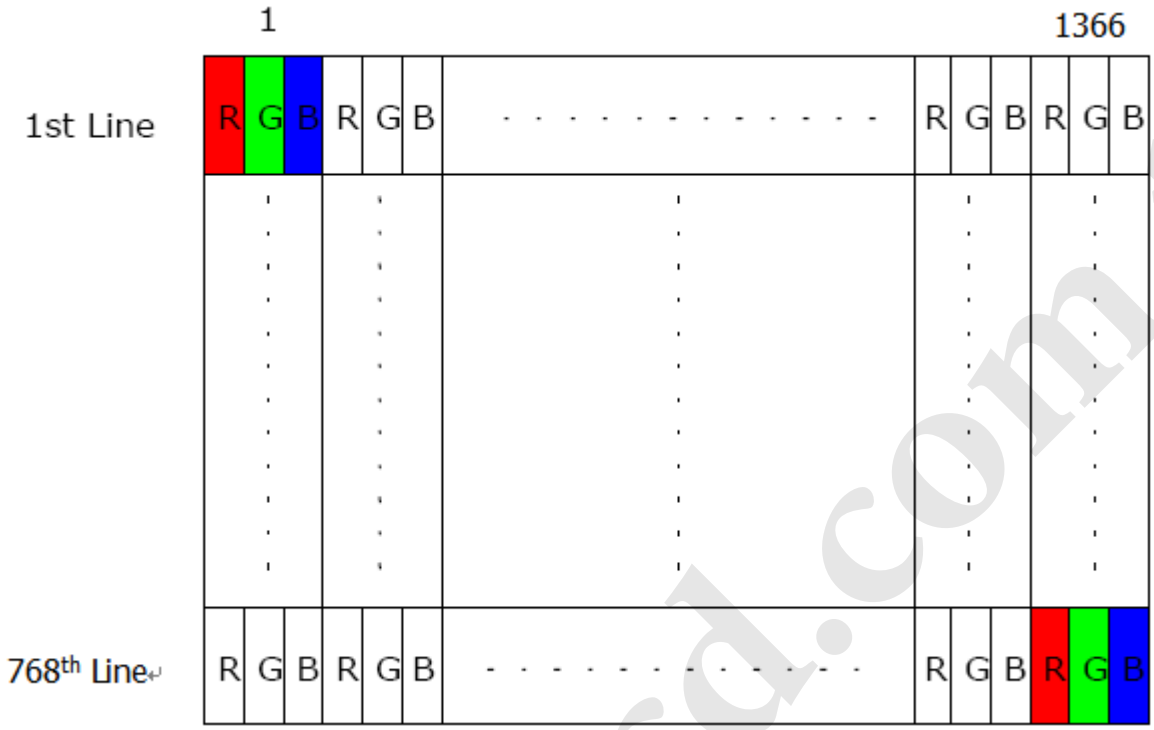


Vin rising time

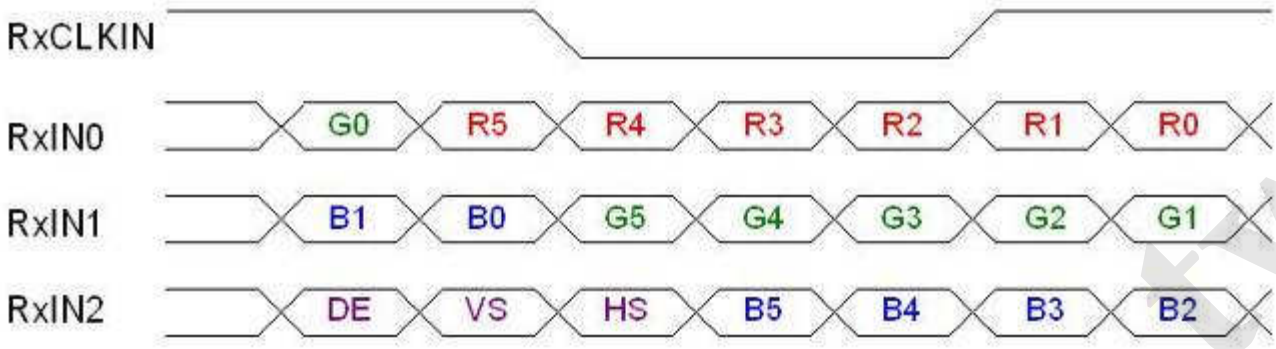
6. Signal Interface Characteristic

6.1 Pixel Format Image

Following figure shows the relationship of the input signals and LCD pixel format.



6.2 The Input Data Format



Signal Name	Description	
R5 R4 R3 R2 R1 R0	Red Data 5 (MSB) Red Data 4 Red Data 3 Red Data 2 Red Data 1 Red Data 0 (LSB) Red-pixel Data	Red-pixel Data Each red pixel's brightness data consists of these 6 bits pixel data.
G5 G4 G3 G2 G1 G0	Green Data 5 (MSB) Green Data 4 Green Data 3 Green Data 2 Green Data 1 Green Data 0 (LSB) Green-pixel Data	Green-pixel Data Each green pixel's brightness data consists of these 6 bits pixel data.
B5 B4 B3 B2 B1 B0	Blue Data 5 (MSB) Blue Data 4 Blue Data 3 Blue Data 2 Blue Data 1 Blue Data 0 (LSB) Blue-pixel Data	Blue-pixel Data Each blue pixel's brightness data consists of these 6 bits pixel data.
RxCLKIN	Data Clock	The signal is used to strobe the pixel data and DE signals. All pixel data shall be valid at the falling edge when the DE signal is high.
DE	Display Timing	This signal is strobed at the falling edge of RxCLKIN. When the signal is high, the pixel data shall be valid to be displayed.
VS	Vertical Sync	The signal is synchronized to RxCLKIN .
HS	Horizontal Sync	The signal is synchronized to RxCLKIN .

Note: Output signals from any system shall be low or High-impedance state when VDD is off.

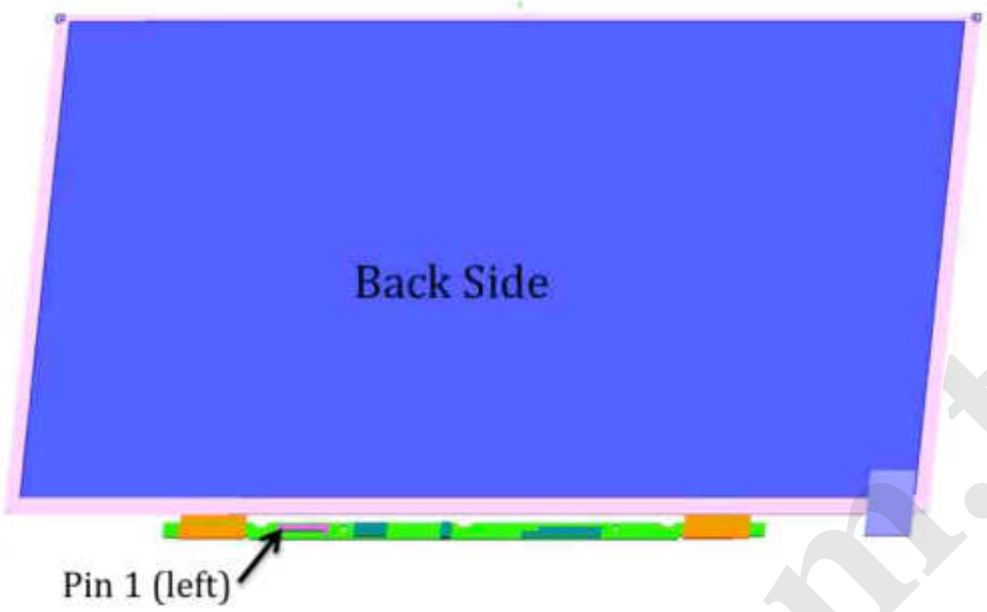
6.3 Integration Interface Requirement

6.3.1 Connector Description

Connector Name / Designation	For Signal Connector
Manufacturer	IPEX or compatible
Type / Part Number	IPEX 20525-030E-02 or compatible
Mating Housing/Part Number	IPEX 20523-030T-01 or compatible

6.3.2 Pin Assignment

Pin	Symbol	Description	Micro-coax cable gauge (AWG)
1	NC-Reserved	NC – Reserved (I2C Data for LCD supplier)	40
2	Vdc(1 to 6)	LED Anode (Positive)	36
3	Vdc(1 to 6)	LED Anode (Positive)	36
4	Vdc(1 to 6)	LED Anode (Positive)	36
5	NC	NC	40
6	Vdc6	LED Cathode (Negative)	40
7	Vdc5	LED Cathode (Negative)	40
8	Vdc4	LED Cathode (Negative)	40
9	Vdc3	LED Cathode (Negative)	40
10	Vdc2	LED Cathode (Negative)	40
11	Vdc1	LED Cathode (Negative)	40
12	Vsync	LED Sync Signal	40
13	FSS	Frame Sync Signal	40
14	HDP	Hot Plug Detect Signal Pin	40
15	LCD_GND	Ground	40
16	LCD_GND	Ground	40
17	LCD_Self_Test	LCD Panel Self Test	40
18	LCD_VCC	LCD logic & driver power	36
19	LCD_VCC	LCD logic & driver power	36
20	H_GND	High Speed Ground	40
21	AUX_CH_N	Complement Signal Aux Ch.	40
22	AUX_CH_P	True Signal Aux Ch.	40
23	H_GND	High Speed Ground	40
24	Lane0_P	True Signal Link 0	40
25	Lane0_N	Complement Signal Link 0	40
26	H_GND	High Speed Ground	40
27	Reserved (Lane1_P)	True Signal Link 1	40
28	Reserved (Lane1_N)	Complement Signal Link 1	40
29	H_GND	High Speed Ground	40
30	NC-Reserved	Reserved (I2C CLK for LCD supplier)	40

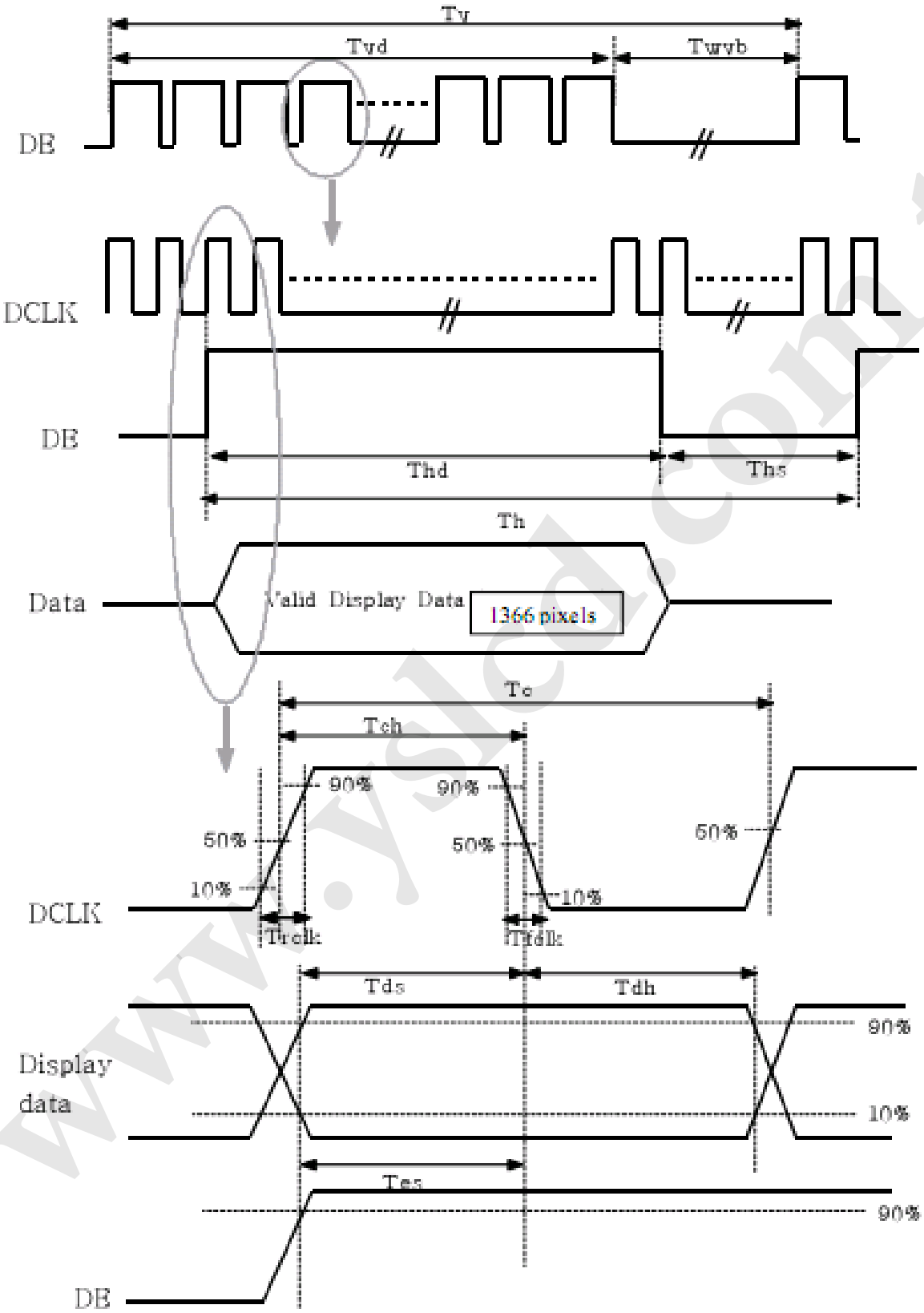


6.4 Interface Timing

6.4.1 Timing Characteristics

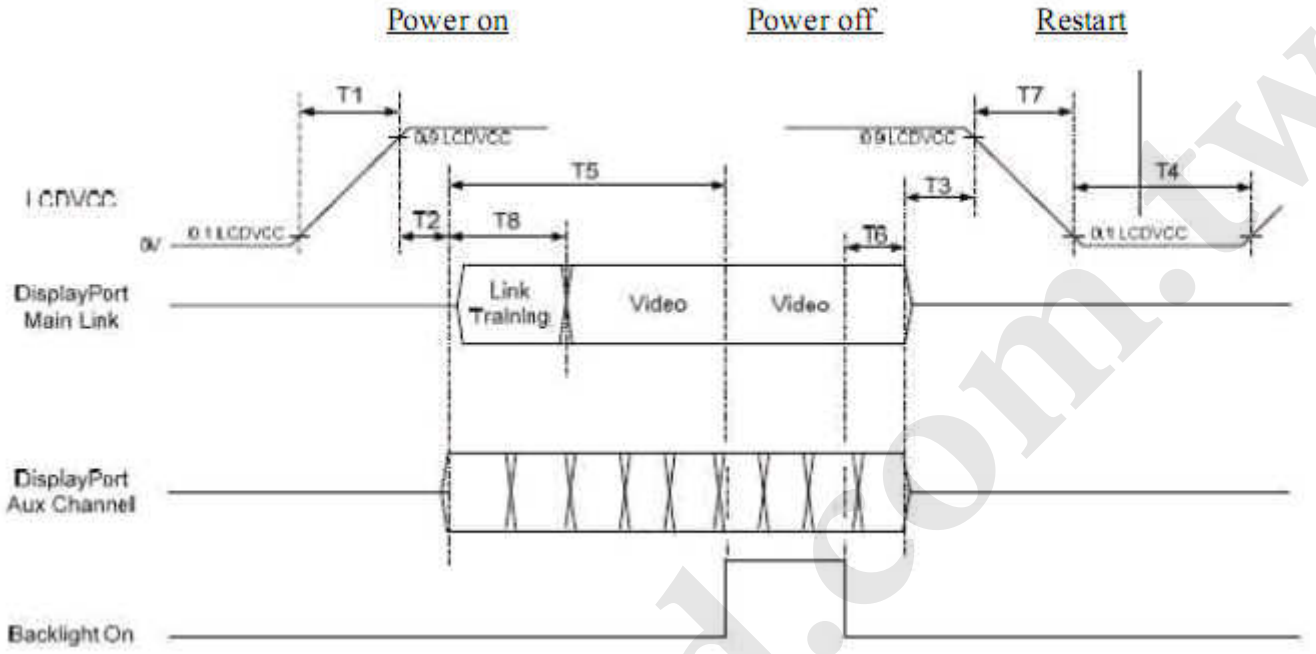
Signal	Parameter	Symbol	Min	Typ	Max	Unit	Note
D_{CLK}	Clock Period	T_C		13.89		ns	1
	Clock Frequency	f_C		72		MHz	$1/T_C$
	Duty Ratio (% High)	K_{dr}	40	50	60	%	T_{Ch}/T_C
	Rise Time	$T_{R\,CLK}$	-	4.42	-	ns	
	Fall Time	$T_{F\,CLK}$	-	4.42	-	ns	
DE	DE Setup Time	T_{se}	4	-	-	ns	
(Data Enable	Data Setup Time	T_{sd}	4	-	-	ns	
Only)	Data Hold Time	T_{hd}	2	-	-	ns	
(DTMG)	Horizontal Period	T_H		1500		T_C	2
Data	Horizontal Blank Period	T_{hb}		134		T_C	
	Vertical Period	T_V		800		T_H	f_V=59.90 Hz, 3
	Vertical Blank Period	T_{vb}		32		T_H	
H_{sync}	H_{sync} Back Porch	H_{bp}	48	64		T_C	
	H_{sync} Pulse Width	T_{wH}	24	54		T_C	
	H_{sync} Front Porch	H_{fp}	8	14		T_C	

6.4.2 Timing diagram



6.5 Power ON/OFF Sequence

Power on/off sequence is as follows. Interface signals and LED on/off sequence are also shown in the chart. Signals from any system shall be Hi-Z state or low level when VDD is off



Parameter	Limit Values		Units	Description
	Min	Max		
T1	0.5	10	ms	Power rail rise time 10% to 90%
T2	0	50	ms	Delay from power on to Sink Aux Channel response ready (note 1)
T3	0	50	ms	Delay from Main Link activity to power off
T4	500	-	ms	Power off time
T5	200	-	ms	Delay from Main Link enable to backlight enable
T6	200	-	ms	Delay from backlight disable to Main Link disable
T7	-	10	ms	Power rail fall time 90% to 10%
T8	-	10	ms	Link training duration, active video enabled by the end of this period

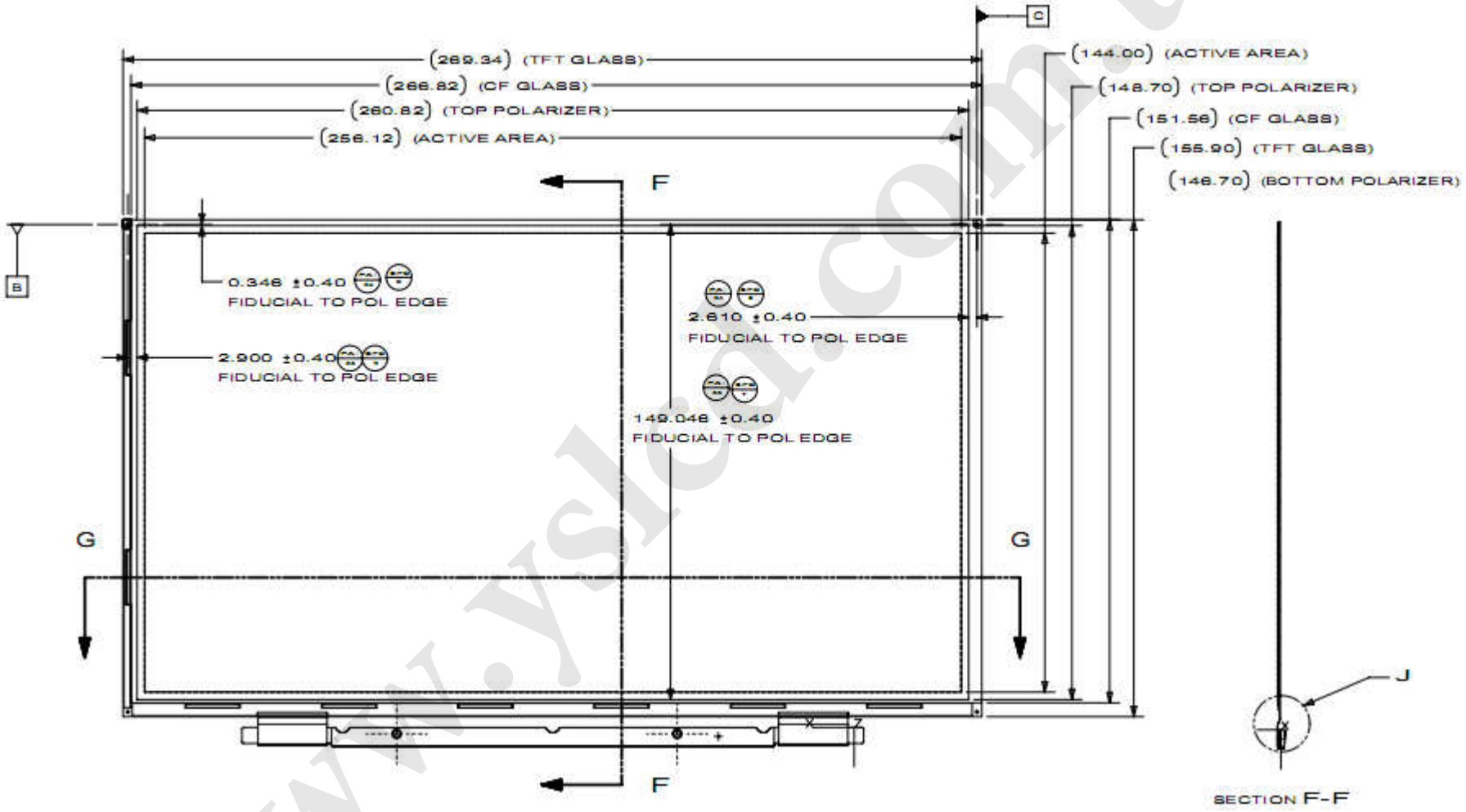
7. Panel Reliability Test

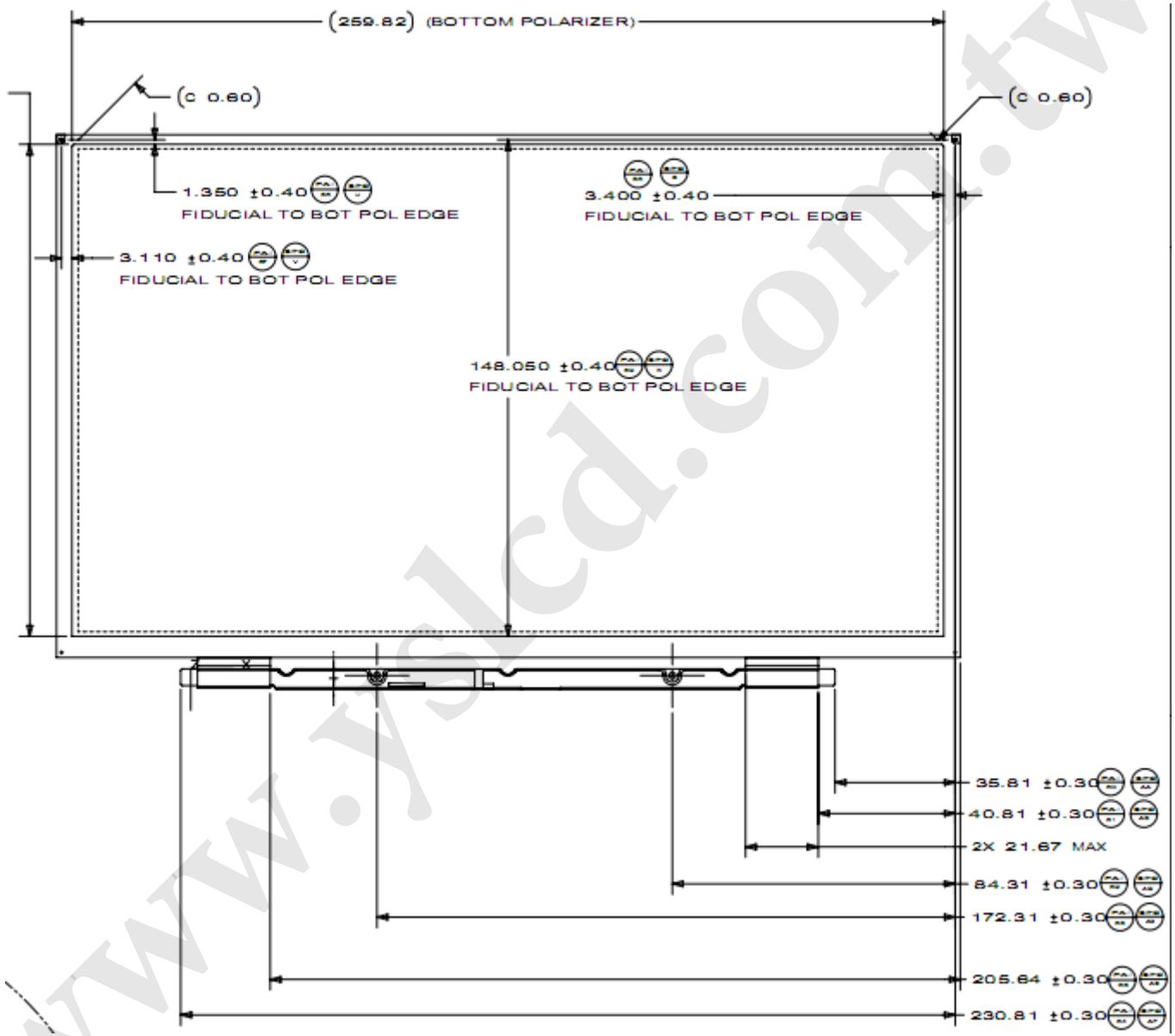
7.1 Reliability Test

Non-operational Testing		
Items	**Required Condition**	**Note**
Low Temperature	-25℃ @ 500h	
High Temperature	65℃ @ 500h	
High Temperature and High Humidity	60℃ @ 500 hrs, R.H. = 75%± 10%	
Thermal Shock Test	Cycle display from -25℃ to 65℃ with 5-minute transfer time, 100 cycles at -25℃/65℃/-25℃	
Operational Testing		
Items	**Required Condition**	**Note**
Low Temperature	0℃ for 500 hours	
High Temperature	50℃ for 500 hours	
Heat Soak	65℃ and 90% R.H. for 72 hours (no obvious FOS degradation or functional failure)	
High Temperature and High Humidity	50℃ and 90% R.H. for 240 hours (Functional Check) Maximum wet-bulb temperature at 39℃ or lower without condensation	

8. Mechanical Characteristics

8.1 LCM Outline Dimension





Note: Prevention IC damage, IC positions not allowed any overlap over these areas.

9. Shipping Label Format

10. Appendix: EDID Description

Address	FUNCTION	B116XW05 V0	Note
HEX	Header	HEX	
00		00	
01		FF	
02		FF	
03		FF	
04		FF	
05		FF	
06		FF	
07		00	
08	EISA Manuf. Code LSB	06	
09	Compressed ASCII	10	
0A	Product Code	10	
0B	hex, LSB first	A0	
0C	32-bit ser #	02	01: Analogix 02: Parade
0D		01	
0E		01	
0F		01	
10	Week of manufacture	19	Week
11	Year of manufacture	15	21(2011-1990=21)
12	EDID Structure Ver.	01	
13	EDID revision #	04	
14	Video input definition	95	Digital Input
15	Max H image size	1A	25.6cm
16	Max V image size	0E	14.4cm
17	Display Gamma	78	Gamma 2.2
18	Feature support	02	no DPMS,Active off,RGB color
19	Red/green low bits	50	
1A	Blue/white low bits	C5	
1B	Red x/ high bits	98	Rx=0.595
1C	Red y	58	Ry=0.345

1D	Green x	52	Gx=0.32
1E	Green y	8E	Gy=0.555
1F	Blue x	27	Bx=0.155
20	Blue y	25	By=0.145
21	White x	50	Wx=0.313
22	White y	54	Wy=0.329
23	Established timing 1	00	unused
24	Established timing 2	00	
25	Manufacturer's Timing	00	
26	Standard timing #1	01	unused
27		01	
28	Standard timing #2	01	
29		01	
2A	Standard timing #3	01	
2B		01	
2C	Standard timing #4	01	
2D		01	
2E	Standard timing #5	01	
2F		01	
30	Standard timing #6	01	
31		01	
32	Standard timing #7	01	
33		01	
34	Standard timing #8	01	
35		01	
36	Pixel Clock/10,000 (LSB)	20	Timing Descriptor #1
37	Pixel Clock/10,000 (MSB)	1C	1366x768 @60_mode:pixel clock=72MHz
38	Horiz. Active pixels(Lower 8 bits)	56	Horiz active=1366 pixels
39	Horiz.Blanking (Lower 8 bits)	86	Horiz blanking=768 pixels
3A	Horiz. Active pixels:Horiz. Blanking (Upper4:4 bits)	50	
3B		00	
3C		20	
3D	Vert. Active pixels:Vert. Blanking (Upper4:4 bits)	30	
3E		0E	Horiz sync. Offset=56 pixels
3F		38	Horiz sync. Pulse Width=56 pixels
40	Vert. Sync. Offset=xx lines, Sync Width=xx lines	13	Verti sync. Offset=1 lines,Sync Width=3 lines

41	Horz. Ver. Sync/Width (upper 2 bits)	00	
42	Hori. Image size (Lower 8 bits)	00	Hori image size= 256.125 mm
43	Vert. Image size (Lower 8 bits)	90	Verti image size = 144mm
44	Hori. Image size : Vert. Image size (Upper 4 bits)	10	
45		00	Horizontal Border = 0
46		00	Vertical Border = 0
47		18	
48	Detailed timing/monitor	00	ASCII Data String:B133EW01 V0
49	descriptor #2	00	
4A		00	
4B		10	For apple
4C	Version	00	For apple
4D	Apple edid signature	00	For apple
4E	Apple edid signature	00	For apple
4F	Link Type (LVDS Link,MSB justified)	00	For apple
50	Pixel and link component format (6-bit panel interface)	00	For apple
51	Panel features (No inverter)	00	For apple
52		00	
53		00	
54		00	
55		00	
56		00	
57		00	
58		00	
59		00	
5A	Detailed timing/monitor	00	ASCII Data String:B154SW02 V0
5B	descriptor #3	00	
5C		00	
5D		FE	
5E		00	
5F		42	B
60		31	1
61		31	1
62		36	6
63		58	X
64		57	W
65		30	0
66		35	5
67		20	
68		56	V
69		36	5

6A		0A	
6B		20	
6C	Detailed timing/monitor	00	Monitor Name: Color LCD
6D	descriptor #4	00	
6E		00	
6F		FC	
70		00	
71		43	C
72		6F	o
73		6C	l
74		6F	o
75		72	r
76		20	
77		4C	L
78		43	C
79		44	D
7A		0A	
7B		20	
7C		20	
7D		20	
7E	Extension Flag	00	
7F	Checksum	F9	