

ADD-A-PAK Generation VII

Power Modules Schottky Rectifier, 100 A




ADD-A-PAK



RoHS
COMPLIANT

FEATURES

- 175 °C T_J operation
- Low forward voltage drop
- High frequency operation
- Low thermal resistance
- UL approved file E78996 
- Designed and qualified for industrial level
- Material categorization: For definitions of compliance please see www.vishay.com/doc?99912

BENEFITS

- Excellent thermal performances obtained by the usage of exposed direct bonded copper substrate
- High surge capability
- Easy mounting on heatsink

ELECTRICAL DESCRIPTION

The VS-VSKDS209.. Schottky rectifier doubler module has been optimized for low reverse leakage at high temperature. The proprietary barrier technology allows for reliable operation up to 175 °C junction temperature. Typical applications are in high current switching power supplies, plating power supplies, UPS systems, converters, freewheeling diodes, welding, and reverse battery protection.

PRODUCT SUMMARY

$I_{F(AV)}$	100 A
V_R	150 V
Package	ADD-A-PAK
Circuit	Two diodes common cathodes

MECHANICAL DESCRIPTION

The ADD-A-PAK generation VII, new generation of ADD-A-PAK module, combines the excellent thermal performances obtained by the usage of exposed direct bonded copper substrate, with advanced compact simple package solution and simplified internal structure with minimized number of interfaces.

MAJOR RATINGS AND CHARACTERISTICS

SYMBOL	CHARACTERISTICS	VALUES	UNITS
$I_{F(AV)}$	Rectangular waveform	100	A
V_{RRM}		150	V
I_{FSM}	$t_p = 5 \mu s$ sine	11 300	A
V_F	100 A _{pk} , $T_J = 125$ °C	0.85	V
T_J	Range	- 55 to 175	°C

VOLTAGE RATINGS

PARAMETER	SYMBOL	VS-VSKDS209/150	UNITS
Maximum DC reverse voltage	V_R	150	V
Maximum working peak reverse voltage	V_{RWM}		

**ABSOLUTE MAXIMUM RATINGS**

PARAMETER	SYMBOL	TEST CONDITIONS	VALUES	UNITS
Maximum average forward current per leg	$I_{F(AV)}$	50 % duty cycle at $T_C = 113\text{ }^{\circ}\text{C}$, rectangular waveform	100	A
Maximum peak one cycle non-repetitive surge current	I_{FSM}	5 μs sine or 3 μs rect. pulse	11 300	
		10 ms sine or 6 ms rect. pulse	1600	
Non-repetitive avalanche energy	E_{AS}	$T_J = 25\text{ }^{\circ}\text{C}$, $I_{AS} = 1.8\text{ A}$, $L = 10\text{ mH}$	15	mJ
Repetitive avalanche current	I_{AR}	Current decaying linearly to zero in 1 μs Frequency limited by T_J maximum $V_A = 1.5 \times V_R$ typical	1	A

ELECTRICAL SPECIFICATIONS

PARAMETER	SYMBOL	TEST CONDITIONS	VALUES	UNITS
Maximum forward voltage drop	V_{FM}	100 A	1.01	V
		200 A	1.35	
		100 A	0.85	
		200 A	1.13	
Maximum reverse leakage current	I_{RM}	$T_J = 25\text{ }^{\circ}\text{C}$	6	mA
		$T_J = 125\text{ }^{\circ}\text{C}$	85	
Maximum junction capacitance	C_T	$V_R = 5\text{ V}_{DC}$ (test signal range 100 kHz to 1 MHz), $25\text{ }^{\circ}\text{C}$	3000	pF
Typical series inductance	L_S	Measured lead to lead 5 mm from package body	7.0	nH
Maximum voltage rate of change	dV/dt	Rated V_R	10 000	V/ μs
Maximum RMS insulation voltage	V_{INS}	50 Hz	3000 (1 min) 3600 (1 s)	V

THERMAL - MECHANICAL SPECIFICATIONS

PARAMETER	SYMBOL	TEST CONDITIONS	VALUES	UNITS
Maximum junction and storage temperature range	T _J , T _{Stg}		- 55 to 175	°C
Maximum thermal resistance, junction to case per leg	R _{thJC}	DC operation	0.52	°C/W
Typical thermal resistance, case to heatsink per module	R _{thCS}		0.1	
Approximate weight			75	g
			2.7	oz.
Mounting torque ± 10 %	to heatsink	A mounting compound is recommended and the torque should be rechecked after a period of 3 hours to allow for the spread of the compound.	4	Nm
	busbar		3	
Case style		JEDEC®	TO-240AA compatible	

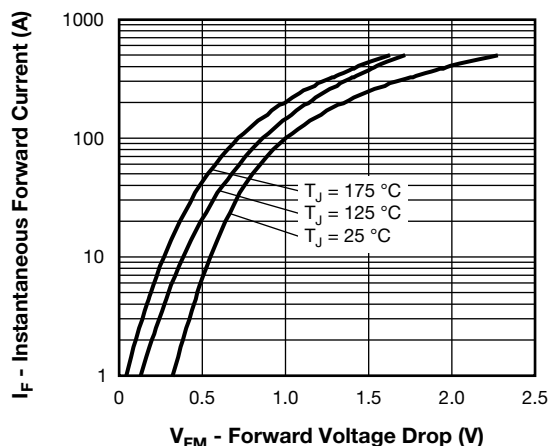


Fig. 1 - Maximum Forward Voltage Drop Characteristics

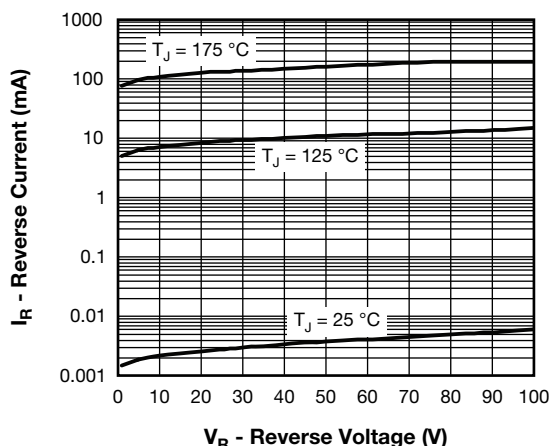


Fig. 2 - Typical Values of Reverse Current vs. Reverse Voltage

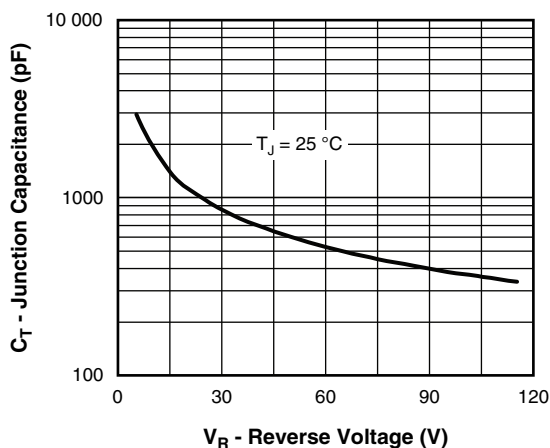
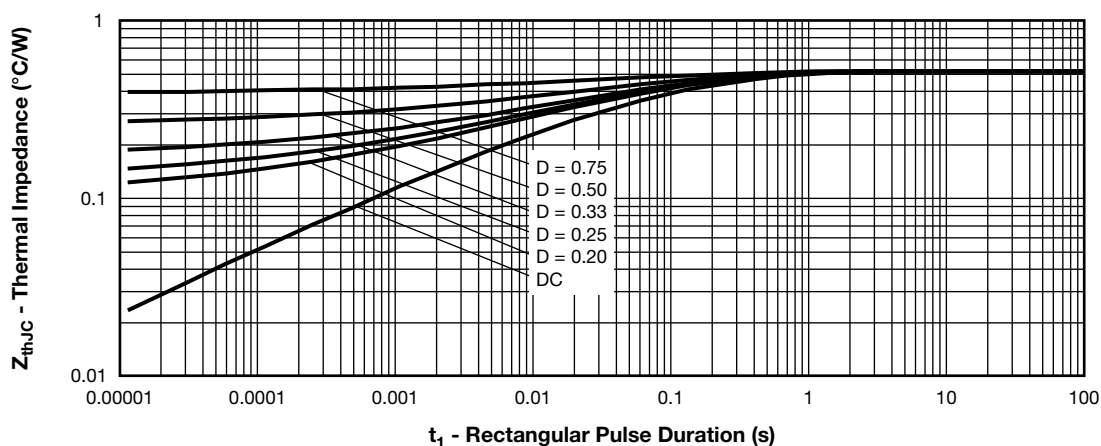


Fig. 3 - Typical Junction Capacitance vs. Reverse Voltage


Fig. 4 - Maximum Thermal Impedance Z_{thJC} Characteristics

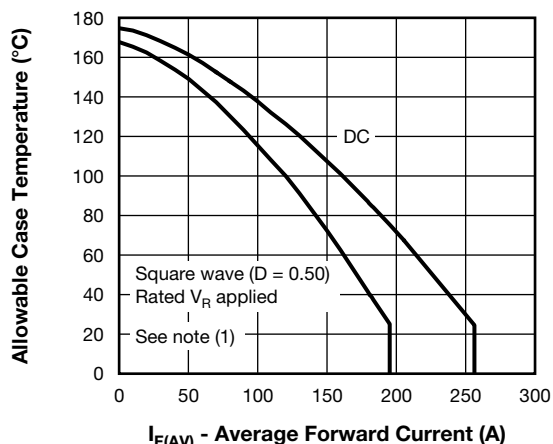


Fig. 5 - Maximum Allowable Case Temperature vs. Average Forward Current

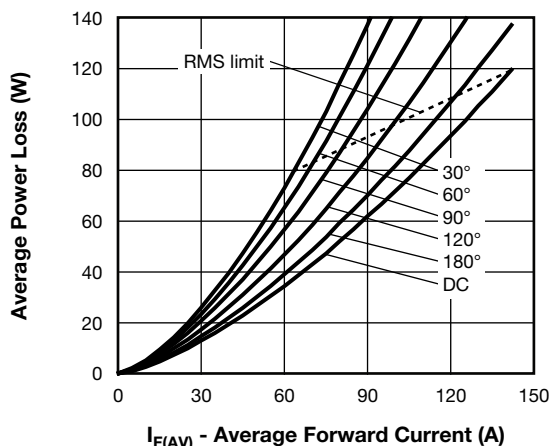


Fig. 6 - Forward Power Loss Characteristics

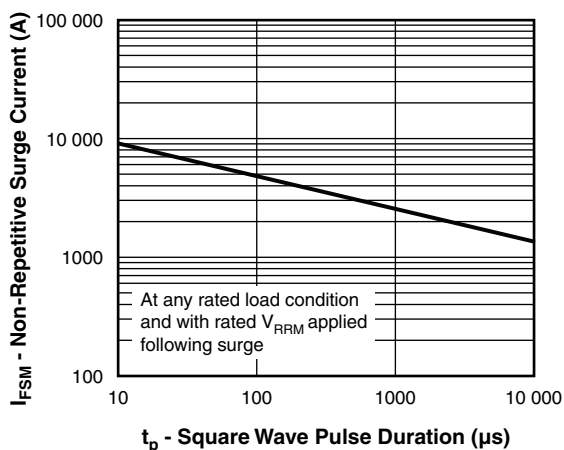


Fig. 7 - Maximum Non-Repetitive Surge Current

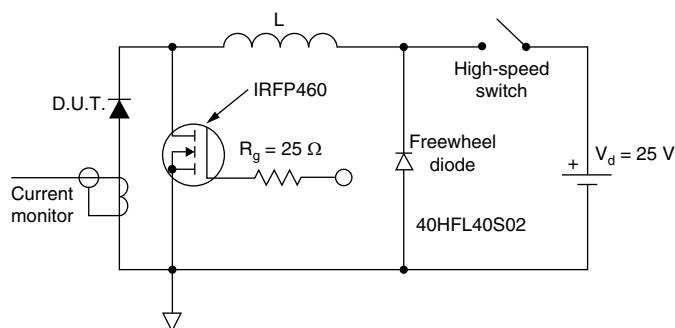


Fig. 8 - Unclamped Inductive Test Circuit

Note

- (1) Formula used: $T_C = T_J - (P_d + P_{dREV}) \times R_{thJC}$;
 P_d = Forward power loss = $I_{F(AV)} \times V_{FM}$ at $(I_{F(AV)}/D)$ (see fig. 6);
 P_{dREV} = Inverse power loss = $V_{R1} \times I_R (1 - D)$; I_R at $V_{R1} = 80\%$ rated V_R

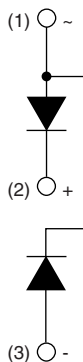


ORDERING INFORMATION TABLE

Device code	VS-VS	KD	S	20	9	/	150
	1	2	3	4	5		6

- 1 - VS-VS = Vishay Semiconductors product
- 2 - Circuit configuration:
KD = ADD-A-PAK - 2 diodes in series
- 3 - S = Schottky diode
- 4 - Average current rating (20 = 200 A)
- 5 - Product silicon identification
- 6 - Voltage rating (150 = 150 V)

CIRCUIT CONFIGURATION



LINKS TO RELATED DOCUMENTS	
Dimensions	www.vishay.com/doc?95369



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