TFT LCD Preliminary Specification

MODEL NO.: N121X5 -L05

Customer : _____

Approved by : _____

Note :

Liquid Crystal Display Division	
QRA Division	OA Head Division
Approval	Approval
陳 94.3.11 永一	林 94.3.11 添仁

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REVISION HISTORY

Version	Date	Page (New)	Section	Description
Ver 1.0	Feb. 04. '05	All	All	Preliminary specification first issued.
Ver1.1	Mar. 11. '05	8	3.1	Modify Power the value of per EBL WG
		9	3.1	Delete item (d) of Note (4)
		9	3.2	Modify the value of Max. Lamp Current, Max. Power Consumption, Min Lamp Life Time
		10	3.2	Modify Note (5): I_L = 5.0mA_{RMS}
		17	5.5	Modify EDID DATA STRUCTURE
		25	7.4.2	Modify the value of No.7,8
		27	7.4.2	Modify Brightness control
		28	8.2	Modify Color Gamut (typ.):45%

1. GENERAL DESCRIPTION

1.1 OVERVIEW

N121X5 -L05 is a 12.1" TFT Liquid Crystal Display module with single CCFL Backlight unit and 20 pins LVDS interface. This module supports 1024 x 768 XGA mode and can display 262,144 colors. The optimum viewing angle is at 6 o'clock direction. The inverter module for Backlight is built in.

1.2 FEATURES

- Thin and light weight
- XGA (1024 x 768 pixels) resolution
- DE (Data Enable) only mode
- 3.3V LVDS (Low Voltage Differential Signaling) interface with 1 pixel/clock
- Support EDID Structure Version 1 Revision 3

1.3 APPLICATION

- TFT LCD Notebook

1.4 GENERAL SPECIFICATI0NS

Item	Specification	Unit	Note
Active Area	245.76 (H) X 184.32 (V)	mm	(1)
Bezel Opening Area	250.5 (H) x 188.9 (V)	mm	
Driver Element	a-si TFT active matrix	-	-
Pixel Number	1024 x R.G.B. x 768	pixel	-
Pixel Pitch	0.24 (H) x 0.24 (V)	mm	-
Pixel Arrangement	RGB vertical stripe	-	-
Display Colors	262,144	color	-
Transmissive Mode	Normally white	-	-
Surface Treatment	Hard coating (3H), Anti-glare (Haze 25 %)	-	-

1.5 MECHANICAL SPECIFICATIONS

Item		Min.	Typ.	Max.	Unit	Note
Module Size	Horizontal(H)	260.5	261	261.5	mm	(1)
	Vertical(V)	197.5	198	198.5	mm	
	Depth(D)	--	4.7	5.0 (Panel Module) 5.2 (Inverter, follow Dell Spec.)	mm	
Weight		--	260	275	g	(2)
		--	270	285	g	(3)

Note (1) Please refer to the attached drawings for more information of front and back outline dimensions.

Note (2) Weight without inverter.

Note (3) Weight with inverter

2. ABSOLUTE MAXIMUM RATINGS

2.1 ABSOLUTE RATINGS OF ENVIRONMENT

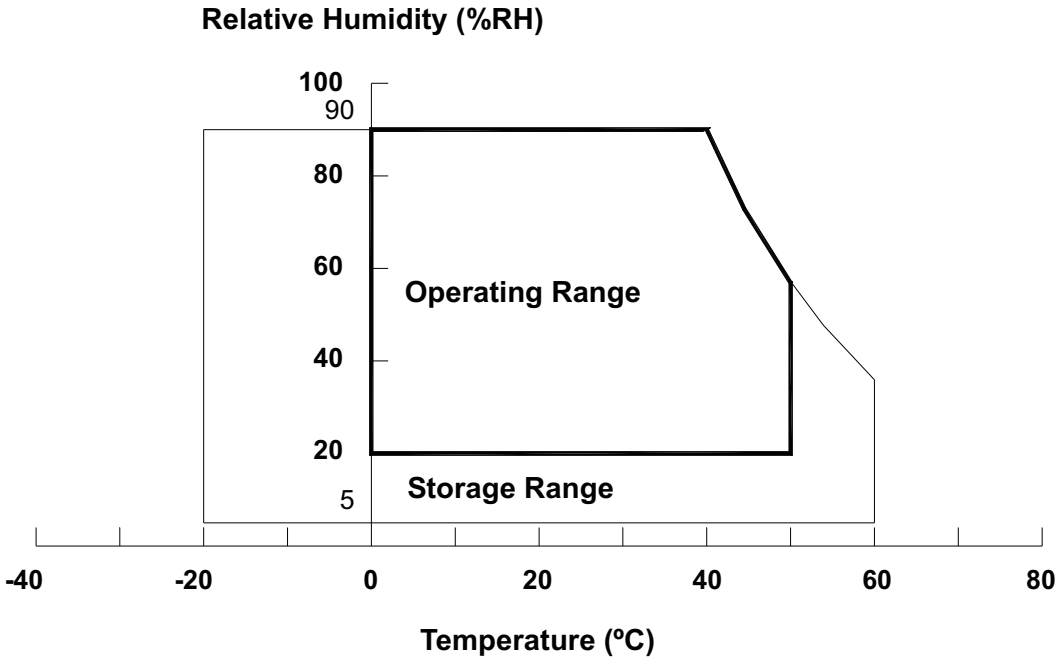
Item	Symbol	Value		Unit	Note
		Min.	Max.		
Storage Temperature	T_{ST}	-20	+60	ºC	(1)
Operating Ambient Temperature	T_{OP}	0	+50	ºC	(1), (2)
Shock (Non-Operating)	S_{NOP}	-	220	G	(3), (5)
Vibration (Non-Operating)	V_{NOP}	-	1.5	G	(4), (5)

Note (1) Temperature and relative humidity range is shown in the figure below.

(a) 90 %RH Max. (Ta ≦ 40 ºC).

(b) Wet-bulb temperature should be 39 ºC Max. (Ta > 40 ºC).

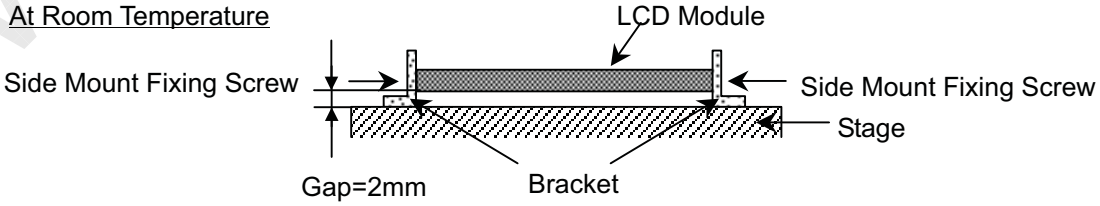
(c) No condensation .



Note (2) The temperature of panel surface should be 0 ºC Min. and 50 ºC Max.

Note (3) 2ms, half sine wave, 1 time for ± X, ± Y, ± Z.

Note (4) 10 ~ 200 Hz, 0.5 Hr / Cycle, 1 cycles for each X, Y, Z. The fixing condition is shown as below:



Note (5) At testing Vibration and Shock, the fixture in holding the module has to be hard and rigid enough so that the module would not be twisted or bent by the fixture.

2.2 ELECTRICAL ABSOLUTE RATINGS

2.2.1 TFT LCD MODULE

Item	Symbol	Value		Unit	Note
		Min.	Max.		
Power Supply Voltage	Vcc	-0.3	+4.0	V	(1)
Logic Input Voltage	V_{IN}	-0.3	Vcc+0.3	V	

2.2.2 BACKLIGHT UNIT

Item	Symbol	Value		Unit	Note
		Min.	Max.		
Lamp Voltage	V_L	-	2.5K	V_{RMS}	(1), (2), I_L = (6.0) mA
Lamp Current	I_L	-	6.5	mA_{RMS}	(1), (2)
Lamp Frequency	F_L	-	80	KHz	

Note (1) Permanent damage to the device may occur if maximum values are exceeded. Function operation should be restricted to the conditions described under Normal Operating Conditions.

Note (2) Specified values are for lamp (Refer to Section 3.2 for further information).

3. ELECTRICAL CHARACTERISTICS

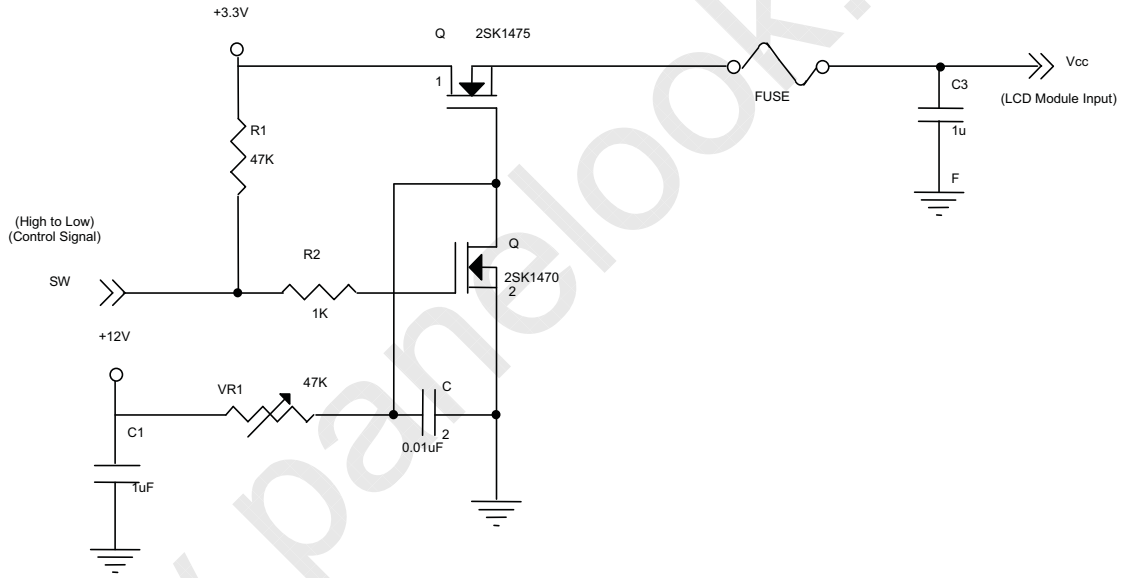
3.1 TFT LCD MODULE

Ta = 25 ± 2 ºC

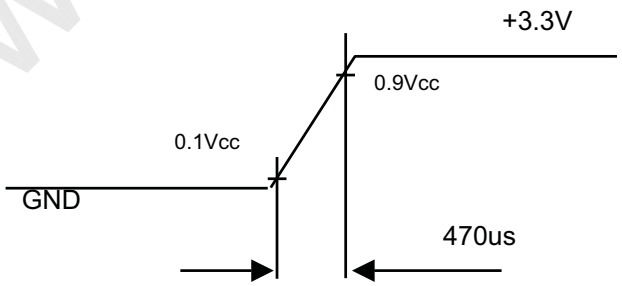
Parameter		Symbol	Value			Unit	Note
			Min.	Typ.	Max.		
Power Supply Voltage		Vcc	3.0	3.3	3.6	V	-
Ripple Voltage		V_{RP}	-	-	100	mV	-
Rush Current		I_{RUSH}	-	-	1.5	A	(2)
Power Supply Current	White	Icc	-	(300)		mA	(3)a
	Black		-	(350)		mA	(3)b
Differential Input Voltage for LVDS Receiver Threshold	"H" Level	V_{IH}	-	-	+100	mV	-
	"L" Level	V_{IL}	-100	-	-	mV	-
Terminating Resistor		R_T	-	100	-	Ohm	-
Power per EBL WG		P_{EBL}	-	(2.71)	-	W	(4)

Note (1) The module should be always operated within above ranges.

Note (2) Measurement Conditions:



Vcc rising time is 470us



Note (3) The specified power supply current is under the conditions at Vcc = 3.3 V, Ta = 25 ± 2 ºC, DC Current and f_v = 60 Hz, whereas a power dissipation check pattern below is displayed.

a. White Pattern

Active Area

b. Black Pattern

Active Area

Note (4) The specified power are the sum of LCD panel electronics input power and the inverter input power. Test conditions are as follows.

(a) Vcc = 3.3 V, Ta = 25 ± 2 ºC, f_v = 60 Hz,

(b) The pattern used is a black and white 32 x 36 checkerboard, slide #100 from the VESA file "Flat Panel Display Monitor Setup Patterns", FPDMSU.ppt.

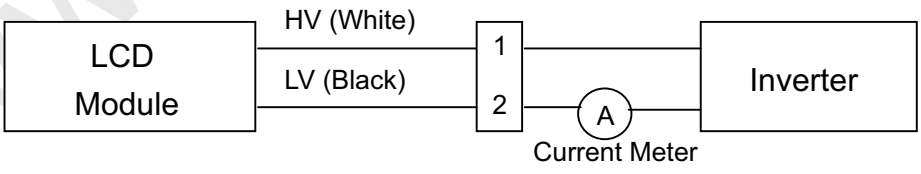
(c) Luminance: 60 nits.

3.2 BACKLIGHT UNIT

Ta = 25 ± 2 ºC

Parameter	Symbol	Value			Unit	Note
		Min.	Typ.	Max.		
Lamp Input Voltage	V_L	(540)	(600)	(660)	V_{RMS}	I_L = 5.0 mA
Lamp Current	I_L	(3.0)	5.0	5.5	mA_{RMS}	(1),(7)
Lamp Turn On Voltage	V_S	-	-	(1170) (25 °C)	V_{RMS}	(2)
		-	-	(1340) (0 °C)	V_{RMS}	(2)
Operating Frequency	F_L	(45)	-	(80)	KHz	(3)
Power Consumption	P_L	-	(3.0)	(3.3)	W	(4), I_L = 5.0 mA
Lamp Life Time	L_{BL}	15,000	-	-	Hrs	(5)

Note (1) Lamp current is measured by utilizing a high frequency current meter as shown below:



Note (2) The voltage shown above should be applied to the lamp for more than 1 second after startup. Otherwise the lamp may not be turned on.

Note (3) The lamp frequency may generate interference with horizontal synchronous frequency from the display, and this may cause line flow on the display. In order to avoid interference, the lamp

frequency should be detached from the horizontal synchronous frequency and its harmonics as far as possible.

Note (4) $P_L = I_L \times V_L$

Note (5) The lifetime of lamp is defined as the time when it continues to operate under the conditions at Ta = 25 ±2 °C and I_L = 5.0mA_{RMS} until one of the following events occurs:

(a) When the brightness becomes ≦ 50% of its original value.

(b) When the effective ignition length becomes ≦ 80% of its original value. (Effective ignition length is defined as an area that the brightness is less than 70% compared to the center point.)

Note (6) The waveform of the voltage output of inverter must be area-symmetric and the design of the inverter must have specifications for the modularized lamp. The performance of the Backlight, such as lifetime or brightness, is greatly influenced by the characteristics of the DC-AC inverter for the lamp. All the parameters of an inverter should be carefully designed to avoid generating too much current leakage from high voltage output of the inverter. When designing or ordering the inverter please make sure that a poor lighting caused by the mismatch of the Backlight and the inverter (miss-lighting, flicker, etc.) never occurs. If the above situation is confirmed, the module should be operated in the same manners when it is installed in your instrument.

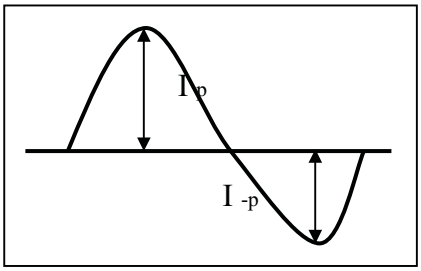
The output of the inverter must have symmetrical (negative and positive) voltage waveform and symmetrical current waveform.(Unsymmetrical ratio is less than 10%) Please do not use the inverter, which has unsymmetrical voltage and unsymmetrical current and spike wave. Lamp frequency may produce interface with horizontal synchronous frequency and as a result this may cause beat on the display. Therefore lamp frequency shall be as away possible from the horizontal synchronous frequency and from its harmonics in order to prevent interference.

Requirements for a system inverter design, which is intended to have a better display performance, a better power efficiency and a more reliable lamp. It shall help increase the lamp lifetime and reduce its leakage current.

a. The asymmetry rate of the inverter waveform should be 10% below;

b. The distortion rate of the waveform should be within $\sqrt{2}$ ± 10%;

c. The ideal sine wave form shall be symmetric in positive and negative polarities.



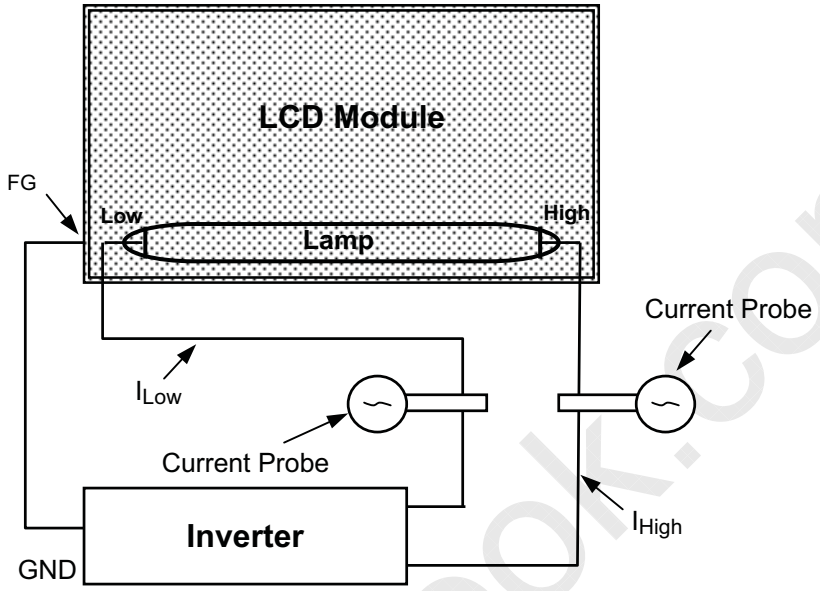
* Asymmetry rate:

$| I_p - I_{-p} | / I_{rms} * 100\%$

* Distortion rate

I_p (or I_{-p}) / I_{rms}

Note (7) The lamp leakage current is measured by the current difference between in and out. And the measurement condition is as below:



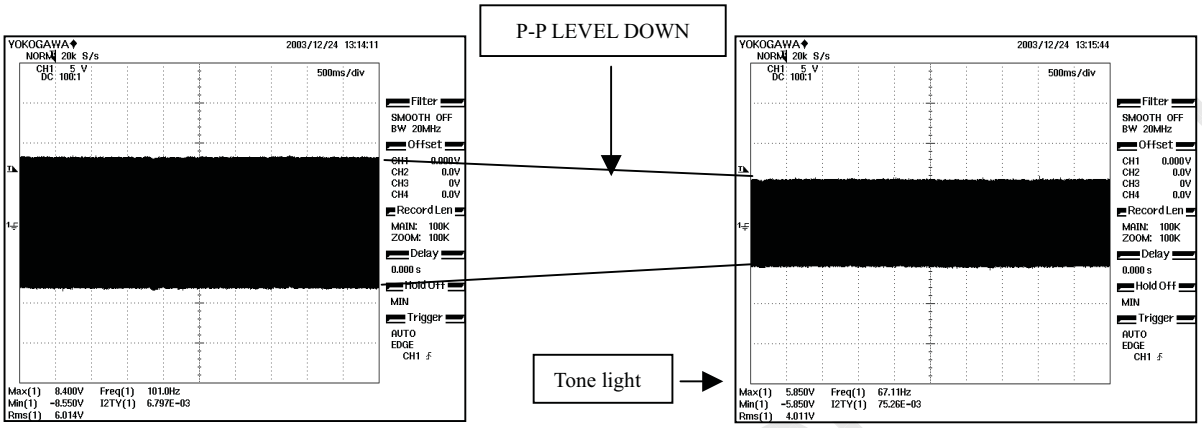
$$I_{Leak(RMS)} = I_{High(RMS)} - I_{Low(RMS)}$$

Note (8) About operating current min 2.0mA , lamp maker has some advice as below

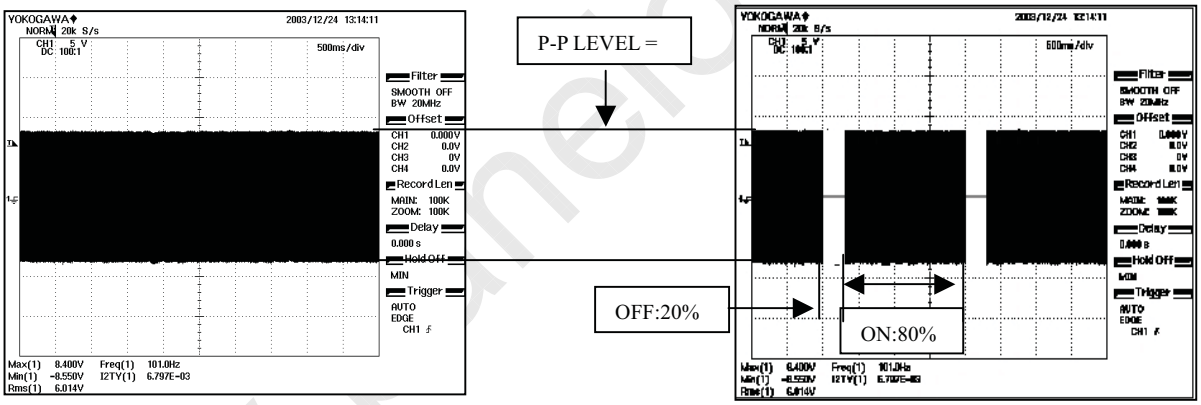
(Reference) Light quantity adjustment method

Explanation and comparison of the kind of tone light:

① Lamp current wave-like by the adjustment of the current.



② Lamp current wave-like by the adjustment of the burst.



Comparative table

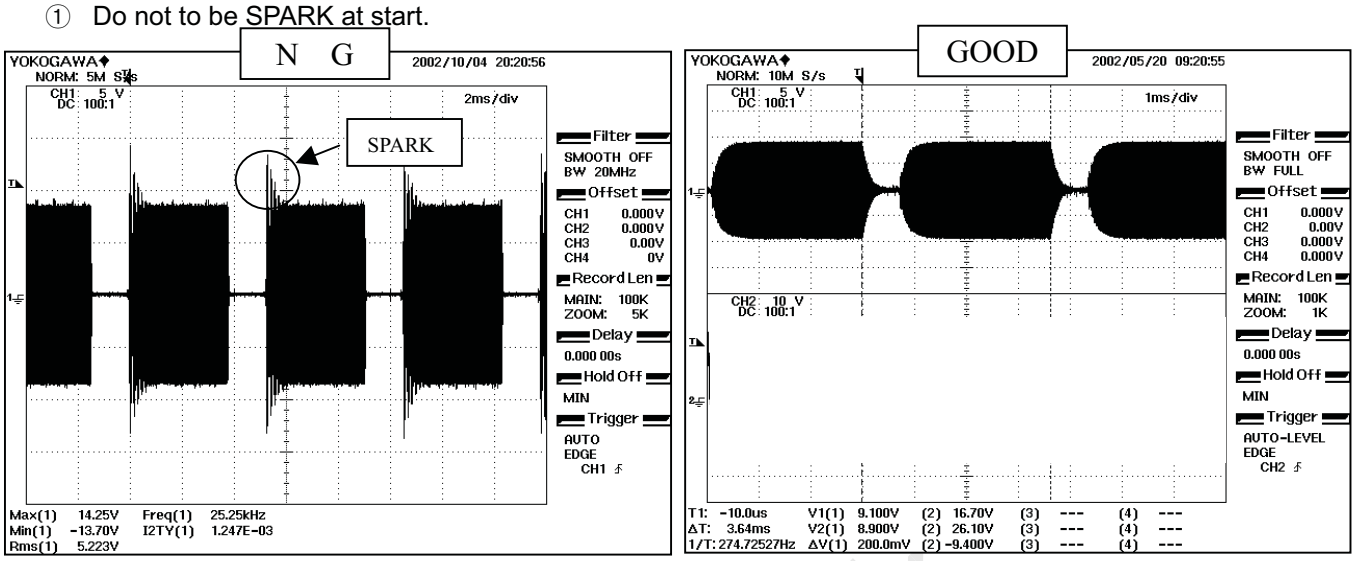
Method	Backlight efficiency (INV+LAMP)	Tone light rate (%)	Circuitry
①current	Good (75 % ~ 85%)	58	Complicated
②burst	Bad (65 % ~ 75%)	10	Easy

Method of case that Lamp current MIN2.0mA is controlled.

It is the setting of minimum 2.0mA (MIN) to Lamp current 6.0mA in the lamp specification. The burst is excellent for circuitry. The marker proposes that pays attention to the following contents.

The attention point of the light with a touch of the burst:

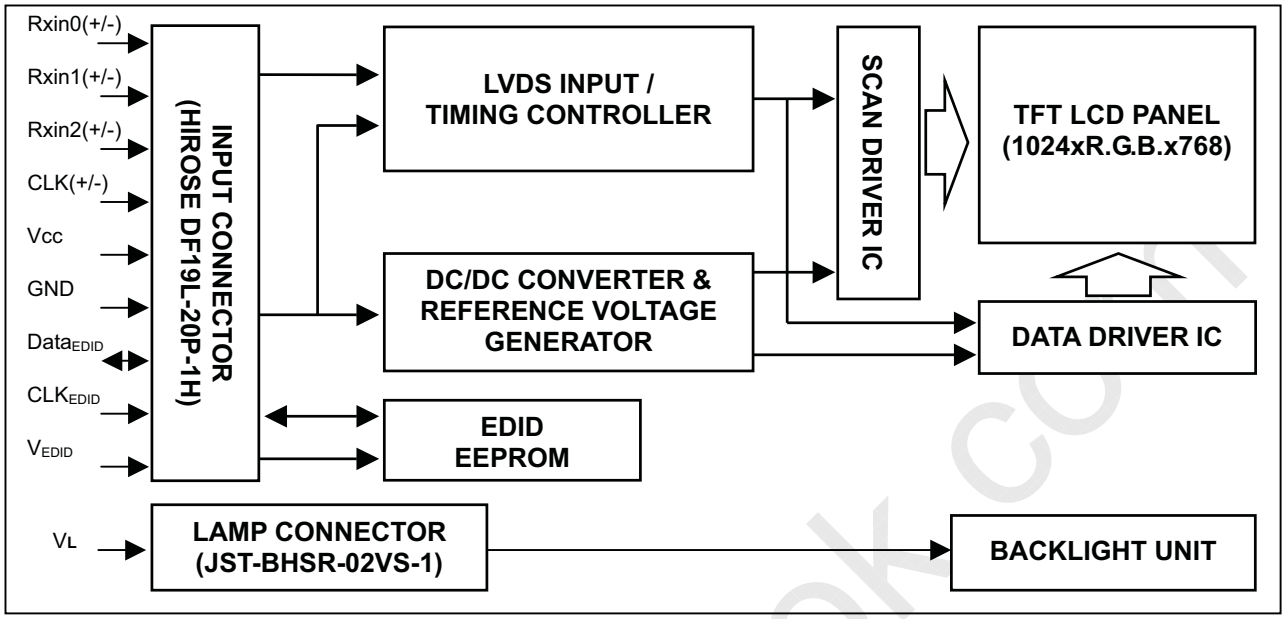
① Do not to be SPARK at start.



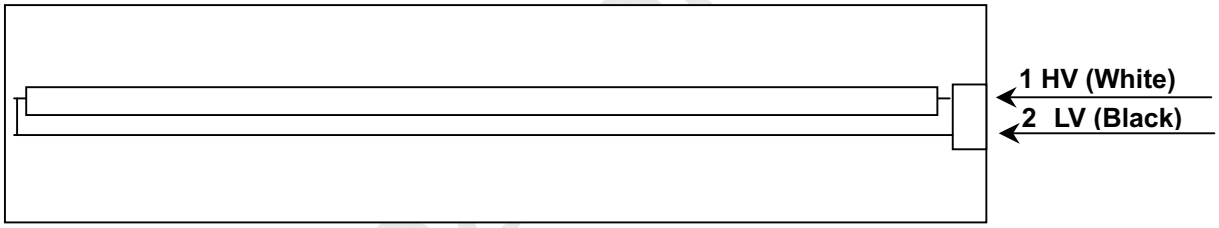
② PWM frequency does so that the frequency that is not able to divide the fixed number time, fixed number to lamp drive frequency is selected. (It is due to resonance noise occurrence prevention.) Even the frequency that is using it for LCD avoids selecting it.

4. BLOCK DIAGRAM

4.1 TFT LCD MODULE



4.2 BACKLIGHT UNIT



5. INPUT TERMINAL PIN ASSIGNMENT

5.1 TFT LCD MODULE

Pin	Symbol	Description	Polarity	Remark
1	Vss	Ground		
2	Vcc	Power Supply +3.3 V (typical)		
3	Vcc	Power Supply +3.3 V (typical)		
4	V_{EDID}	DDC 3.3V Power		
5	BIST	Panel BIST enable pin		
6	CLK_{EDID}	DDC Clock		
7	$DATA_{EDID}$	DDC Data		
8	Rxin0-	LVDS Differential Data Input	Negative	R0~R5,G0
9	Rxin0+	LVDS Differential Data Input	Positive	-
10	Vss	Ground		
11	Rxin1-	LVDS Differential Data Input	Negative	G1~G5,B0,B1
12	Rxin1+	LVDS Differential Data Input	Positive	-
13	Vss	Ground		
14	Rxin2-	LVDS Differential Data Input	Negative	B2~B5,DE,Hsync,Vsync
15	Rxin2+	LVDS Differential Data Input	Positive	
16	Vss	Ground		
17	CLK-	LVDS Clock Data Input	Negative	LVDS Level Clock
18	CLK+	LVDS Clock Data Input	Positive	
19	Vss	Ground		
20	Vss	Ground		

Note (1) The first pixel is even.

Note (2) Connector Part No.: HIROSE DF19L-20P-1H or equivalent

Note (3) User's connector Part No: HIROSE DF19G-20S-1C or equivalent

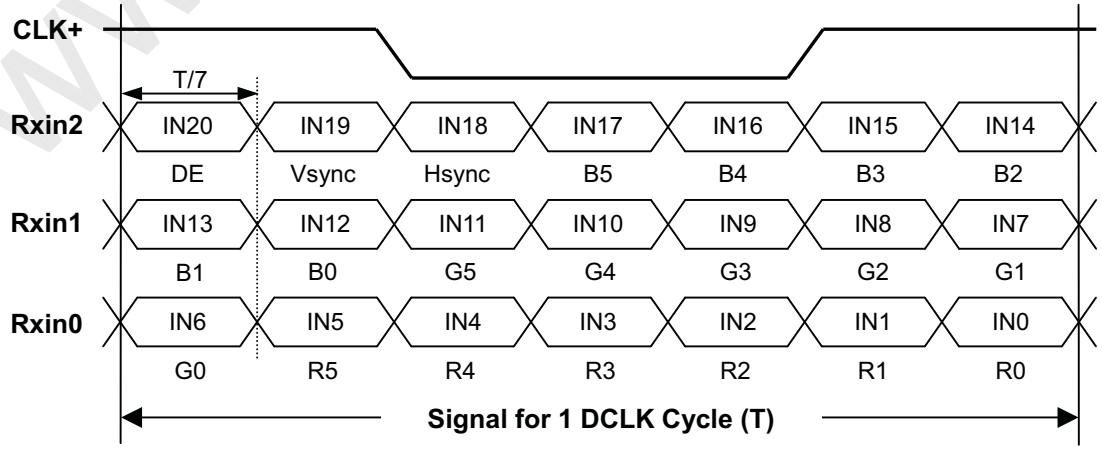
5.2 BACKLIGHT UNIT

Pin	Symbol	Description	Color
1	HV	High Voltage	White
2	LV	Ground	Black

Note (1) Connector Part No.: JST-BHSR-02VS-1 or equivalent

Note (2) User's connector Part No.: JST-SM02B-BHSS-1-TB or equivalent

5.3 TIMING DIAGRAM OF LVDS INPUT SIGNAL



5.4 COLOR DATA INPUT ASSIGNMENT

The brightness of each primary color (red, green and blue) is based on the 6-bit gray scale data input for the color. The higher the binary input the brighter the color. The table below provides the assignment of color versus data input.

Color		Data Signal																	
		Red						Green						Blue					
		R5	R4	R3	R2	R1	R0	G5	G4	G3	G2	G1	G0	B5	B4	B3	B2	B1	B0
Basic Colors	Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0
	Green	0	0	0	0	0	0	1	1	1	1	1	1	0	0	0	0	0	0
	Blue	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1
	Cyan	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1
	Magenta	1	1	1	1	1	1	0	0	0	0	0	0	1	1	1	1	1	1
	Yellow	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0
	White	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Gray Scale Of Red	Red(0)/Dark	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red(1)	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0
	Red(2)	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
	Red(61)	1	1	1	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0
	Red(62)	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red(63)	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0
Gray Scale Of Green	Green(0)/Dark	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Green(1)	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0
	Green(2)	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0
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	Green(61)	0	0	0	0	0	0	1	1	1	1	0	1	0	0	0	0	0	0
	Green(62)	0	0	0	0	0	0	1	1	1	1	1	0	0	0	0	0	0	0
	Green(63)	0	0	0	0	0	0	1	1	1	1	1	1	0	0	0	0	0	0
Gray Scale Of Blue	Blue(0)/Dark	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Blue(1)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
	Blue(2)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0
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	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
	Blue(61)	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	0	1
	Blue(62)	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	0
	Blue(63)	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1

Note (1) 0: Low Level Voltage, 1: High Level Voltage

5.5 EDID DATA STRUCTURE

The EDID (Extended Display Identification Data) data formats are to support displays as defined in the VESA Plug & Display and FPDI standards.

Byte # (decimal)	Byte # (hex)	Field Name and Comments	Value (hex)	Value (binary)
0	0	Header	00	00000000
1	1	Header	FF	11111111
2	2	Header	FF	11111111
3	3	Header	FF	11111111
4	4	Header	FF	11111111
5	5	Header	FF	11111111
6	6	Header	FF	11111111
7	7	Header	00	00000000
8	8	EISA ID manufacturer name (“CMO”)	0D	00001101
9	9	EISA ID manufacturer name (Compressed ASCII)	AF	10101111
10	0A	ID product code (N121X5)	04	00000100
11	0B	ID product code (hex LSB first; N121X5)	12	00010010
12	0C	ID S/N (fixed “0”)	00	00000000
13	0D	ID S/N (fixed “0”)	00	00000000
14	0E	ID S/N (fixed “0”)	00	00000000
15	0F	ID S/N (fixed “0”)	00	00000000
16	10	Week of manufacture (fixed “50”)	32	00110010
17	11	Year of manufacture (fixed “2004”)	0E	00001110
18	12	EDID structure version # (“1”)	01	00000001
19	13	EDID revision # (“3”)	03	00000011
20	14	Video I/P definition (“digital”)	80	10000000
21	15	Max H image size (“24.576 cm”)	19	00011001
22	16	Max V image size (“18.432 cm”)	12	00010010
23	17	Display Gamma (Gamma = ” 2.2”)	78	01111000
24	18	Feature support (“RGB, preferred timing”)	0A	00001010
25	19	Red/Green (Rx1, Rx0, Ry1, Ry0, Gx1, Gx0, Gy1, Gy0)	FE	11111110
26	1A	Blue/White (Bx1, Bx0, By1, By0, Wx1, Wx0, Wy1, Wy0)	60	01100000
27	1B	Red-x (Rx = “0.585”)	95	10010101
28	1C	Red-y (Ry = “0.335”)	55	01010101
29	1D	Green-x (Gx = “0.32”)	51	01010001
30	1E	Green-y (Gy = “0.53”)	87	10000111
31	1F	Blue-x (Bx = “0.15”)	26	00100110
32	20	Blue-y (By = “0.135”)	22	00100010
33	21	White-x (Wx = “0.313”)	50	01010000
34	22	White-y (Wy = “0.329”)	54	01010100
35	23	Established timings 1	00	00000000
36	24	Established timings 2 (1024x768@60Hz)	08	00001000
37	25	Manufacturer’s reserved timings	00	00000000
38	26	Standard timing ID # 1	01	00000001
39	27	Standard timing ID # 1	01	00000001
40	28	Standard timing ID # 2	01	00000001
41	29	Standard timing ID # 2	01	00000001

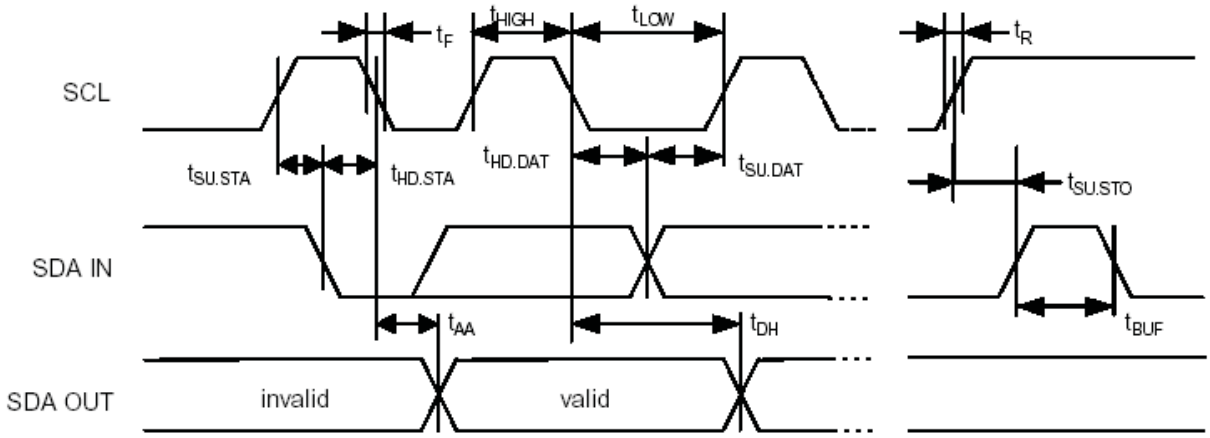
42	2A	Standard timing ID # 3	01	00000001
43	2B	Standard timing ID # 3	01	00000001
44	2C	Standard timing ID # 4	01	00000001
45	2D	Standard timing ID # 4	01	00000001
46	2E	Standard timing ID # 5	01	00000001
47	2F	Standard timing ID # 5	01	00000001
48	30	Standard timing ID # 6	01	00000001
49	31	Standard timing ID # 6	01	00000001
50	32	Standard timing ID # 7	01	00000001
51	33	Standard timing ID # 7	01	00000001
52	34	Standard timing ID # 8	01	00000001
53	35	Standard timing ID # 8	01	00000001
54	36	Detailed timing description # 1 Pixel clock (“65 MHz”)	64	01100100
55	37	# 1 Pixel clock (hex LSB first)	19	00011001
56	38	# 1 H active (“1024”)	00	00000000
57	39	# 1 H blank (“320”)	40	01000000
58	3A	# 1 H active: H blank (“1024 : 320”)	41	01000001
59	3B	# 1 V active (” 768”)	00	00000000
60	3C	# 1 V blank (” 38”)	26	00100110
61	3D	# 1 V active: V blank (” 768 : 38”)	30	00110000
62	3E	# 1 H sync offset (” 24”)	18	00011000
63	3F	# 1 H sync pulse width (” 136”)	88	10001000
64	40	# 1 V sync offset: V sync pulse width (” 3 : 6”)	36	00110110
65	41	# 1 H sync offset: H sync pulse width : V sync offset : V sync width (” 24 : 136 : 3 : 6”)	00	00000000
66	42	# 1 H image size (” 245.76 mm”)	F6	11110110
67	43	# 1 V image size (” 184.32 mm”)	B8	10111000
68	44	# 1 H image size: V image size (” 245 : 184”)	00	00000000
69	45	# 1 H boarder (” 0”)	00	00000000
70	46	# 1 V boarder (” 0”)	00	00000000
71	47	# 1 Flags (” Non-Interlace, Non-Stereo, Digital Separate”)	18	00011000
72	48	Detailed timing description # 2 Pixel clock (“52 MHz”, According to VESA CVT Rev. 1.1)	50	01010000
73	49	# 2 Pixel clock (hex LSB first)	14	00010100
74	4A	# 2 H active (“1024”)	00	00000000
75	4B	# 2 H blank (“288”)	20	00100000
76	4C	# 2 H active : H blank (“1024 : 288”)	41	01000001
77	4D	# 2 V active (“768”)	00	00000000
78	4E	# 2 V blank (“25”)	19	00011001
79	4F	# 2 V active : V blank (“768 : 25”)	30	00110000
80	50	# 2 H sync offset (“40”)	28	00101000
81	51	# 2 H sync pulse width (“104”)	68	01101000
82	52	# 2 V sync offset : V sync pulse width (“3 : 4”)	34	00110100
83	53	# 2 H sync offset : H sync pulse width : V sync width : V sync pulse width (“24 : 136 : 3 : 4”)	00	00000000
84	54	# 2 H image size (“245.76 mm”)	F6	11110110
85	55	# 2 V image size (“184.32 mm”)	B8	10111000
86	56	# 2 H image size : V image size (“245 : 184”)	00	00000000

87	57	# 2 H boarder (“0”)	00	00000000
88	58	# 2 V boarder (“0”)	00	00000000
89	59	Module “A” Revision= Example : 00, 01, 02, 03, etc.	00	00000000
90	5A	Detailed timing description # 3	00	00000000
91	5B	# 3 Flag	00	00000000
92	5C	# 3 Reserved	00	00000000
93	5D	# 3 FE (hex) defines ASCII string (Model Name “N121X5”, ASCII)	FE	11111110
94	5E	# 3 Flag	00	00000000
95	5F	# 3 1st character of string (“N”)	4E	01001110
96	60	# 3 2nd character of string (“1”)	31	00110001
97	61	# 3 3rd character of string (“2”)	32	00110010
98	62	# 3 4th character of string (“1”)	31	00110001
99	63	# 3 5th character of string (“X”)	58	01011000
100	64	# 3 6th character of string (“5”)	35	00110101
101	65	# 3 New line character # 3 indicates end of ASCII string	20	00100000
102	66	# 3 Padding with “Blank” character	20	00100000
103	67	# 3 Padding with “Blank” character	20	00100000
104	68	# 3 Padding with “Blank” character	20	00100000
105	69	# 3 Padding with “Blank” character	20	00100000
106	6A	# 3 Padding with “Blank” character	20	00100000
107	6B	# 3 Padding with “Blank” character	20	00100000
108	6C	Detailed timing description # 4	00	00000000
109	6D	# 4 Flag	00	00000000
110	6E	# 4 Reserved	00	00000000
111	6F	# 4 Data Type Tag:	FE	11111110
112	70	# 4 Flag	00	00000000
113	71	SMBUS value= (10) nits	(E5)	11100101
114	72	SMBUS value= (17) nits	(D1)	11010001
115	73	SMBUS value= (24) nits	(C3)	11000011
116	74	SMBUS value= (30) nits	(BA)	10111010
117	75	SMBUS value= (60) nits	(91)	10010001
118	76	SMBUS value= (90) nits	(6C)	01101100
119	77	SMBUS value= (120) nits	(44)	01000100
120	78	SMBUS value= (MAX) nits	(00)	00000000
121	79	Numbers of LVDS Receiver chip= 0	00	00000000
122	7A	Numbers of LVDS Receiver chip = 0 (“Yes”)	00	00000000
123	7B	(If < 13 char, then terminate with ASCII code 0Ah, set remaining char = 20h)	0A	00001010
124	7C	(If < 13 char, then terminate with ASCII code 0Ah, set remaining char = 20h)	20	00100000
125	7D	(If < 13 char, then terminate with ASCII code 0Ah, set remaining char = 20h)	20	00100000
126	7E	Extension flag	00	00000000
127	7F	Checksum	25	00100101

5.6 EDID SIGINAL SPECIFICATION

(1) EDID Power

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Power supply voltage	Vcc	Read Operation	2.2	—	5.5	V



(2) DC characteristics

		Symbol	Min.	Max.	Unit	Index
SCL, SDA terminal input voltage	High Voltage	VIH	0.7 Vcc	—	V	
	Low Voltage	VIL	—	0.3 Vcc	V	
Hysteresis Voltage		VHYS	0.05 VCC	—	V	
Output Voltage		VOL1 VOL2	—	0.4 0.6	V	IOL=3mA, CC=2.5V IOL=6mA, CC=2.5V
Input Leak current (Vin =0.1V~VCC)		ILI	-10 -10	10 50	uA	WP=VSS WP=VCC
Output Leak current		ILO	-10	10	uA	Vout =0.1V~VCC, WP=VSS
Terminal capacity(Input, Output)		Cin, Cout	—	10	pF	VCC=5.0V Ta=25^{0}C, Fclk=1.0MHz
Operating current		ICC Write ICC Read	—	3 1	mA	VCC=5.5V, SCL=400KHz
Stillness current (SDA=SCL=VCC) (WP=VSS,A0,A1,A2=VSS)		ICCS	—	30 100	uA	VCC=3.0V VCC=5.5V

(3) AC characteristics (VCC=2.5~5.5V standard operation mode)

Item	Symbol	VCC=2.5V-5.5V (Standard operation mode)		VCC=4.5V-5.5V (High-speed operation mode)			
		Min.	Max.	Min.	Max.	Unit	Index
Clock frequency	Fclk	—	100	—	400	KHz	
Clock High Time	THIGH	4000	—	900	—	ns	
Clock Low Time	TLOW	4700	—	1300	—	ns	
SDA, SCL falling time	TR	—	1000	—	300	ns	
SDA, SCL rising time	TF	—	300	—	300	ns	
START hold time	THD: STA	4000	—	600	—	ns	
START setup time	TSU: STA	4700	—	600	—	ns	
Data input hold time	THD: Data	0	—	0	—	ns	
Data input setup time	TSU: Data	250	—	100	—	ns	
STOP setup time	TSU: STO	4700	—	600	—	ns	
Output decision time from a clock	TAA	—	3500	100	900	ns	
Bus free time	TBUF	4700	—	1300	—	ns	
Rising time of Min VIH, VIL	TOF	—	250	20	250	ns	CB≦100pF
Spike oppression	TSP	—	50	—	50	ns	
A write-in cycle time	TWR	—	10	—	10	ms	Byte and page mode
The number of times of data rewriting	—	1M	—	1M	—	cycles	VCC=5.0V Ta=25^{0}C,

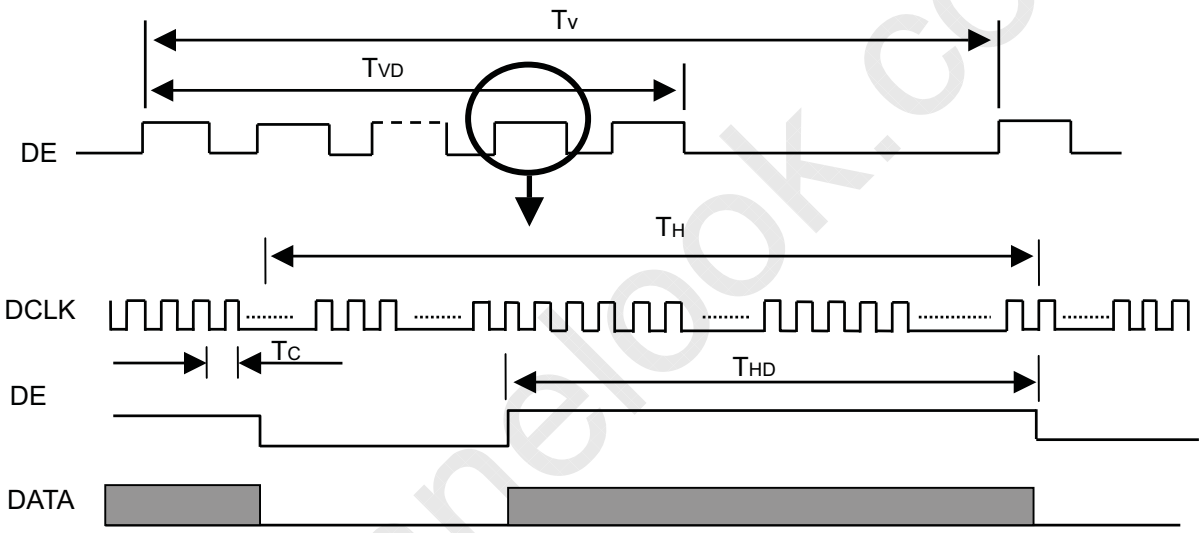
6. INTERFACE TIMING

6.1 INPUT SIGNAL TIMING SPECIFICATIONS

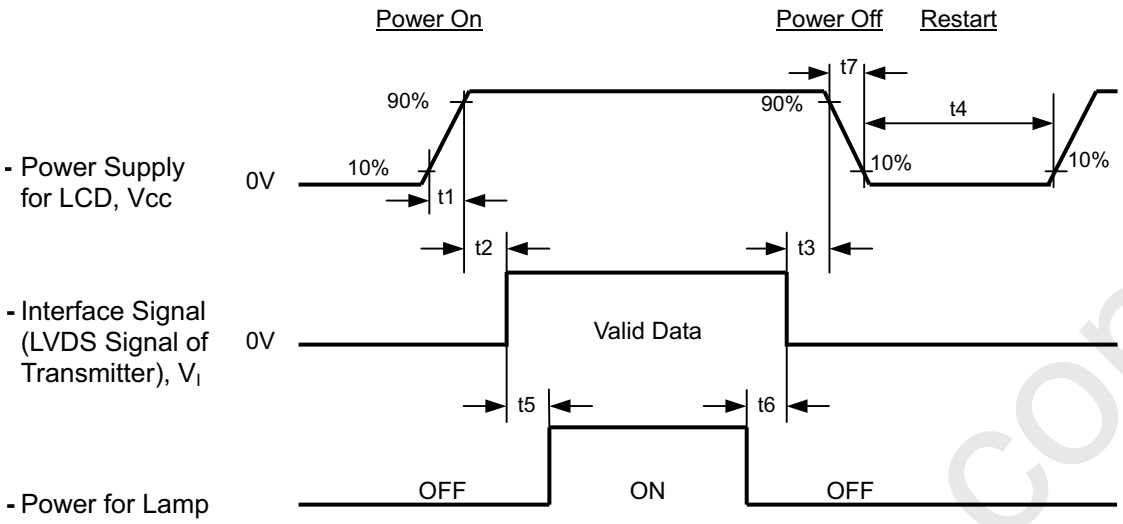
The input signal timing specifications are shown as the following table and timing diagram.

Signal	Item	Symbol	Min.	Typ.	Max.	Unit	Note
DCLK	Frequency	1/Tc	(50)	65	(68)	MHz	-
DE	Vertical Total Time	TV	(771)	806	(850)	TH	-
	Vertical Addressing Time	TVD	(768)	768	(768)	TH	-
	Horizontal Total Time	TH	(1200)	1344	(1500)	Tc	-
	Horizontal Addressing Time	THD	(1024)	1024	(1024)	Tc	-

INPUT SIGNAL TIMING DIAGRAM



6.2 POWER ON/OFF SEQUENCE



Timing Specifications:

$0.5 \leqq t1 \leqq 10$ msec

$0 < t2 \leqq 50$ msec

$0 < t3 \leqq 50$ msec

$t4 \geqq 500$ msec

$t5 \geqq 200$ msec

$t6 \geqq 200$ msec

Note (1) Please avoid floating state of interface signal at invalid period.

Note (2) When the interface signal is invalid, be sure to pull down the power supply of LCD Vcc to 0 V.

Note (3) The Backlight inverter power must be turned on after the power supply for the logic and the interface signal is valid. The Backlight inverter power must be turned off before the power supply for the logic and the interface signal is invalid.

Note (4) Sometimes some slight noise shows when LCD is turned off (even backlight is already off). To avoid this phenomenon, we suggest that the Vcc falling time had better to follow

$t7 \geqq$ 5 msec

7. INVERTER SPECIFICATION

7.1 TYPE OF INVERTER CONNECTOR

Input connector type: **LVC-D20SFYG** (HONDA)

Output connector: **JST SM02B-BHSS-1-TB** (JST)

7.2 BUILT-IN INVERTER INPUT PIN ASSIGNMENT

Input connector		Comments
HONDA	**LVC-D20SFYG**	
Pin	**Function**	
1	INV_SRC	This power rail should be used as a power rail to drive the backlight DC-AC converter
2	INV_SRC	This power rail should be used as a power rail to drive the backlight DC-AC converter
3	INV_SRC	This power rail should be used as a power rail to drive the backlight DC-AC converter
4	NC	No Connection
5	GND	Ground
6	5VSUS	This should be used as power source for the control circuitry on the inverter
7	5VALW	This should be used as power source that stores the brightness/contrast values & the circuit that interfaces with SMB_CLK & SMB_DAT
8	GND	Ground
9	SMB_DAT	SMBus interface for sending brightness & contrast information to the inverter/panel
10	SMB_CLK	SMBus interface for sending brightness & contrast information to the inverter/panel
11	GND	Ground
12	FPBACK	Control signal input into the inverter to turn the backlight ON & OFF (1 - ON, 0 – OFF)
13	GND	Ground
14	LAMP_STAT	Lamp status (Feedback, Lamp On = 5v, Lamp Off 0v), from control chip
15 ~ 20	NC	No Connection

7.3 BUILT-IN INVERTER OUTPUT PIN ASSIGNMENT

Pin	Name	Description
1	CFL-High	High-voltage output to the CCFL

2	CFL-Low	Low-voltage output to the CCFL

7.4 GENERAL ELECTRICAL SPECIFICATION

7.4.1 Absolute Maximum Ratings

Items	Absolute max. ratings	Unit
INV_SRC (Voltage)	-1.0~23.5	V
FPBACK/SMB_CLK/SMB_DAT (Voltage)	-1.0~5.5	V

7.4.2 Electrical Characteristics

No.	Item	Symbol	Condition	Min.	Typ.	Max.	Uint
1	Input Voltage	INV_SRC		7.5	14.4	21	V
2	Input Signal Level for 5VSUS	5VSUS		4.85	5	5.2	V
3	Input Signal Level for 5VALW	5VALW		4.85	5	5.2	V
4	Input Power	Pin(Max)	Vin=7.5V~21V SMB_DAT=00H	TBD	TBD	TBD	W
	CCFL Power	Po	Vin=7.5V~21V SMB_DAT=00H		3.45		W
5	Backlight ON/OFF Control	FPBACK=ON	Enable the inverter	2.0	-	5.25	V
		FPBACK=OFF	Disable the inverter	-0.3	-	0.8	V
6	Brightness Adjust (Lamp Current Control)	SMB_DAT	Control by SMBus	FFH	-	00H	-
7	Output Voltage	Vout	IL = 5.0mA(typ)	(540)	(600)	(660)	Vrms
8	Output Current	Iout (Min)	Vin=7.5V~21V SMB_DAT=FFH Ta=25℃, after running 30 min.	2.0	2.3	2.6	mArms
		Iout (Max)	Vin=7.5V~21V SMB_DAT=00H Ta=25℃, after running 30 min.	4.7	5.0	5.3	mArms
9	Operation Frequency	Freq	Vin=7.5V~21V	(45)	-	(65)	KHz

10	Burst mode frequency	f_B	Vin=7.5V~21V	200	-	220	Hz
11	Open Lamp Voltage	Vopen	No Load	1220	TBD	TBD	Vrms
12	Striking Time	Ts	No Load	0.6	1	1.4	Sec
13	Efficiency	η	Vin=7.5V, SMB_DAT=00H (RES LOAD=100K ohm)	(80)	-	-	%
14	Start and Delay Time		Vin=14.4V, SMB_DAT=FFH	-	130	200	uS
15	Start –up time(Turn on delay time)			-	-	0.1	Sec

Remarks:

- Input Voltage

  The operating input voltage of inverter shall be defined.

  The inverter shall ignite the CCFL lamp at minimum input voltage at any environment conditions.

- On/Off control

  Enable: At "**ON**" condition (FPBACK=Hi), enable the inverter.

  Disable: At "**OFF**" condition (FPBACK=Lo), disable the inverter.

- Quiescent current

  At the inverter "**OFF**" condition, input quiescent should be less than 0.1mA.

- Open lamp voltage

  The inverter start-up output voltage will be above "**Vopen**" for "**Ts**" minimum at any condition under specify until lamp to be ignited. The inverter should be shutdown if lamp ignition was failed in "**Ts**" maximum. The inverter shall be capable of withstanding the output connections open without component over-stress / fire / smoke /arc.

- Burst mode frequency

  The burst mode frequency should be in specification in any environment condition and electrical condition.

- Brightness control

  SM-BUS values for panel luminance are to be included in the on LCD board EEDID ROM chip table. The supplier will measure panel luminance in a system and define the SMBUS values for each of the 8 required luminance levels. The panel luminance, for which SMBUS values will be provided in the EEDID from byte # 113(hex #71), to byte # 120, (hex # 78), is show in the table below. The inverter supplier should provide these appropriate values to CMO.

Step Count	Step 1	Step 2	Step3	Step 4	Step 5	Step 6	Step 7	Step 8
Address	Byte 113	Byte 114	Byte 115	Byte 116	Byte 117	Byte 118	Byte 119	Byte 120
SM-Bus Data Value	(E5)	(D1)	(C3)	(BA)	(91)	(6C)	(44)	(00)
Luminance (nits)	10	17	24	30	60	90	120	MAX

- Output ripple ratio

  Ripple ratio = 2 * (Ipeak - Ivalley) / (Ipeak + Ivalley) * 100%

  The Ripple ratio should be less than 5% and ripple frequency should be less than 200 Hz.

- Power up Overshoot & Undershoot

  Overshoot & Undershoot at power up should not exceed the following limits.

Vin	Output current Io(rms)	Io (dI) Overshoot/Undershoot	Settling time (dT)
0→Vin(min.)	Io(max.)	150% / 50%	5 ms max.
	Io(min.)		
0→Vin(typ.)	Io(max.)	150% / 50%	5 ms max.
	Io(min.)		
0→ Vin(max.)	Io(max.)	150% / 50%	5 ms max.
	Io(min.)		

  dI=Imax.-Io or dI=(Io-Imin.)/Io

- Output connections short protection

  The inverter shall be capable of withstanding the output connections short without damage or over-stress. And the inverter maximum input power shall be limited within 1W.

8. OPTICAL CHARACTERISTICS

8.1 TEST CONDITIONS

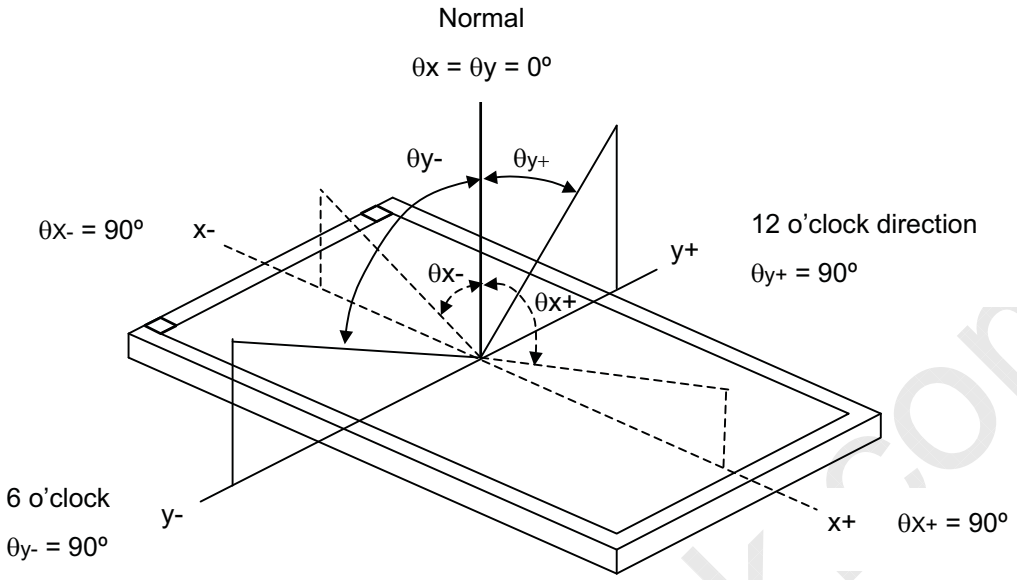
Item	Symbol	Value	Unit
Ambient Temperature	Ta	25±2	°C
Ambient Humidity	Ha	50±10	%RH
Supply Voltage	V_{CC}	3.3	V
Input Signal	According to typical value in "3. ELECTRICAL CHARACTERISTICS"		
Inverter Current	I_L	5.0	mA
Inverter Driving Frequency	F_L	(55)	KHz
Inverter	Sumida-H05-4915		

The measurement methods of optical characteristics are shown in Section 7.2. The following items should be measured under the test conditions described in Section 7.1 and stable environment shown in Note (6).

8.2 OPTICAL SPECIFICATIONS

Item		Symbol	Condition	Min.	Typ.	Max.	Unit	Note
Color Chromaticity	Red	Rx	θ_x=0°, θ_Y =0° Viewing Normal Angle (CS-1000T)	TYP -0.03	0.590	TYP +0.03	-	(1), (6)
		Ry			0.335		-	
	Green	Gx			0.320		-	
		Gy			0.530		-	
	Blue	Bx			0.150		-	
		By			0.135		-	
	White	Wx			0.313		-	
		Wy			0.329		-	
	Color Gamut	C.G%		42	45	-	%	(8)
Average luminance of white		L_{AVE}		(145)	(175)	-	cd/m^2	(4), (6)
Contrast Ratio		CR		(250)	(400)	-	-	(2), (6)
Response Time		T_R	θ_x=0°, θ_Y =0°	-	5	10	ms	(3)
		T_F		-	11	16	ms	
Cross Talk		CT	θ_x=0°, θ_Y =0° (BM-5A)	-	-	4.0	%	(5), (6)
White Variation of 5 Points		δW_{5p}		80	-	-	%	(6), (7)
White Variation of 13 Points		δW_{13p}		55	-	-	%	
Viewing Angle	Horizontal	θ_x+	CR≥10 (BM-5A)	40	-	-	Deg.	(1), (6)
		θ_x-		40	-	-		
	Vertical	θ_Y+		10	-	-		
		θ_Y-		30	-	-		

Note (1) Definition of Viewing Angle (θx, θy):



Note (2) Definition of Contrast Ratio (CR):

The contrast ratio can be calculated by the following expression.

Contrast Ratio (CR) = L63 / L0

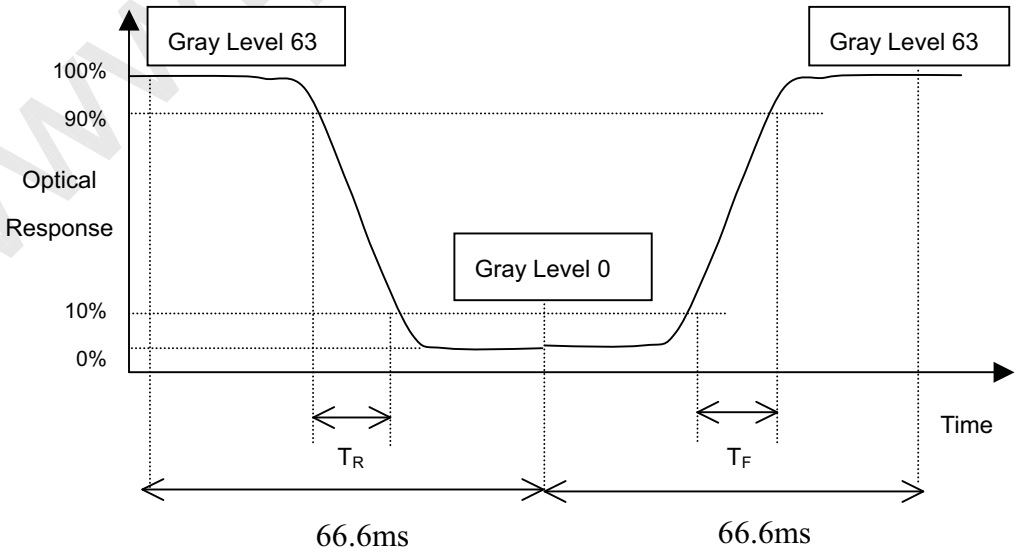
L63: Luminance of gray level 63

L 0: Luminance of gray level 0

CR = CR (5)

CR (X) is corresponding to the Contrast Ratio of the point X at Figure in Note (7).

Note (3) Definition of Response Time (T_R, T_F) and measurement method:



Note (4) Definition of Average Luminance of White (L_{AVE}):

Measure the luminance of gray level 63 at 5 points

L_{AVE} = [L (1)+ L (2)+ L (3)+ L (4)+ L (5)] / 5

L (x) is corresponding to the luminance of the point X at Figure in Note (7).

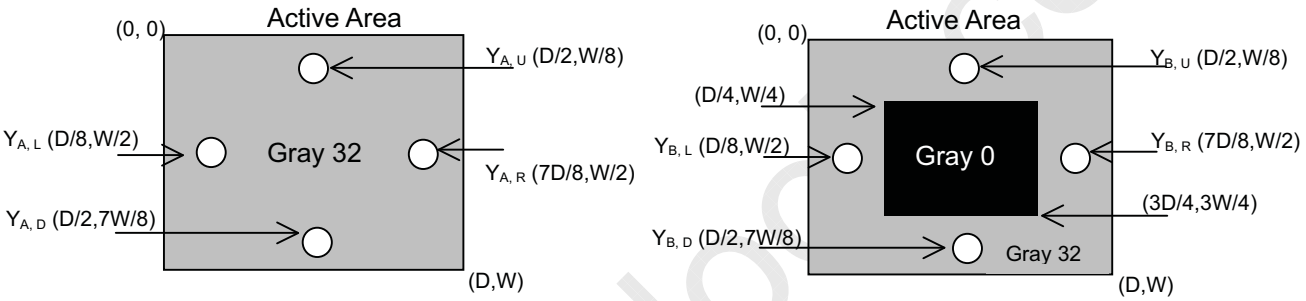
Note (5) Definition of Cross Talk (CT):

$CT = | Y_B – Y_A | / Y_A \times 100$ (%)

Where:

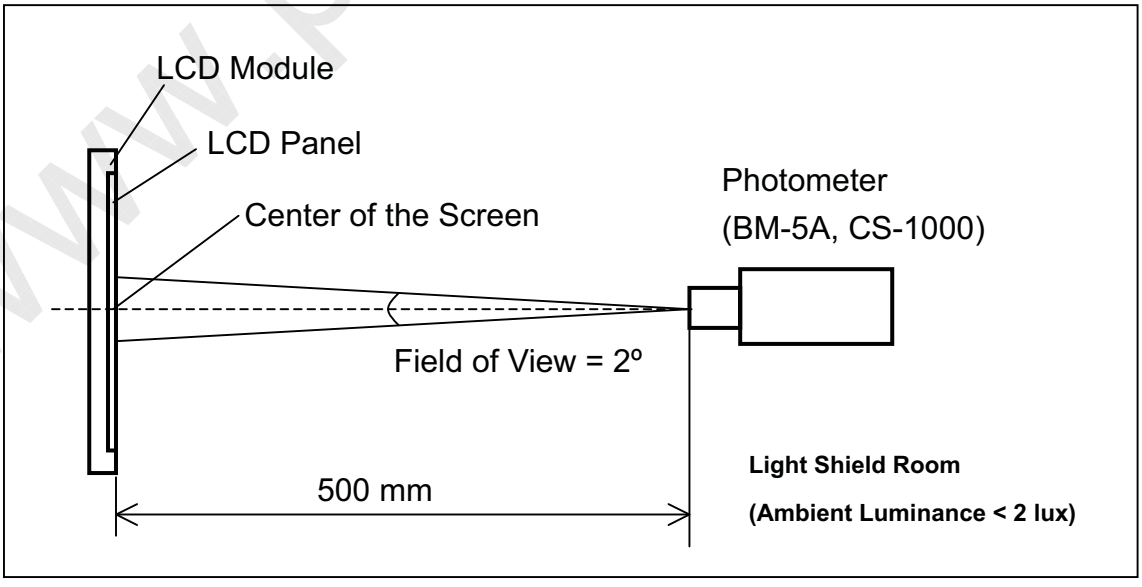
Y_A = Luminance of measured location without gray level 0 pattern (cd/m^2)

Y_B = Luminance of measured location with gray level 0 pattern (cd/m^2)



Note (6) Measurement Setup:

The LCD module should be stabilized at given temperature for 20 minutes to avoid abrupt temperature change during measuring. In order to stabilize the luminance, the measurement should be executed after lighting Backlight for 20 minutes in a windless room.

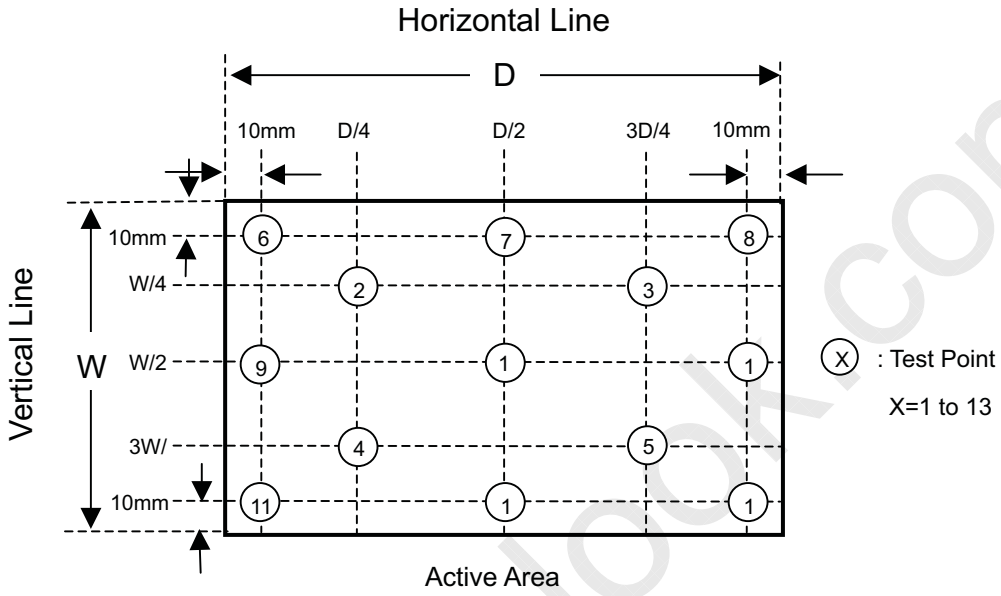


Note (7) Definition of White Variation (δW):

Measure the luminance of gray level 63 at 5 points

δW_{5p} = Minimum [L (1), L (2), L (3), L (4), L (5)] / Maximum [L (1), L (2), L (3), L (4), L (5)]

δW_{13p} = Minimum [L (1) ~ L (13)] / Maximum [L (1) ~ L (13)]



Note (8) Definition of color gamut (C.G%):

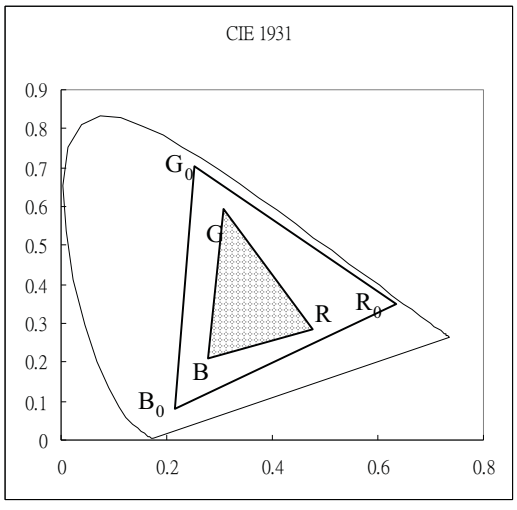
C.G%= R G B / R_0 G_0 B_0,*100%

R_0, G_0, B_0 : color coordinates of red, green, and blue defined by NTSC, respectively.

R, G, B : color coordinates of module on 63 gray levels of red, green, and blue, respectively.

R_0 G_0 B_0 : area of triangle defined by R_0, G_0, B_0

R G B: area of triangle defined by R, G, B



9. PRECAUTIONS

9.1 HANDLING PRECAUTIONS

(1) The module should be assembled into the system firmly by using every mounting hole. Be careful not to twist or bend the module.

(2) While assembling or installing modules, it can only be in the clean area. The dust and oil may cause electrical short or damage the polarizer.

(3) Use fingerstalls or soft gloves in order to keep display clean during the incoming inspection and assembly process.

(4) Do not press or scratch the surface harder than a HB pencil lead on the panel because the polarizer is very soft and easily scratched.

(5) If the surface of the polarizer is dirty, please clean it by some absorbent cotton or soft cloth. Do not use Ketone type materials (ex. Acetone), Ethyl alcohol, Toluene, Ethyl acid or Methyl chloride. It might permanently damage the polarizer due to chemical reaction.

(6) Wipe off water droplets or oil immediately. Staining and discoloration may occur if they left on panel for a long time.

(7) If the liquid crystal material leaks from the panel, it should be kept away from the eyes or mouth. In case of contacting with hands, legs or clothes, it must be washed away thoroughly with soap.

(8) Protect the module from static electricity, it may cause damage to the C-MOS Gate Array IC.

(9) Do not disassemble the module.

(10) Do not pull or fold the lamp wire.

(11) Pins of I/F connector should not be touched directly with bare hands.

9.2 STORAGE PRECAUTIONS

(1) High temperature or humidity may reduce the performance of module. Please store LCD module within the specified storage conditions.

(2) It is dangerous that moisture come into or contacted the LCD module, because the moisture may damage LCD module when it is operating.

(3) It may reduce the display quality if the ambient temperature is lower than 10 ºC. For example, the response time will become slowly, and the starting voltage of lamp will be higher than the room temperature.

9.3 OPERATION PRECAUTIONS

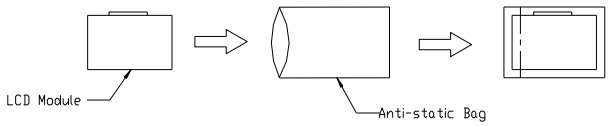
(1) Do not pull the I/F connector in or out while the module is operating.

(2) Always follow the correct power on/off sequence when LCD module is connecting and operating. This can prevent the CMOS LSI chips from damage during latch-up.

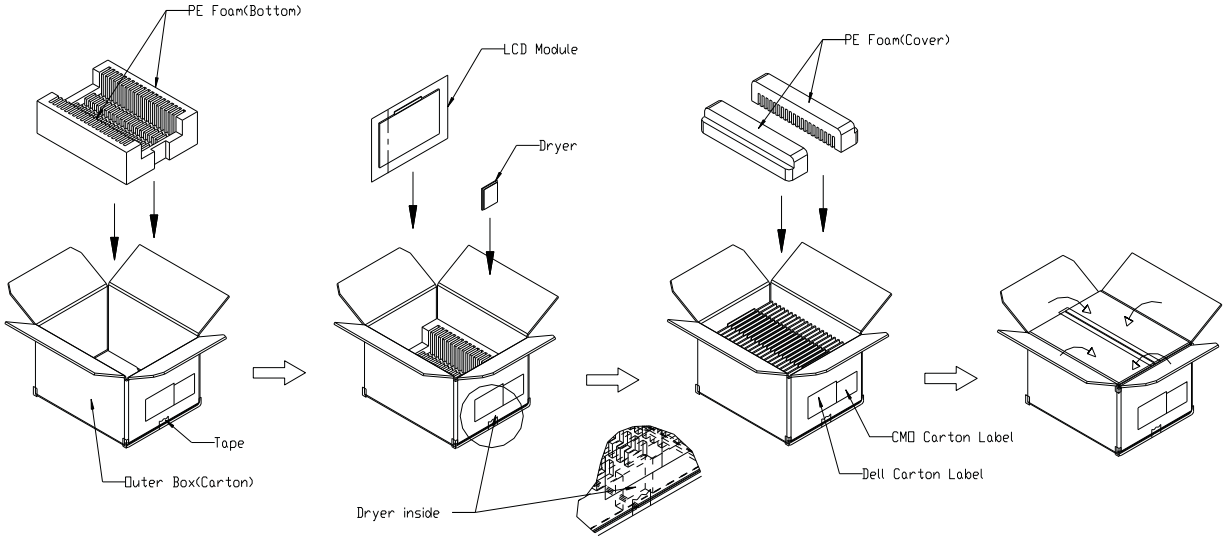
(3) The startup voltage of Backlight is approximately 1000 Volts. It may cause electrical shock while assembling with inverter. Do not disassemble the module or insert anything into the Backlight unit.

10. PACKING

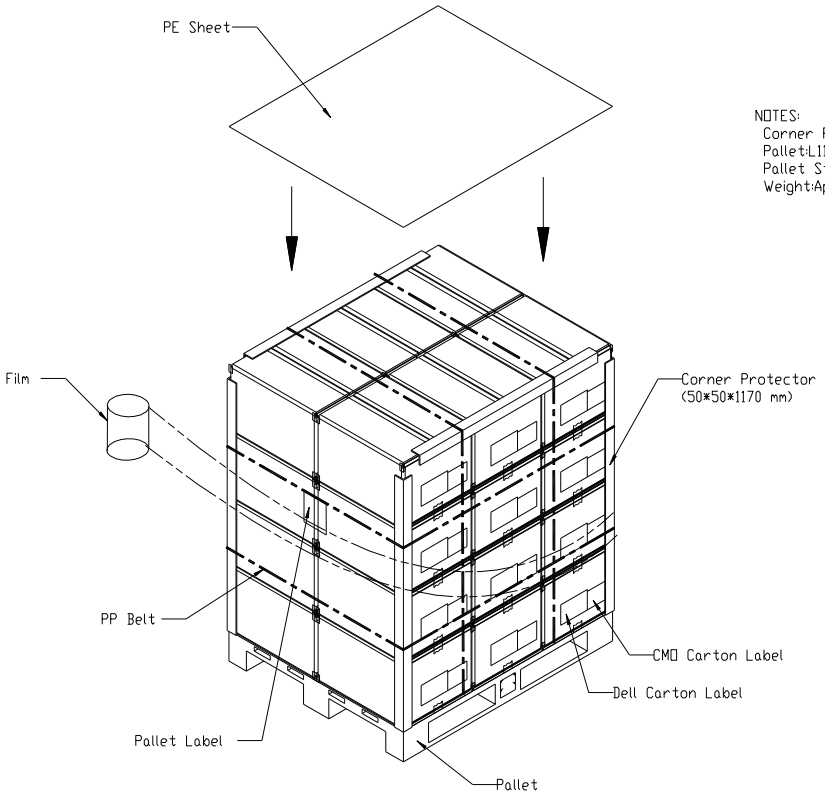
10.1 CARTON



Box Dimesions: 489(L)*382(W)*330(H)
Weight: Approx. 6.9kg(20 module .per. 1box)



10.2 PALLET

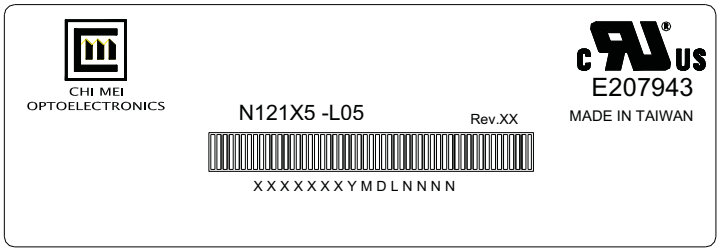


NOTES:
Corner Protector:L1170mm*50mm*50mm
Pallet:L1180*W1000*H135mm
Pallet Stock Dim:L1180*W1000*H1465mm
Weight:Approx.186kg

11. DEFINITION OF LABELS

11.1 CMO MODULE LABEL

The barcode nameplate is pasted on each module as illustration, and its definitions are as following explanation.



(a) Model Name: N121X5 - L05

(b) Revision: Rev. XX, for example: A1, …, C1, C2 …etc.

(c) Serial ID: X X X X X X Y M D X N N N N

- Serial No.
- CMO Internal Use
- Year, Month, Date
- CMO Internal Use
- Revision
- CMO Internal Use

Serial ID includes the information as below:

(a) Manufactured Date: Year: 1~9, for 2001~2009

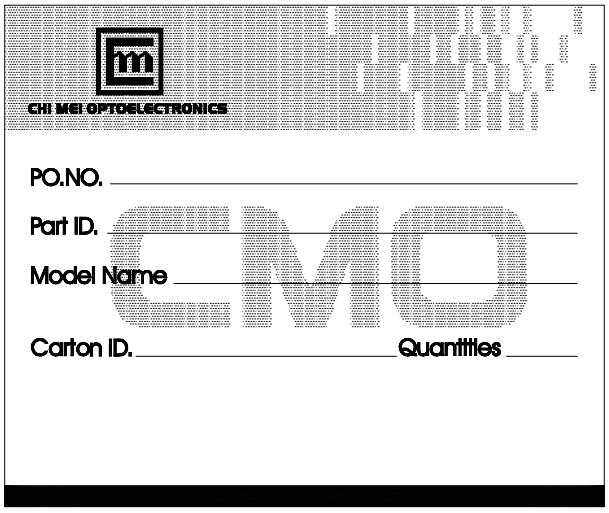
Month: 1~9, A~C, for Jan. ~ Dec.

Day: 1~9, A~Y, for 1st to 31st, exclude I , O and U

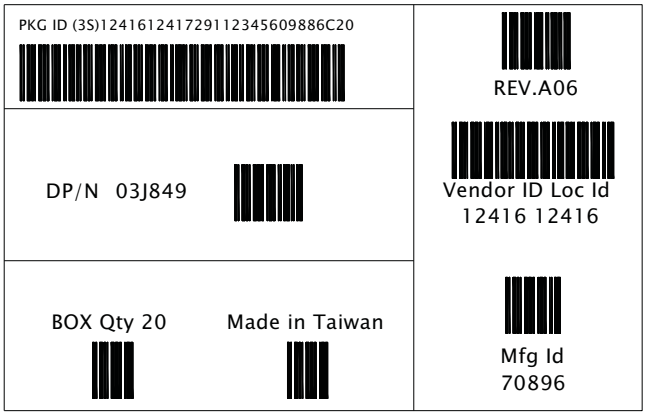
(b) Revision Code: cover all the change

(c) Serial No.: Manufacturing sequence of product

11.2 CARTON LABEL



11.3 CUSTOMER CARTON LABEL



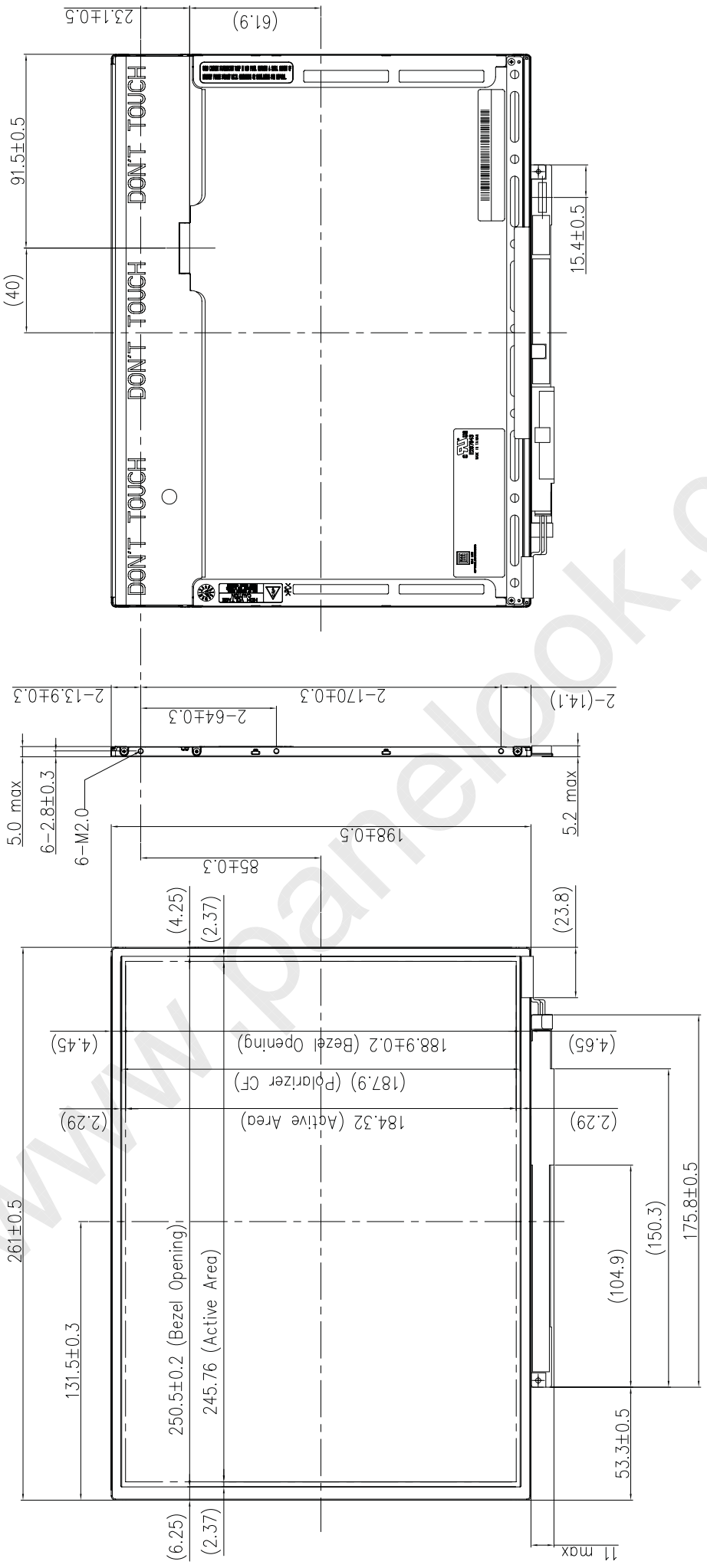
Type J Label

- Verdana font or equivalent,bold
- 20pt.–all fields
- 203 DPI printer minimum
- Code 128B
- 10–15 mil minimum narrow bar
- .75"minimum barcode height
- .10" or greater quiet zone
- 4.0" x 6.0" label size
- Brady THT –25–402–1 or equivalent
- Brady R6107 series ribbon or equivalent

11.4 CUSTOMER PALLET LABEL

Type K Label

- Verdana font or equivalent,bold
- 12pt.–all descript fields
- 10pt.–all data fields
- 203 DPI printer minimum
- Code 128B
- 10 mil minimum narrow bar
- .30–,50"minimum barcode height
- .10" or greater quiet zone
- 4.0" x 6.5" label size
- Brady THT –78–402–.9 or equivalent
- Brady R6107 series ribbon or equivalent



NOTES:
1."*" MARKS THE DESIGN CRITICAL DIMENSION.
2." Ⓟ " MARKS THE PROCESS CRITICAL DIMENSION.
3.MAX.SCREW LENGTH: 2.5 mm.
4.MAX.SCREW TORQUE: 2.0 kgf-cm.
5.SIGNAL INTERFACE CONNECTOR: DF19L-20P-1H (HIROSE)
6.CCFL CONNECTOR: BHSR-02VS-1 (JST)

TITLE	ASSY_MODULE_N121X5-L05			2D REV.	1		
Approved	Bill Sheu	Drawing No.	N121S4L041	3D REV.	1.1		
Checked	Yule Sheu	Part No.				Sheet	1 / 1
Drawer	Mulciber Hsieh	Material					A1
Designer	Mulciber Hsieh	Date	04-Feb-2005	Scale	1:1	Unit:mm	

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Mark	Description	Date	Changed_By	Approved_By	ECN No.	Remark