

## MM74HC594 8-Bit Shift Register with Output Registers

### General Description

This high speed shift register utilizes advanced silicon-gate CMOS technology. This device possesses the high noise immunity and low power consumption of standard CMOS integrated circuits, as well as the ability to drive 15 LS-TTL loads.

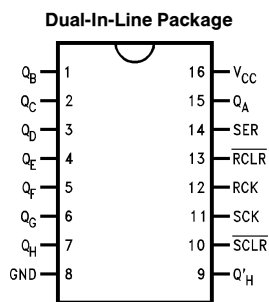
This device contains an 8-bit serial-in, parallel-out shift register that feeds an 8-bit D-type storage register. Separate clocks and direct overriding clears are provided for both the shift register and the storage register. The shift register has a direct-overriding clear, serial input, and serial output (standard) pins for cascading. Both the shift register and storage register use positive-edge triggered clocks. If both clocks are connected together, the shift register state will always be one clock pulse ahead of the storage register.

The 54HC/74HC logic family is speed, function, and pin-out compatible with the standard 54LS/74LS logic family. All inputs are protected from damage due to static discharge by internal diode clamps to  $V_{CC}$  and ground.

### Features

- Low quiescent current: 80  $\mu A$  maximum (74HC Series)
- Low input current: 1  $\mu A$  maximum
- 8-bit serial-in, parallel-out shift register with storage
- Wide operating voltage range: 2V–6V
- Cascadable
- Shift register has direct clear
- Guaranteed shift frequency: DC to 30 MHz

### Connection Diagram



Top View

**Order Number MM74HC594**  
**See NS Package Number N16E**

TL/F/10915–1

### Truth Table

RCK	SCK	$\overline{SCLR}$	$\overline{RCLR}$	Function
X	X	X	L	Storage Register cleared
X	X	L	X	Shift Register cleared $Q'_H = 0$
X	$\uparrow$	H	H	Shift Register clocked $Q_N = Q_{n-1}$ , $Q_0 = SER$
$\uparrow$	X	H	H	Contents of Shift Register transferred to output latches

**Absolute Maximum Ratings** (Notes 1 & 2)

Supply Voltage ( $V_{CC}$ )	−0.5 to +7.0V
DC Input Voltage ( $V_{IN}$ )	−1.5 to $V_{CC} + 1.5V$
DC Output Voltage ( $V_{OUT}$ )	−0.5 to $V_{CC} + 0.5V$
Clamp Diode Current ( $I_{IK}, I_{OK}$ )	±20 mA
DC Output Current, per pin ( $I_{OUT}$ )	±35 mA
DC $V_{CC}$ or GND Current, per pin ( $I_{CC}$ )	±70 mA
Storage Temperature Range ( $T_{STG}$ )	−65°C to +150°C
Power Dissipation ( $P_D$ )	
(Note 3)	600 mW
S.O. Package only	500 mW
Lead Temp. ( $T_L$ ) (Soldering 10 seconds)	260°C

**Operating Conditions**

	Min	Max	Units
Supply Voltage ( $V_{CC}$ )	2	6	V
DC Input or Output Voltage ( $V_{IN}, V_{OUT}$ )	0	$V_{CC}$	V
Operating Temp. Range ( $T_A$ )			
MM74HC	−40	+85	°C
Input Rise or Fall Times ( $t_r, t_f$ )			
$V_{CC} = 2.0V$		1000	ns
$V_{CC} = 4.5V$		500	ns
$V_{CC} = 6.0V$		400	ns

**DC Electrical Characteristics** (Note 4)

Symbol	Parameter	Conditions	V <sub>CC</sub>	T <sub>A</sub> = 25°C		74HC T <sub>A</sub> = − 40 to 85°C		Units
				Typ	Guaranteed Limits			
V <sub>IH</sub>	Minimum High Level Input Voltage		2.0V		1.5	1.5	V	
			4.5V		3.15	3.15	V	
			6.0V		4.2	4.2	V	
V <sub>IL</sub>	Maximum Low Level Input Voltage		2.0V		0.5	0.5	V	
			4.5V		1.35	1.35	V	
			6.0V		1.8	1.8	V	
V <sub>OH</sub>	Minimum High Level Output Voltage	V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub>  I <sub>OUT</sub>   ≤ 20 μA	2.0V	2.0	1.9	1.9	V	
			4.5V	4.5	4.4	4.4	V	
			6.0V	6.0	5.9	5.9	V	
	Q' <sub>H</sub>	V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub>  I <sub>OUT</sub>   ≤ 4.0 mA  I <sub>OUT</sub>   ≤ 5.2 mA	4.5V	4.2	3.98	3.84	V	
			6.0V	5.2	5.48	5.34	V	
	Q <sub>A</sub> thru Q <sub>H</sub>	V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub>  I <sub>OUT</sub>   ≤ 6.0 mA  I <sub>OUT</sub>   ≤ 7.8 mA	4.5V	4.2	3.98	3.84	V	
6.0V			5.7	5.48	5.34	V		
V <sub>OL</sub>	Maximum Low Level Output Voltage	V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub>  I <sub>OUT</sub>   ≤ 20 μA	2.0V	0	0.1	0.1	V	
			4.5V	0	0.1	0.1	V	
			6.0V	0	0.1	0.1	V	
	Q' <sub>H</sub>	V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub>  I <sub>OUT</sub>   ≤ 4 mA  I <sub>OUT</sub>   ≤ 5.2 mA	4.5V	0.2	0.26	0.33	V	
			6.0V	0.2	0.26	0.33	V	
	Q <sub>A</sub> thru Q <sub>H</sub>	V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub>  I <sub>OUT</sub>   ≤ 6.0 mA  I <sub>OUT</sub>   ≤ 7.8 mA	4.5V	0.2	0.26	0.33	V	
6.0V			0.2	0.26	0.33	V		
I <sub>IN</sub>	Maximum Input Current	V <sub>IN</sub> = V <sub>CC</sub> or GND	6.0V		± 0.1	± 1.0	μA	
I <sub>CC</sub>	Maximum Quiescent Supply Current	V <sub>IN</sub> = V <sub>CC</sub> or GND I <sub>OUT</sub> = 0 μA	6.0V		8.0	80	μA	

**Note 1:** Absolute Maximum Ratings are those values beyond which damage to the device may occur.

**Note 2:** Unless otherwise specified all voltages are referenced to ground.

**Note 3:** Power Dissipation temperature derating — plastic “N” package: −12 mW/°C from 65°C to 85°C; ceramic “J” package: −12 mW/°C from 100°C to 125°C.

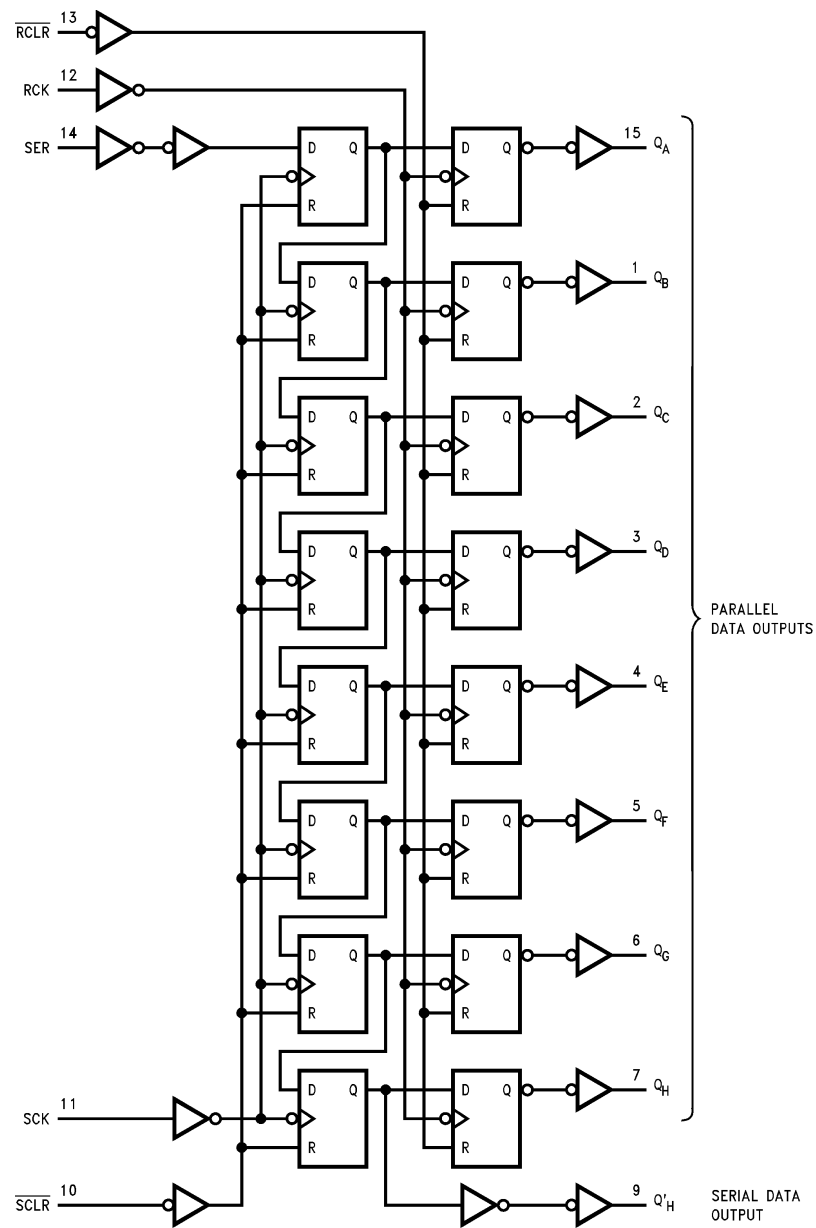
**Note 4:** For a power supply of 5V ±10% the worst case output voltages ( $V_{OH}$  and  $V_{OL}$ ) occur for HC at 4.5V. Thus the 4.5V values should be used when designing with this supply. Worst case  $V_{IH}$  and  $V_{IL}$  occur at  $V_{CC} = 5.5V$  and 4.5V respectively. (The  $V_{IH}$  value at 5.5V is 3.85V.) The worst case leakage current ( $I_{IN}$  and  $I_{CC}$ ) occur for CMOS at the higher voltage and so the 6.0V values should be used.

# AC Electrical Characteristics $V_{CC} = 2.0\text{--}6.0\text{V}$ , $C_L = 50\text{ pF}$ , $t_r = t_f = 6\text{ ns}$ (unless otherwise specified)

Symbol	Parameter	Conditions	V <sub>CC</sub>	T <sub>A</sub> = 25°C		74HC T <sub>A</sub> = −40 to 85°C		Units
				Typ	Guaranteed Limits			
f <sub>MAX</sub>	Maximum Operating Frequency	C <sub>L</sub> = 50 pF	2.0V 4.5V 6.0V		6 30 35	4.8 24 28		MHz MHz MHz
t <sub>PHL</sub> , t <sub>PLH</sub>	Maximum Propagation Delay from SCK to Q' <sub>H</sub>	C <sub>L</sub> = 50 pF	2.0V 4.5V 6.0V		150 30 25	185 37 31		ns ns ns
t <sub>PHL</sub> , t <sub>PLH</sub>	Maximum Propagation Delay from RCK to Q <sub>A</sub> thru Q <sub>H</sub>	C <sub>L</sub> = 50 pF	2.0V		150	185		ns
		C <sub>L</sub> = 150 pF	2.0V		200	250		ns
		C <sub>L</sub> = 50 pF	4.5V		30	37		ns
		C <sub>L</sub> = 150 pF	4.5V		40	50		ns
		C <sub>L</sub> = 50 pF	6.0V		25	31		ns
		C <sub>L</sub> = 150 pF	6.0V		34	43		ns
t <sub>PHL</sub> , t <sub>PLH</sub>	Maximum Propagation Delay from SCLR to Q' <sub>H</sub>		2.0V 4.5V 6.0V		150 30 25	185 37 31		ns ns ns
t <sub>PHL</sub>	Maximum Propagation Delay from RCLR to Q <sub>A</sub> thru Q <sub>H</sub>	C <sub>L</sub> = 50 pF	2.0V		125	155		ns
			4.5V		25	31		ns
			6.0V		21	26		ns
			C <sub>L</sub> = 150 pF	2.0V 4.5V 6.0V		200 40 34	250 50 43	
t <sub>S</sub>	SCLR Low to RCK		2.0V 4.5V 6.0V		50 10 9	63 13 11		ns ns ns
t <sub>S</sub>	RCLR High to SCK		2.0V		5	5		ns
			4.5V		5	5		ns
			6.0V		5	5		ns
t <sub>S</sub>	Minimum Setup Time from SER to SCK		2.0V		90	110		ns
			4.5V		18	22		ns
			6.0V		15	19		ns
t <sub>R</sub>	Minimum Removal Time from SCLR to SCK		2.0V		20	20		ns
			4.5V		10	10		ns
			6.0V		10	10		ns
t <sub>S</sub>	Minimum Setup Time from SCK to RCK		2.0V		90	110		ns
			4.5V		18	22		ns
			6.0V		15	19		ns
t <sub>H</sub>	Minimum Hold Time SER to SCK		2.0V 4.5V 6.0V		5 5 5	5 5 5		ns ns ns
t <sub>W</sub>	Minimum Pulse Width of SCK or SCLR or RCK or RCLR		2.0V		100	125		ns
			4.5V		20	25		ns
			6.0V		17	21		ns
t <sub>r</sub> , t <sub>f</sub>	Maximum Input Rise and Fall Time, Clock		2.0V		1000	1000		ns
			4.5V		500	500		ns
			6.0V		400	400		ns
t <sub>THL</sub> , t <sub>TLH</sub>	Maximum Output Rise and Fall Time Q <sub>A</sub> –Q <sub>H</sub>		2.0V		60	75		ns
			4.5V		12	15		ns
			6.0V		10	13		ns
t <sub>THL</sub> , t <sub>TLH</sub>	Maximum Output Rise and Fall Time Q' <sub>H</sub>		2.0V		75	95		ns
			4.5V		15	19		ns
			6.0V		13	16		ns
C <sub>PD</sub>	Power Dissipation Capacitance, Outputs Enabled (Note 6)	G <sub>0</sub> = V <sub>CC</sub> G <sub>0</sub> = GND		90 150				pF pF
C <sub>IN</sub>	Maximum Input Capacitance			5	10	10		pF
C <sub>OUT</sub>	Maximum Output Capacitance			15	20	20		pF

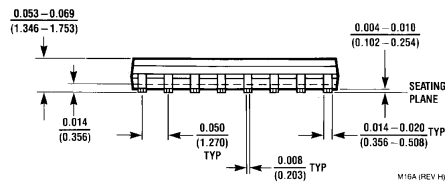
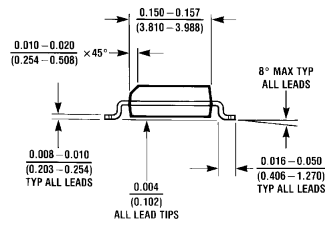
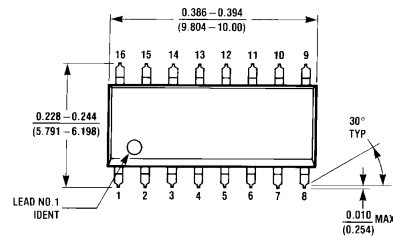
**Note 6:**  $C_{PD}$  determines the no load dynamic power consumption,  $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$ , and the no load dynamic current consumption,  $I_S = C_{PD} V_{CC} f + I_{CC}$ .

# **Logic Diagram** (positive logic)

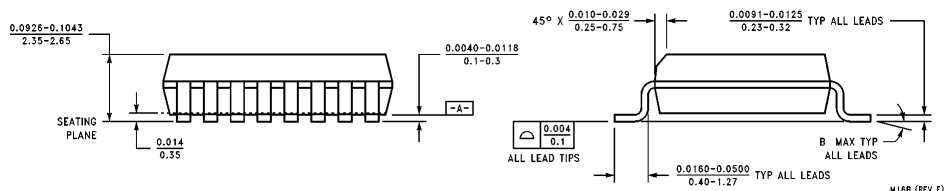
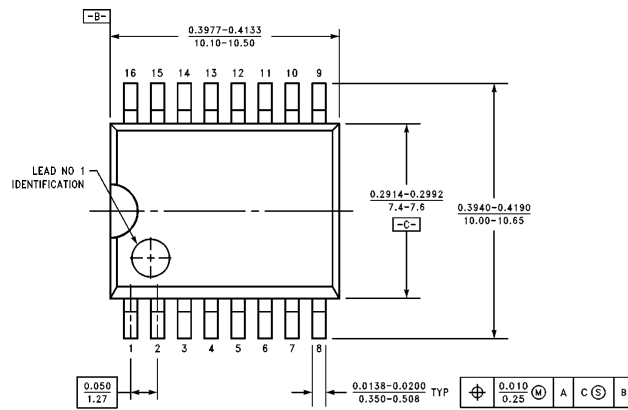


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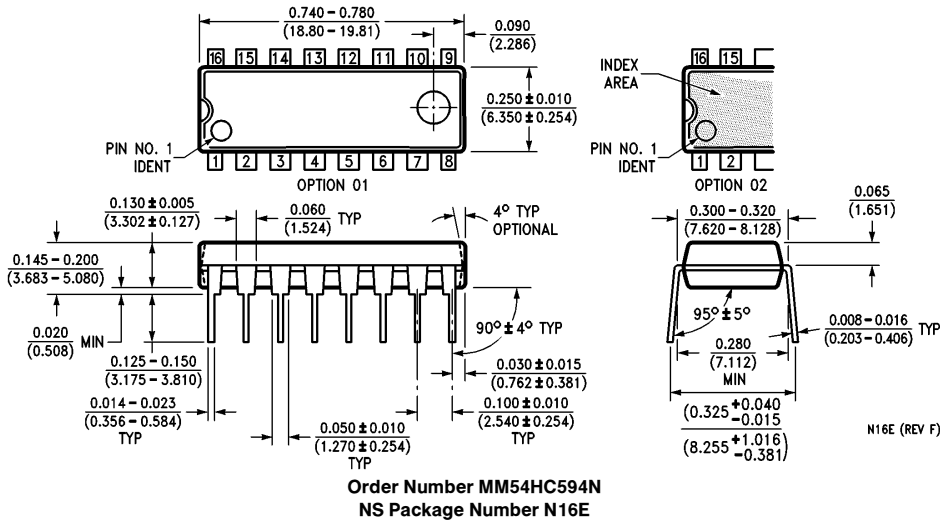
# Physical Dimensions inches (millimeters)



Order Number MM74HC594M  
NS Package Number M16A



Order Number MM74HC594WM  
NS Package Number M16B

**Physical Dimensions** inches (millimeters) (Continued)**LIFE SUPPORT POLICY**

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