L5953

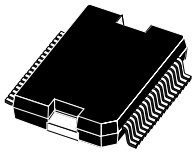
Multiple switching voltage regulator

Features

- PWM: adjustable 2.5/10V - 1A switching voltage regulator
- External POWER MOS ability for output current enhancement
- Synchronization function
- REG1- Linear low drop 3.3/5V - 250mA STBY voltage regulator (low current consumption) with RESET
- REG2- Linear voltage regulator 1.5V to 3.3V externally adjustable - 300mA maximum current
- HSD1 : 500mA High side driver
- HSD2 : 200mA High side driver
- SPI Interface
- SPI Diagnostics HSD1, HSD2
- Double switching frequency SPI selectable
- Double inpuT LVW

SPI functions

- Input controls
  - Turn-on/off PWM
  - Turn-on/off REG2
  - Turn-on/off HSD1
  - Turn-on/off HSD2
  - Switching frequency selection f1- f2
- Output functions:
  - HSD1 & HSD2 short to gnd, open load and short to battery (Test mode)
  - Thermal warning



PowerSO36

Protections

- Over voltage protection
- Internal current limiting
- Thermal shutdown
- ESD

Description

The L5953 is the integration of one switching regulator, two linear voltage regulators, two low voltage warnings and two high side drivers. It has a stand-by operation mode (low current consumption) where only the stand-by voltage regulator plus the low voltage warnings are active. The other regulators and high side drivers are controlled by the SPI interface.

Table 1. Device summary

Part number	Package	Packing
L5953	PowerSO36	Tray

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1 Block diagram and electrical specifications

Figure 1. Block diagram

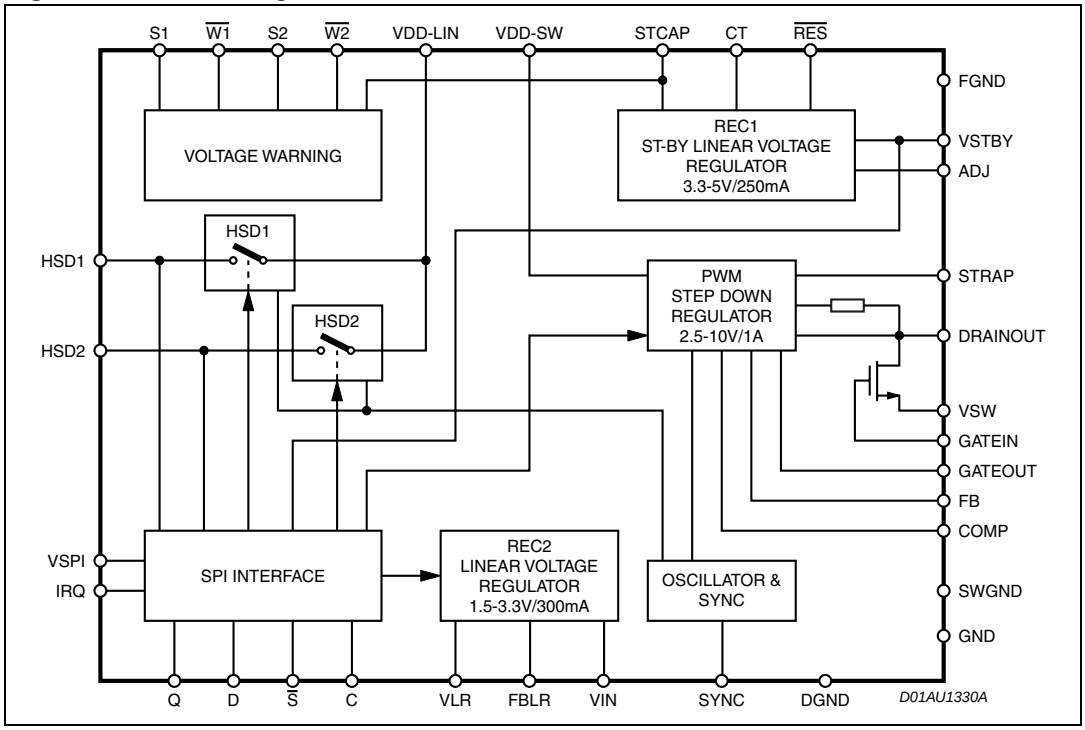


Table 2. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{DD}	DC operating supply voltage	-0.6 to 30	V
	Transient supply over voltage (250ms)	50	V
V_{SPI}	Supply voltage for SPI I/O	-0.6 to 6	V
I_O	Voltage regulator output current	Internally limited	
V_{inlog}	Input voltage (C, D, Q, $\overline{S}$, SYNC)	0 to 6	V
RESR	Output capacitor series e.g. resistance (linear reg.) (allowed range)	From 0.2 to 10	W
T_{op}	Operating temperature range	-40 to 85	°C
T_{stg}	Storage temperature ranges	-55 to 150	°C
T_j	Operative junction temperature	-40 to 150	°C

Table 3. Thermal data

Symbol	Parameter	Value	Unit
$R_{thj\text{-}case}$	Thermal resistance junction to case	1.7	°C/W

Figure 2. PIN connections

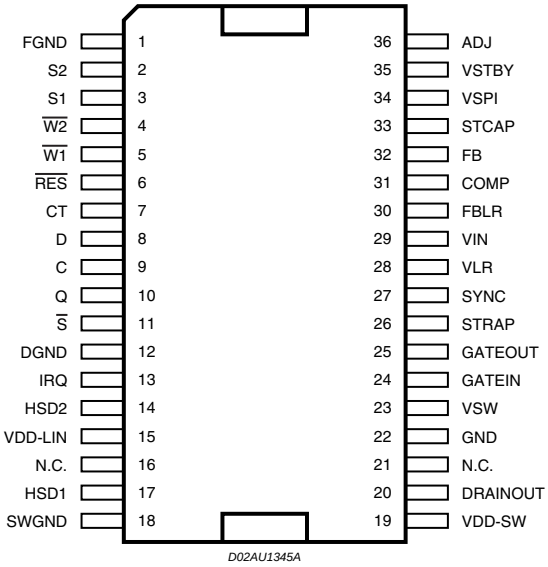


Table 4. PIN function

Pin number	Pin name	Function
1	FGND	Analog ground
2	S2	Input voltage for LVW2
3	S1	Input voltage for LVW1
4	W2	LVW2 output
5	W1	LVW1 output
6	RES	Reset
7	CT	Timing capacitor
8	D	SPI serial input
9	C	SPI clock
10	Q	SPI serial output
11	S	SPI chip select
12	DGND	SPI ground
13	IRQ	Interrupt
14	HSD2	HSD2 output
15	VDD-LIN	Battery
16	N.C.	Not connected
17	HSD1	HSD1 output
18	SWGND	Switching ground
19	VDD-SW	PWM battery
20	DRAINOUT	Drain of the external MOS

Table 4. PIN function (continued)

Pin number	Pin name	Function
21	N.C.	Not connected
22	GND	Ground
23	VSW	Source of the external MOS
24	GATEIN	Gate of the internal MOS
25	GATEOUT	Switching output for power mos gate
26	STRAP	Bootstrap
27	SYNC	Synchronization
28	VLR	REG2 linear voltage regulator output
29	VIN	REG2 linear voltage regulator input
30	FBLR	REG2 linear voltage regulator feedback
31	COMP	PWM compensation
32	FB	PWM feedback
33	STCAP	ST-CAP
34	VSPI	Supply voltage for SPI I/O
35	VSTBY	REG1 stand-by linear voltage regulator output
36	ADJ	3.3V/5V REG1 voltage select

Table 5. Electrical characteristics (T_{amb} = 25°C, V_{DD} = 14.4V)

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
$I_{Q,STBY}$	Quiescent current with regulators and high-side drivers off	$\overline{W1}$, $\overline{W2}$, $\overline{RES}$, IRQ, not active; REG2, HSD1, HSD2, PWM off; $\overline{S}$, C, D fixed at high/low logic level			100	µA
T_{sd}	Thermal shutdown junction temperature			150		°C
SMPS.PWM (T_{amb} = 25°C, V_{DD} = 14.4V, V_o = 5V; unless otherwise specified.)						
$V_{o,min}$	Minimum output voltage	I_o = 200mA	2.4	2.5	2.6	V
$V_{o,max}$	Maximum output voltage	I_o = 200mA	9.6	10	10.4	V
Vref,PWM	Voltage reference			1.275		V
V_i	Input voltage range	V_o = 5V; I_o = 0.5A	6		18	V
ΔV_o	Line regulation	I_o = 0.5A			100	mV
ΔV_o	Load regulation	V_o = 5V; I_o = 0.2A to 0.5A			50	mV
V_d	Dropout voltage between Pin 19 and Pin 23	I_o = 0.5A, V_o = 5V			0.5	V
		I_o = 1A, V_o = 5V			1	V
I_{Lim}	Current limit		1.2			A

Table 5. Electrical characteristics (continued) (T_{amb} = 25°C, V_{DD} = 14.4V)

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
h	Efficiency	f = 260kHz; I_o = 0.5A f = 400kHz; I_o = 0.5A		90 86		% %
SVR	Supply voltage ripple rejection	ΔV_i = 1Vrms; f_{ripple} = 300Hz; I_o = 0.4A		50		dB
Oscillator						
f_1	Switching frequency		240	260	280	kHz
f_2	Switching frequency		375	400	425	kHz
$\frac{\Delta f}{\Delta V_i}$	Voltage stability of switching frequency	V_{DD} = 8 to 18V		Tbd		%
$\frac{\Delta f}{\Delta T_j}$	Temperature stability of switching frequency	T_j = -40°C to 85°C		Tbd		%
Sync						
V_{IL}	Low input voltage				0.8	V
V_{IH}	High input voltage		2			V
V_{OL}	Low output voltage				0.4	V
V_{OH}	High output voltage	I_{SOURCE}=1.5mA	4			V
I_{SLAVE}	Slave sink current			100		µA
T_W	Output pulse width			300		ns
REG1 - 3.3V/5V STBY linear voltage regulator						
V_{STBY}	Output voltage	no load; ADJ pin = open no load; ADJ pin = VSTBY pin	4.9 3.20	5 3.3	5.1 3.4	V V
ΔV_{line}	Line regulation	no load; 7 < Vdd < 26V		5	50	mV
ΔV_{load}	Load regulation	5mA < I_o < 250mA		12	80	mV
$V_{dropout}$	V_{STCAP} - V_{STBY}	I_o = 100mA, V_o = 5V I_o = 100mA, V_o = 3.3V		0.36 0.47	0.5 0.65	V
I_{lim}	Current limit	Out short to GND	300			mA
SVR	Supply voltage rejection	ΔV_{DD} = 1Vrms: f = 300Hz I_o = 250mA		55		dB
REG2 - Linear voltage regulator 1.5V to 3.3V						
V_{LR}	Linear regulator output voltage	no load; 4.75 ≤ V_{IN} ≤ 16V; 1+ (R5/R6) = 2.588	3.2	3.3	3.4	V
		no load; 3.135 ≤ V_{IN} ≤ 16V; 1+ (R5/R6) = 1.176	1.45	1.5	1.55	

Table 5. Electrical characteristics (continued) (T_{amb} = 25°C, V_{DD} = 14.4V)

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
V_{IN}	Input voltage	I_O = 150mA 1.5V ≤ V_{LR} ≤ 2V	3.135		16	V
		I_O = 300mA 1.5V ≤ V_{LR} ≤ 3.3V	4.75		16	V
ΔV_{load}	Load regulation	5mA ≤ I_O ≤ 300mA 4.75V ≤ V_{IN} ≤ 16V; 1.5V ≤ V_{LR} ≤ 3.3V		12		mV
ΔV_{line}	Line regulation	no load; 4.75V ≤ V_{IN} ≤ 16V; 1.5V ≤ V_{LR} ≤ 3.3V		1		mV
$V_{ref,REG2}$	Voltage reference			1.275		V
I_{Lim}	Current limit	Out short to ground	400			mA
SVR	Supply voltage rejection	V_{IN} = 5Vdc, 0.5Vacpp, 300Hz I_O = 300mA; 1.5V ≤ V_{LR} ≤ 3.3V		55		dB
		V_{IN} = 3.3Vdc, 0.5Vacpp, 300Hz I_O = 150mA; 1.5V ≤ V_{LR} ≤ 2V		55		dB
HSD1						
$V_{sat, peak}$	Saturation voltage	I_O = 0.5A			350	mV
I_{lim}	Current limit		600			mA
L_{load}	Load inductance				100	mH
HSD2						
$V_{sat, peak}$	Saturation voltage	I_O = 0.2A			300	mV
I_{lim}	Current limit		300			mA
L_{load}	Load inductance				100	mH
Voltage warning						
V_{st}	Sense low threshold		1.245	1.275	1.305	V
V_{sth}	Sense threshold hysteresis		35	45	60	mV
V_{SL}	Sense output low voltage	I_o = 1mA			0.4	V
I_{SH}	Sense output leakage	V_W = 5V; V_{SI} ≥ 1.5V			10	µA
I_{SI}	Sense input current	V_{SI}=5V		1		µA
Reset						
V_{RT}	Reset threshold voltage			0.95 x V_{STBY}		V
V_{RTH}	Reset threshold hysteresis			0.02 x V_{STBY}		V
V_{RL}	Reset output voltage	I_o = 1mA			0.4	V

Table 5. Electrical characteristics (continued) (T_{amb} = 25°C, V_{DD} = 14.4V)

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
I_{RH}	Reset output leakage	$V_{RT} = V_{STBY}$			10	µA
V_{CTth}	Delay comparator threshold			0.5 x V_{STBY}		
V_{CThy}	Delay comparator threshold hysteresis			180		mV
I_{CT1}	Timing capacitor output source current			7.5		µA
R_{CT2}	Timing capacitor output pull-down equivalent resistor			150		Ω

Table 6. Diagnostic parameters

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
HSD1W1	High side driver 1 overcurrent warning activation			1		A
HSD1W2	High side driver 1 open load warning activation	HSD1 output voltage in test mode		3		V
HSD1W2 TEST	High side driver 1 v_{dd} short warning activation in test mode	HSD1 in test mode measure $V_{VDD-LIN}$-V_{HSD1}	1	1.5	2	V
HSD2W1	High side driver 2 overcurrent warning activation			0.5		A
HSD2W2	High side driver 2 open load warning activation	HSD2 output voltage in test mode		3		V
HSD2W3	High side driver 2 v_{dd} short warning activation in test mode	HSD2 in test mode measure $V_{VDD-LIN}$-V_{HSD1}	1	1.5	2	V
THW	Thermal warning activation			145		°C
IRQ - Interrupt request pin						
IRQ-L	IRQ low voltage	I_o = 1mA			0.4	V
IRQ-H	IRQ leakage	V_{irq} = 5V			1	µA

Table 7. SPI interface

Symbol	Alt	Parameter	Test conditions	Min.	Max.	Unit
Recommended DC operating voltage						
V_{SPI}		Supply voltage for SPI I/O		3	5.5	V
Input parameters (Tamb = 25°C, f = 1MHz)						
C_{IN}		Input capacitance (D)			8	pF
C_{IN}		Input capacitance (others pins)			6	pF
t_{LPF}		Input signal pulse width			10	ns

Table 7. SPI interface (continued)

Symbol	Alt	Parameter	Test conditions	Min.	Max.	Unit
DC characteristics (T_{amb} = -40 to 85°C, V_{SPI} = 3V to 5.5V)						
I_{LI}		Input leakage current			5	µA
I_{LO}		Output leakage current			±2	µA
V_{IL}		Input low voltage		-0.3	$0.3V_{SPI}$	V
V_{IH}		Input high voltage		$0.7V_{SPI}$	V_{SPI}+1	V
V_{OL}		Output low voltage	I_{OL} = 2mA		$0.2V_{SPI}$	V
V_{OH}		Output high voltage	I_{OH} = -2mA	$0.8V_{SPI}$		V
AC characteristics (Tamb = -40 to 85°C, V_{SPI} = 3V to 5.5V						
t_{SCLH}	t_{SU}	$\overline{S}$ setup time		50		ns
t_{CLSH}	t_{SH}	$\overline{S}$ hold time		50		ns
t_{CH}	t_{WH}	Clock high time		200		ns
t_{CL}	t_{WL}	Clock low time		300		ns
t_{CLCH}	t_{RC}	Clock rise time			1	µs
t_{CHCL}	t_{FC}	Clock fall time			1	µs
t_{DVCH}	t_{DSU}	Data In setup time		50		ns
t_{CHDX}	t_{DH}	Data In hold time		50		ns
t_{DLDH}	t_{RI}	Data In rise time			1	µs
t_{DHDL}	t_{FI}	Data in fall time			1	µs
t_{SHSL}	t_{CS}	$\overline{S}$ deselect time	$4.5V < V_{SPI} < 5.5V$ $3V < V_{SPI} < 4.5V$	200 250		ns ns
t_{SHQZ}	t_{DIS}	Output disable time			150	ns
t_{QVCL}	t_V	Clock low to output valid			250	ns
t_{CLQX}	t_{HO}	Output hold time		0		ns
t_{QLQH}	t_{RO}	Output rise time			100	ns
t_{QHQL}	t_{FO}	Output fall time			100	ns

Figure 3. AC testing input output waveforms

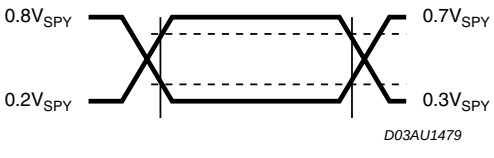


Figure 4. SPI clocking scheme

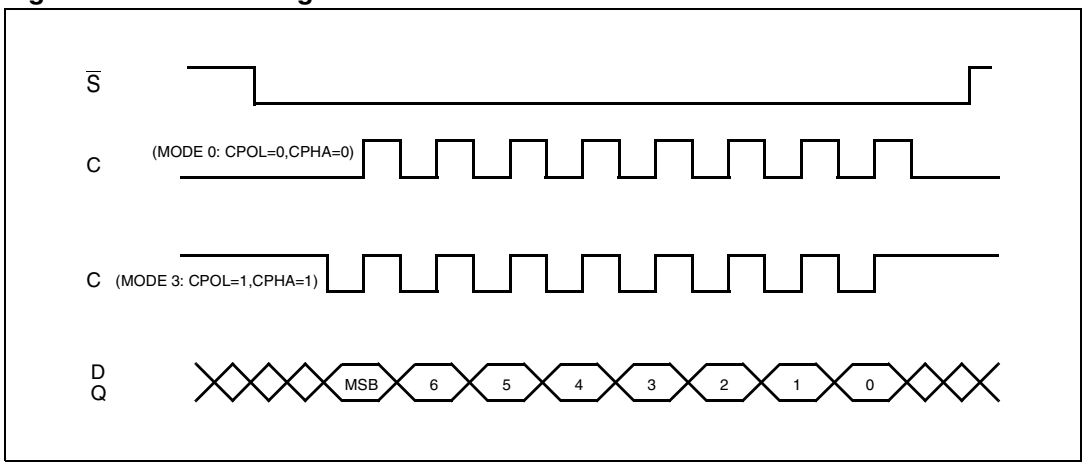


Figure 5. Output timing

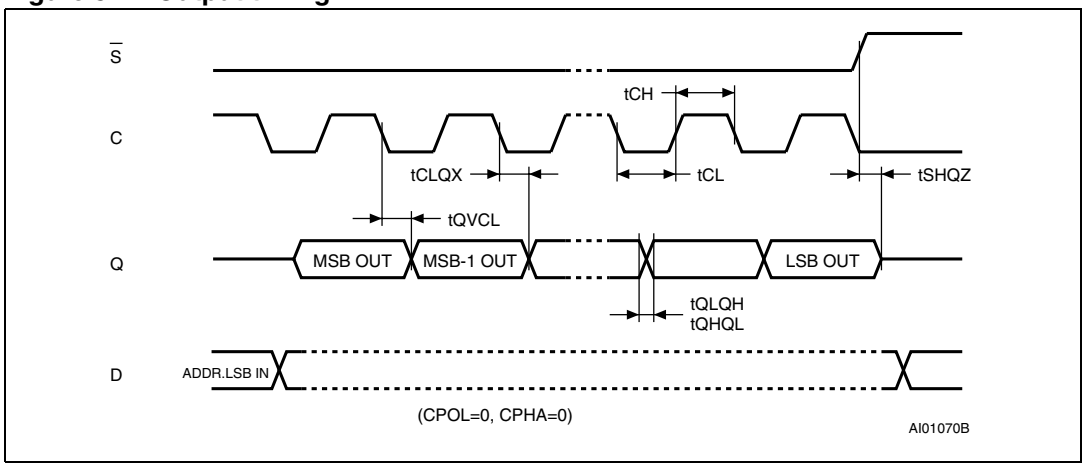
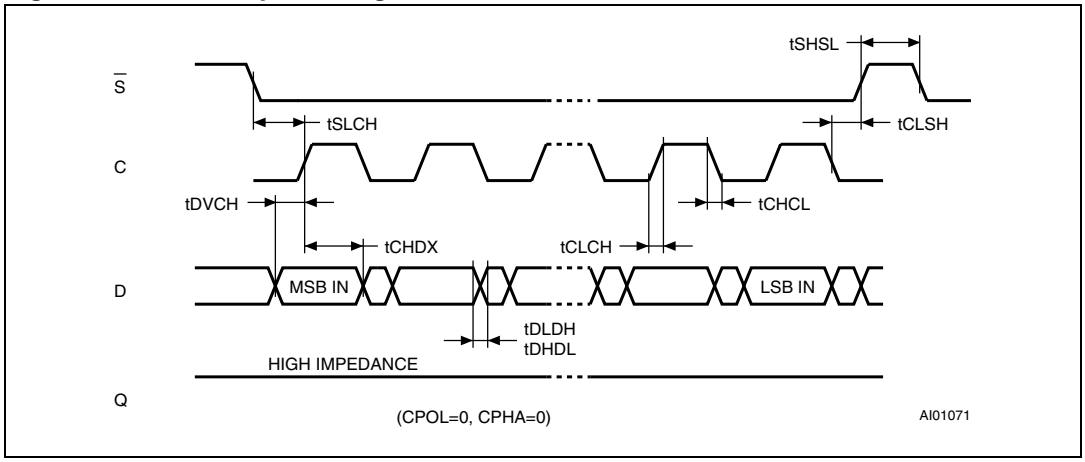


Figure 6. Serial input timing



2 Functional description

2.1 REG1 stand-by regulator

The stand-by regulator (*Figure 7.*) output voltage can be 5V or 3.3V. It is externally selectable by means of the ADJ pin:

- leaving the ADJ pin open, the output voltage is 5V;

- connecting the ADJ pin to the Vstby pin the output voltage becomes 3.3V.

This regulator is supplied by STCAP pin and provide the reset information.

It has a current protection which limits the maximum allowable output current.

2.2 Reset

The $\overline{\text{RES}}$ pin (*Figure 8.*) is an open collector that is activated (that is forced to zero) when the stand-by regulator is not in regulation (including thermal shutdown and faults). The indication that REG1 is in regulation is delayed by a time set up by the external capacitor CT.

When the $\overline{\text{RES}}$ is switched on, HSD1, HSD2, REG2, PWM are turned off and until the $\overline{\text{RES}}$ is forced to zero only the REG1 and low Voltage Warnings are active.

2.3 Low voltage warning

This circuit is able to sense two different voltages through external resistors to increase the overall flexibility. (*Figure 9.*)

If S1 pin voltage is higher than Vst, the output of mos M1 is off: $\overline{\text{W1}}$ is floating and can be pulled up by an external resistor. If S1 pin voltage goes down and becomes lower than Vst, the mos M1 is turned on and forces $\overline{\text{W1}}$ to zero. The same thing happens for S2 - $\overline{\text{W2}}$.

The outputs $\overline{\text{W1}}$ and $\overline{\text{W2}}$ can be connected together to get a single output.

2.4 REG2 linear voltage regulator

REG2 is a linear voltage regulator (*Figure 7.*) with a dedicated supply pin VIN. The output voltage (between 1.5V and 3.3V) is fixed by an external divider. It can be turned on/off by SPI. It has a current protection which limits the maximum allowable output current.

2.5 High side drivers

Two high-side driver (*Figure 10.*) with charge pump controlled by SPI are available inside L5953. They are protected against short to ground: the short circuit protection limits the maximum output current.

A diagnostic procedure is available to detect open load, short to battery and overcurrent.

Open load and short to battery can be reveal only in test mode while overcurrent is active only during normal operation of the device. (see *4.2 on page 18*)

2.6 PWM step down voltage regulator

The switching regulator (*Figure 11.*) inside the L5953 is a voltage control mode (also known as a direct duty cycle) Buck regulator: the error signal coming from the error amplifier is compared with a sawtooth to set on and off times of the power switch.

The feedforward control is introduced to get a quickly response to input voltage changes: the sawtooth has a fixed frequency and an amplitude variable with the battery voltage.

Continuous mode operation is recommended in order to reduce the stress of the output capacitor and of the free-wheeling diode.

2.6.1 Error amplifier and compensation network

The error amplifier (EA) is a voltage amplifier whose non-inverting input is fixed to the reference voltage (1.275V bandgap voltage) and whose inverting input and output are externally available for feedback and frequency compensation.

3 Internal pin connections

Figure 7. Linear regulators

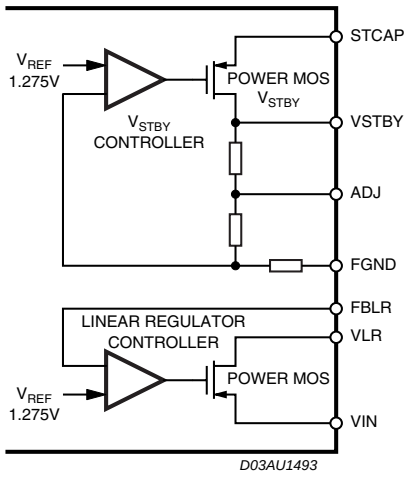


Figure 8. Reset

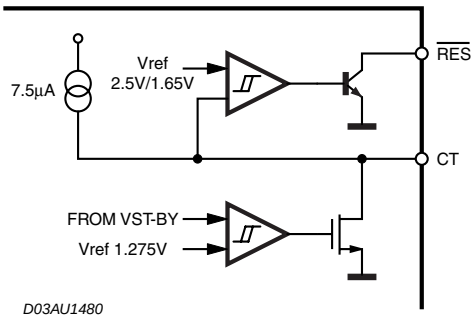


Figure 9. Low voltage warning block diagram.

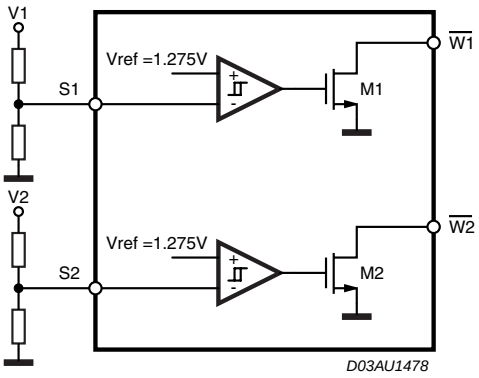


Figure 10. HSD

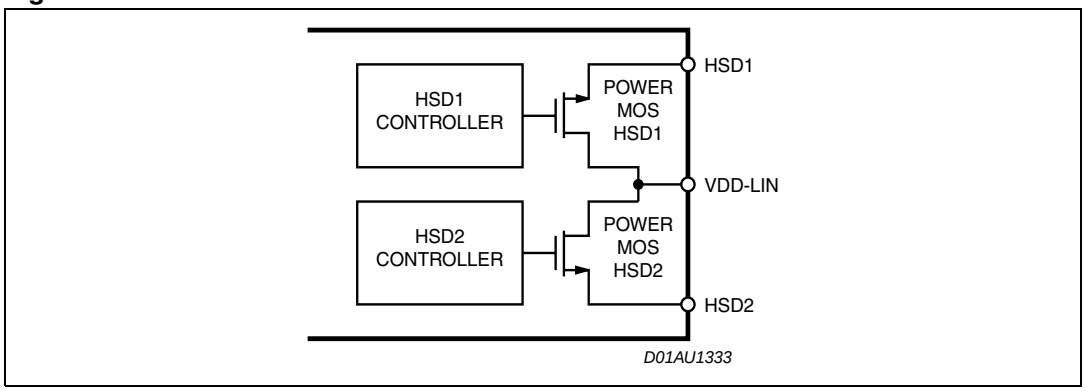


Figure 11. PWM

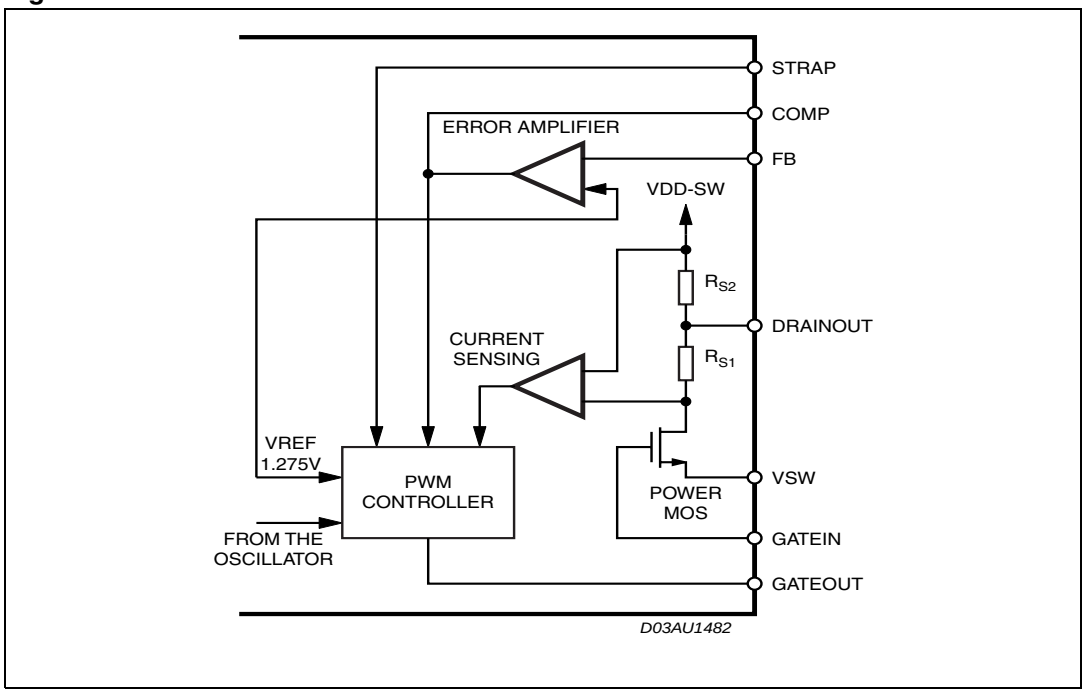
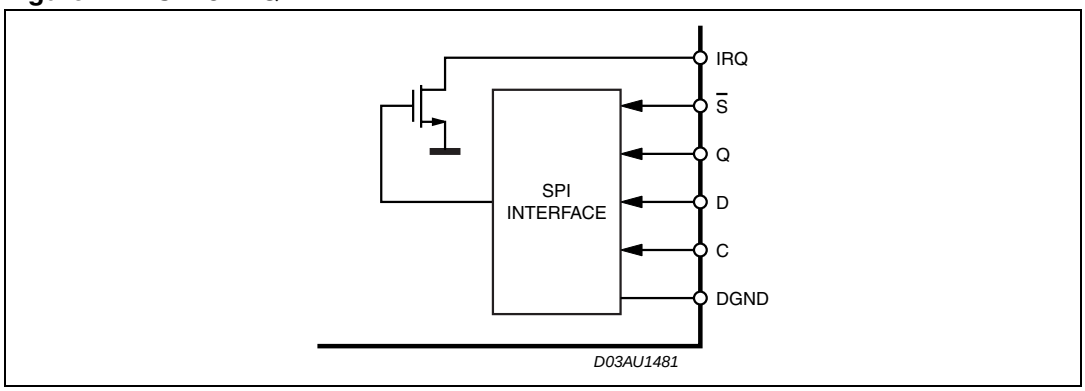


Figure 12. SPI & IRQ



4 SPI interface

4.1 Signals description

The SPI interface available inside L5953 is able to work both in Mode 0 and Mode 3.

Serial output (Q). The output pin is used to transfer data serially out of the L5953. Data is shifted out on the falling edge of the serial clock.

Serial input (D). The input pin is used to transfer data serially into the device. It receives instructions, addresses, and data to be written. Input is latched on the rising edge of the serial clock.

Serial clock (C). The serial clock provides the timing of the serial interface. Instructions, addresses, or data present at the input pin are latched on the rising edge of the clock input, while data on the Q pin changes after the falling edge of the clock input.

Chip select ($\overline{S}$). This input is used to select the L5953. The chip is selected by a high to low transition on the $\overline{S}$ pin. At any time, the chip is deselected by a low to high transition on the $\overline{S}$ pin. As soon as the chip is deselected, the Q pin is at high impedance state. The pin allows multiple L5953 to share the same SPI bus. After power up, the chip is at the deselect state.

SPI Input/Output are supplied by an external supply voltage VSPI while the core is supplied by the stand-by regulator VSTBY. The SPI is reset by an internal signal whose buffered version is $\overline{RES}$. (See *Figure 12.*)

4.2 Operations

All instructions, addresses and data are shifted in and out of the chip MSB first. Data input (D) is sampled on the first rising edge of clock (C) after the chip select ($\overline{S}$) goes low. Prior to any operation, a one-byte instruction code must be entered in the chip. This code is entered in the chip. This code is entered via the data input (D), and latched on the rising edge of the clock input (C). To enter an instruction code, the product must have been previously selected ($\overline{S}$ = low). Table 1 shows the instruction set and format for device operation. An invalid instruction (one not contained in table 1) leaves the chip as previously selected.

4.3 Write enable (WREN and write disable (WRDI))

The L5953 contains a write enable latch. This latch must be set prior to every WRITE operation. The WREN instruction will set the latch and the WRDI instruction will reset the latch. The latch is reset under all the following conditions:

- – Power on
- – WRDI instruction executed

As soon as the WREN or WRDI instruction is received by the L5953, the circuit executes the instruction and enters a wait mode until it is deselected.

Table 8. Instruction set

Instruction	Description	Instruction Format
WREN	Set write enable latch	00000110
WRDI	Reset write enable latch	00000100
WSTA	Write status register	00000010
RDIA	Read diagnostic register	00000101
RSTA	Read status register	00000011

Table 9. Status register

s15	s14	s13	s12	s11	s10	s9	s8	s7	s6	s5	s4	s3	s2	s1	s0
REG 2	HSD 1	HSD 2	TBD	TBD	PWM freq.	PWM	TBD	TBD	TBD	TBD	TBD	TBD	TBD	Test mode	START DIAG

Table 10. Status register description

		0	1
s15	REG2 linear voltage regulator 1.5 to 3.3V	Regulator off	Regulator on
s14	High side driver 1	HSD1 off	HSD1 on
s13	High side driver 2	HSD2 off	HSD2 on
s12	TBD		
s11	TBD		
s10	PWM switching frequency	260kHz	400kHz
s9	PWM voltage regulator	PWM1 off	PWM1 on
s8	TBD		
s7	TBD		
s6	TBD		
s5	TBD		
s4	TBD		
s3	TBD		
s2	TBD		
s1	Test mode	Test mode off	Test mode on (1)
s0	Diagnostic	Diagnostic off	Starts the diagnostic procedure: - in test mode if s1=1; - during normal operation if s1=0 If s1=0 and s0=1, must be s14 = 1 (HSD1 ON) and s13=1 (HSD2 ON)

1. In this case the bits s15 - s2 are internally set to 0 (regulators and high side drivers are in off condition)

Table 11. Diagnostic register

d7	d6	d5	d4	d3	d2	d1	d0
Test mode	HSD1W1	HSD1W2	HSD1W3	HSD2W1	HSD2W2	HSD2W3	THW

Table 12. Diagnostic register description

		0	1
d7	Test mode	The diagnostic register is referred to a test performed during the normal working of the L5953	The diagnostic register is referred to a test performed in Test mode
d6	HSD1W1	If d7=0: HSD1 in normal condition; If d7=1: bit value meaningless	If d7=0: HSD1 is in overcurrent If d7=1: bit value meaningless
d5	HSD1W2	If d7=0: bit value meaningless; If d7=1: HSD1 in normal condition	If d7=0: bit value meaningless If d7=1: an open load is present on HSD1
d4	HSD1W3	If d7=0: bit value meaningless; If d7=1: HSD1 in normal condition	If d7=0: bit value meaningless If d7=1: HSD1 is shorted to the supply voltage VDD
d3	HSD2W1	If d7=0: HSD1 in normal condition; If d7=1: bit value meaningless	If d7=0: HSD2 is in overcurrent; If d7=1: bit value meaningless
d2	HSD2W2	If d7=0: bit value meaningless If d7=1: HSD2 in normal condition	If d7=0: bit value meaningless If d7=1: an open load is present on HSD2
d1	HSD1W3	If d7=0: bit value meaningless If d7=1: HSD2 in normal condition;	If d7=0: bit value meaningless If d7=1: HSD1 is shorted to the supply voltage VDD
d0	Thermal warning	Normal condition	Over temperature protection activated(Tj>150°C)

5 Summary of the main operations

5.1 Operation A

- Test mode diagnostic procedure start
- 1) WREN instruction (*Figure 13.*)
- 2) WSTA instruction (*Figure 14.*)

5.2 Operation B

- Read the diagnostic register
  Case1: after a test mode diagnostic procedure start
  1) RDIA instruction (*Figure 15.*)
  2) Diagnostic register output (*Figure 15.*)

Note: An operation B must follow an operation A. The delay between the end of the operations A to the start of the operations B must be longer than 100µS

5.3 Operation C

- Write the status register
  1) WREN instruction (*Figure 13.*)
  2) WSTA instruction (*Figure 18.*)

5.4 Operation D

- Read the status register
  1) RSTA instruction (*Figure 19.*)
  2) Status Register output (*Figure 19.*)

5.5 Operation E

- Diagnostic procedure start
  1) WREN instruction (*Figure 13.*)
  2) WSTA instruction (*Figure 16.*)

5.6 Operation F

- Read the diagnostic register
  Case 2: after a diagnostic procedure start
  1) RDIA instruction (*Figure 17.*)
  2) Diagnostic register output (*Figure 17.*)
  An operation F must follow an operation E, if the IRQ pin is not activated. The delay between Operation E and Operation F must be longer than 100µs. To be recognized, the fault must be present without interruptions, during all the delays mentioned. After an Operation F, the bit s0 of the status register is reset (0)

5.7 Operation G

- Write operation disabled
  1) WRDI instruction (*Table 8.*)

5.8 Operation H

- Read the diagnostic register case 3: after an IRQ pin activation
  1) RDIA instruction (*Figure 17.*)
  2) Diagnostic register output (*Figure 17.*)
  The delay between the IRQ activation and operation F must be longer than 100µs

Figure 13. Write enable latch sequence

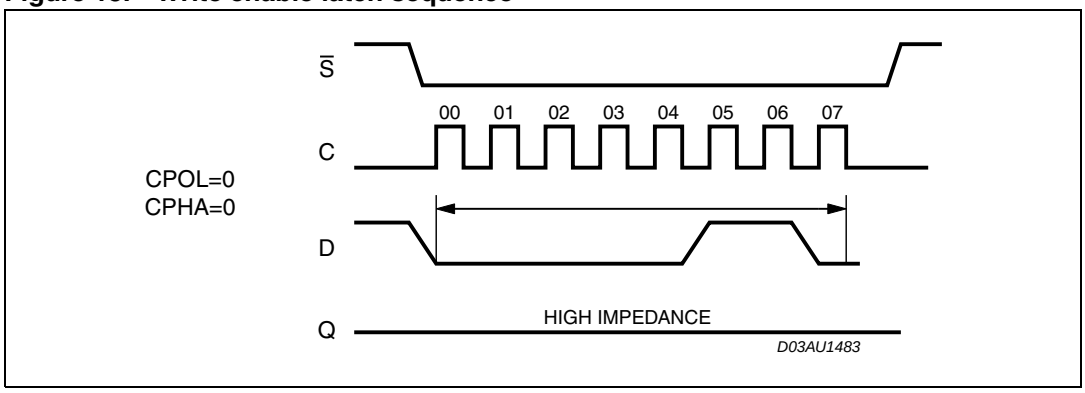


Figure 14. Test mode diagnostic procedure start (after a write enable latch sequence)

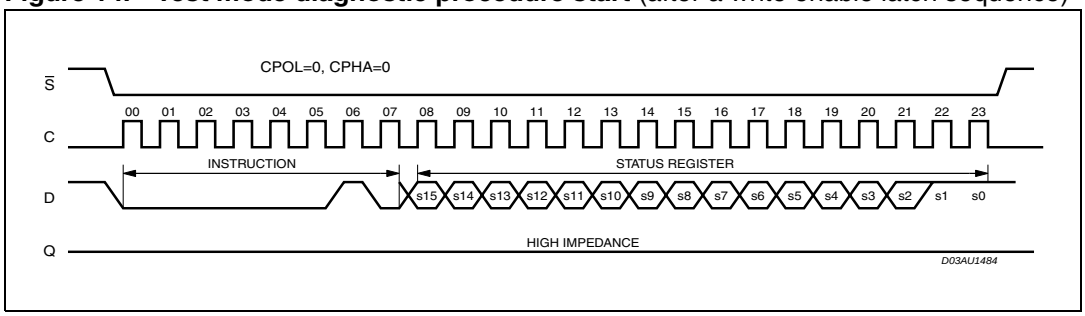


Figure 15. Read the diagnostic registerCase1: (after a test mode diagnostic procedure start**)**

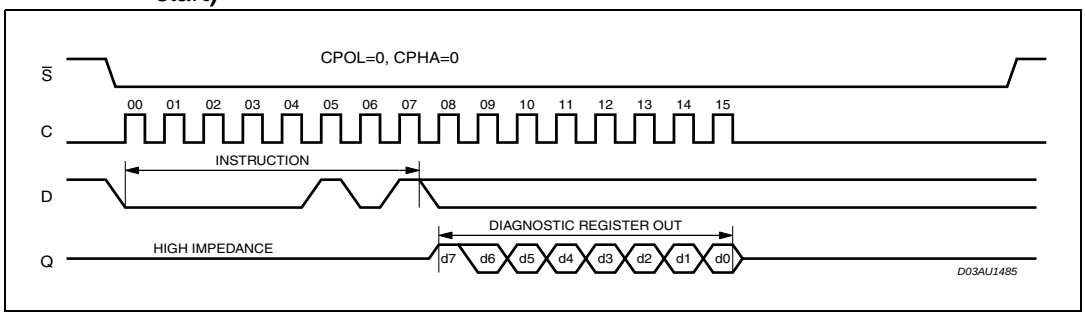


Figure 16. Diagnostic procedure start (after write enable latch sequence operation A)

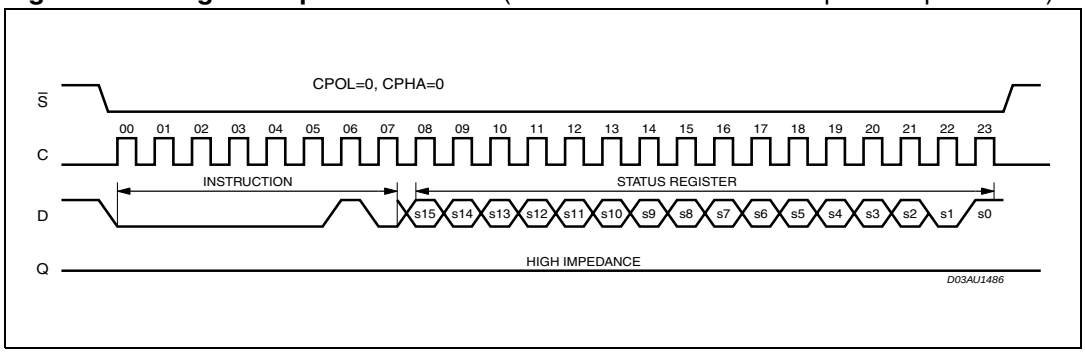


Figure 17. Read the diagnostic RegisterCase2: during the normal working of the L5953 (after a diagnostic procedure start, see *Figure 16*)

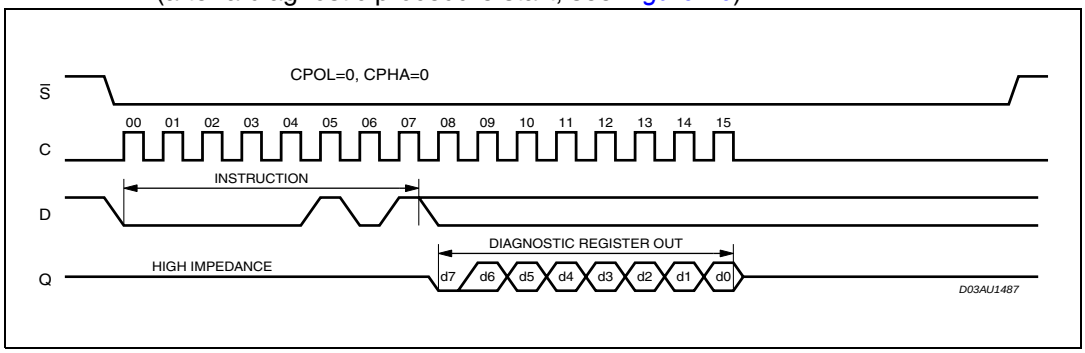


Figure 18. Write the status register (after a write enable latch sequence operation A**)**

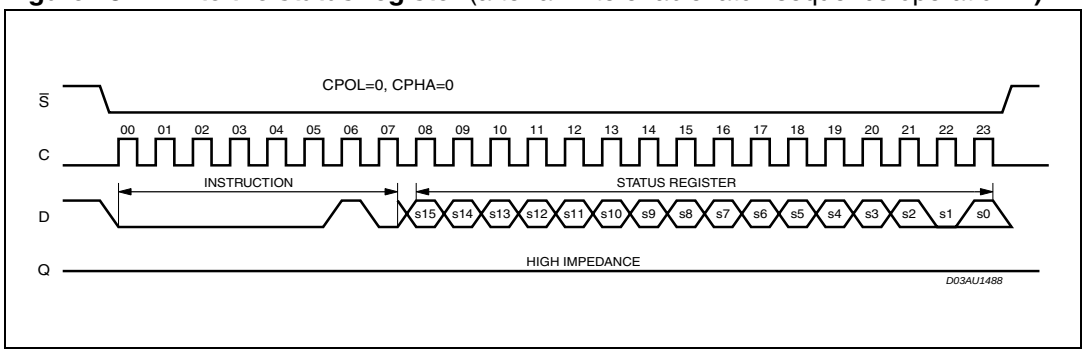
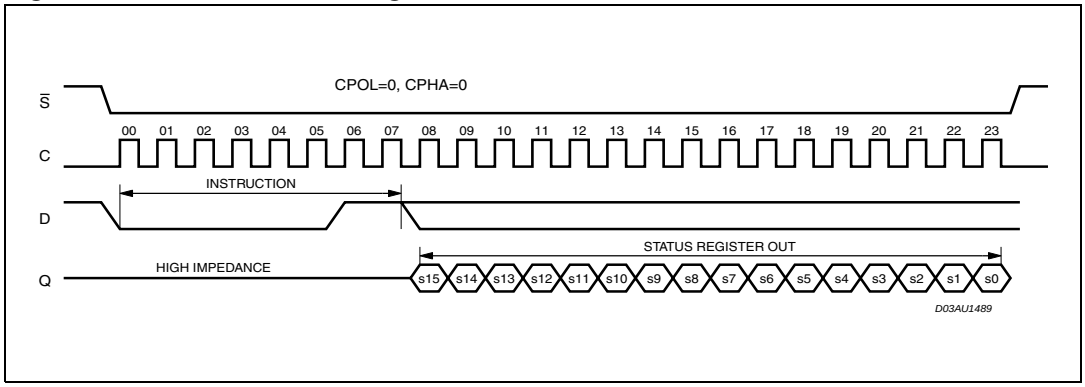


Figure 19. Read the status register



5.9 IRQ - Interrupt request pin

- It is an open drain pin activated (low) every time a variation occurs in the diagnostic register.
- Purpose: to alert the μP that one or more warning bit of the diagnostic register has changed from 0 to 1 or from 1 to 0.
- An activation of this pin puts the bit s0 of the status register to 1 (start diagnostic) like an operation e (diagnostic procedure start). Then an operation F has to be executed without an operation E before.
- After an operation F, the IRQ pin is deactivated, and goes to 1 if connected to a pull-up resistor.

6 Application note

Figure 20. Block and application diagram

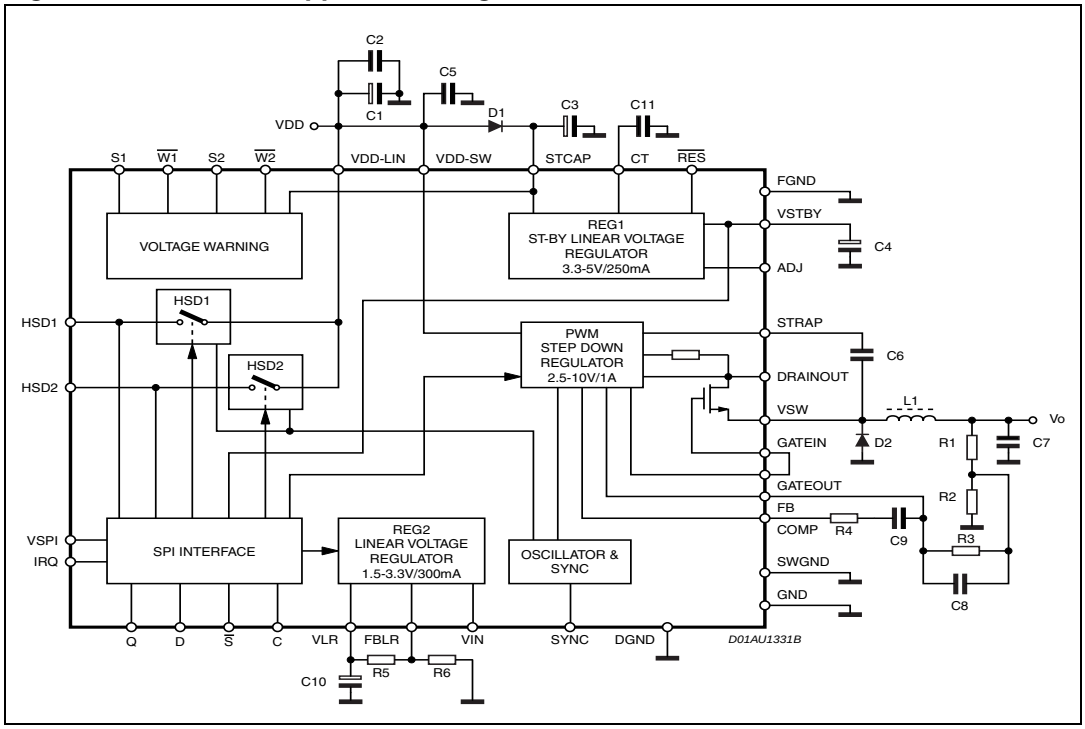
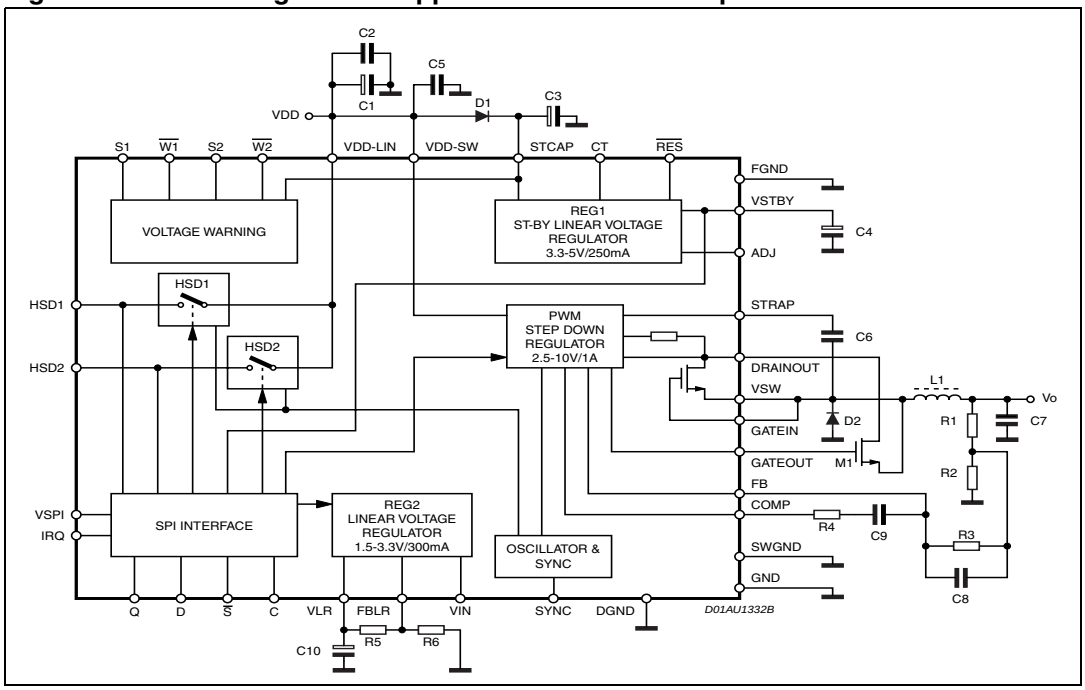


Figure 21. Block diagram and application with external power MOS



Part list on evaluation board

C1 = 470 µF	C2 = 220 nF	C3 = 470 µF	C4 = 10 µF	C5 = 1 µF	C6 = 100 nF
C7 = 470 µF ESR=65 mΩ	C8 = 56nF	C9 = 2.7 nF	C10 = 10 µF	C11 = 4.7 nF	
R1 = 2.2 kΩ	R2 = 2 x 1.5 kΩ in parallel	R3 = 10 kΩ	R4 = 220 kΩ	R5 = 3.3 kΩ	R6 = 1 kΩ
L1 = 180 µH		D1 = 1N4007 or MBR160	D2 = MBR360		

6.1 REG1 output voltage

V_{STBY} = 5V if pin ADJ left floating
V_{STBY} = 3.3V if pin ADJ is connected to the pin V_{STBY}
Timing capacitor

The value for this capacitor has to be chosen according the wanted power-on delay T_d:

$$C11 = \frac{I_{CT1} \cdot T_d}{(0.5 \cdot V_{STBY}) + V_{CTLHy}}$$

where I_{CT1} is the source current used to charge the timing capacitor and V_{STBY} is the REG1 output voltage.

6.2 Feedback resistors for REG2

$$R5 = R6 \cdot \left(\frac{V_{LR}}{V_{ref,\,REG2}} - 1 \right)$$

where VLR is the required output voltage for REG2.

6.3 External components for PWM regulator

6.3.1 Bootstrap capacitor

The suggested value for the bootstrap capacitor is C6 = 100nF

Here following you find the criteria for the selection of the inductor L1, the free-wheeling diode D2, the output filter capacitor C7, the feedback resistor R1, R2 and the compensation network R3, C8, R4, C9 to have a Buck regulator working in continuous mode. Continuous mode operation is recommended in order to reduce the stress of the output capacitor and of the free-wheeling diode.

6.3.2 Inductor selection

The minimum value of the inductor L7 has to be so that the maximum inductor current ripple $\Delta I_{L,max}$ is 20% to 30% of the maximum load current load $I_{o,max}$.The maximum ripple is present when the switching frequency is minimum ($f_{sw,min}$) and the input voltage is maximum ($V_{in,max}$) so the minimum value for the inductor L_{min} is:

$$L_{min} = \frac{V_O}{\Delta I_{L,max}} \cdot \left[1 - \frac{V_O}{V_{i,max}}\right] \cdot \frac{1}{f_{sw,min}}$$

6.3.3 Output capacitor selection

The criteria for the selection of the capacitor C7 is based on the output voltage ripple requirements. The ripple on the output voltage is due to a capacitive contribute, often negligible, equal to

$$\Delta V_c = \frac{\Delta I_{L,max}}{8 \cdot C7 \cdot f_{sw,min}}$$

and a resistive contribute given by the ESR of the capacitor and which is equal to

$$\Delta V_{ESR} = ESR \cdot \Delta I_{L,max}$$

ΔVC fixes the value for C7 while ΔVESR limits the ESR of the capacitor.Usually the capacitor is chosen so that the total ripple on the output regulated voltage Vo is equal to 1% of the value of Vo. If V_{ripple} is the maximum allowed voltage ripple on Vo then it should result:

$$V_{ripple} \geq \sqrt{\Delta V_c^{\,2} + \Delta V_{ESR}^{\,2}}$$

More often the minimum value of C7 is imposed by other considerations such as to get a good dynamic behavior of the output voltage in case of large load variations.

6.4 Free-wheeling diode

The diode must withstand an average current Id equal to Id = I_{lim} (1- D_{min}) where I_{lim} is the current of intervention of the short circuit protection and D_{min} is the minimum duty cycle. As D_{min} is very low, the current Id can be assumed equal to I_{lim}.

6.5 Compensation network

In continuous mode, the voltage controlled buck converter shows two poles due to the output LC filter and one zero due to the ESR of the output capacitor. The suggested compensation network introduces two zeros and two poles:

- the zeros compensate the double poles of the LC filter
- one pole compensates the zero due to ESR of the output capacitor

the second pole is nominally located in the origin which means an infinite gain at frequency null. In the reality the DC value of the closed loop gain can not be greater than the DC value of the EA open loop gain and the pole is located at very low frequency.

The values for the components of the compensation network can be fixed when the inductor L1 and the output capacitor C7 are chosen. The necessary steps are:

1. Fix the cross-over frequency f_C of the overall loop gain. Usually:

$$f_c = 0.1 \cdot f_{sw,min}$$

where $f_{sw,min}$ is the minimum switching frequency

2. Calculate the high frequency error amplifier gain

$$G_c = 0.25 \cdot f_c \cdot 2 \cdot \pi \cdot \frac{L1}{ESR}$$

3. Chose R3 and calculate

$$C8 = 2 \cdot \frac{\sqrt{L1 \cdot C7}}{R3}$$

The value for R3 has not to be very high (for example 10KΩ) so to limit the error due to an error amplifier input offset current.

4. Calculate

$$R_p = \frac{R3}{\left(\frac{2}{ESR} \cdot \sqrt{\frac{L1}{C7}}\right) - 1}$$

$$R1 = R_p \cdot \frac{V_O}{V_{ref,\,PWM}}$$

$$R2 = \frac{R_p}{1 - \frac{V_{ref,PWM}}{V_O}}$$

5. Finally calculate

$$R4 = G_C \cdot R1$$

and

$$C9 = 2 \cdot \frac{\sqrt{L1 \cdot C7}}{R4}$$

7 Package information

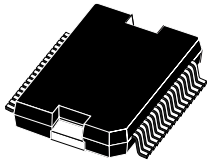
In order to meet environmental requirements, ST offers these devices in ECOPACK® packages. These packages have a lead-free second level interconnect. The category of second level interconnect is marked on the package and on the inner box label, in compliance with JEDEC standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an ST trademark. ECOPACK specifications are available at: www.st.com.

Figure 22. PowerSO36 mechanical data and package dimensions

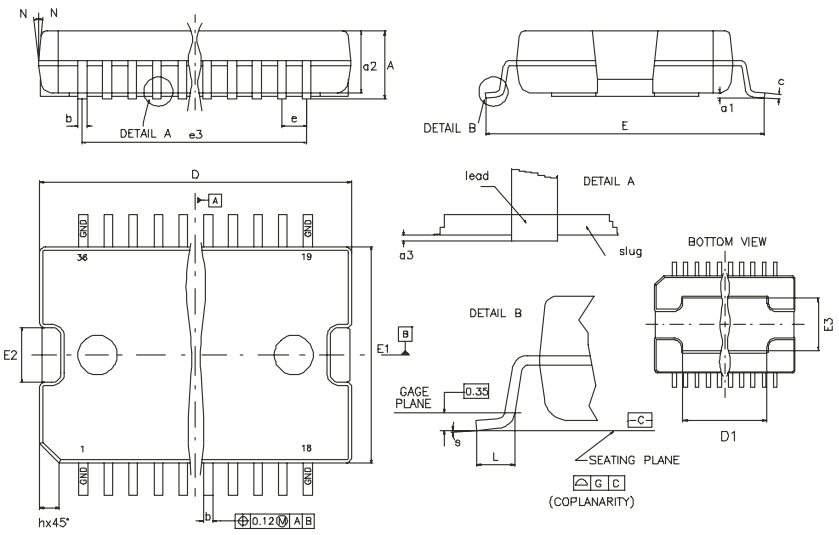
DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A			3.60			0.1417
a1	0.10		0.30	0.0039		0.0118
a2			3.30			0.1299
a3	0		0.10			0.0039
b	0.22		0.38	0.0087		0.0150
c	0.23		0.32	0.0091		0.0126
D	15.80		16.00	0.6220		0.6299
D1	9.40		9.80	0.3701		0.3858
E	13.90		14.5	0.5472		0.5709
E1	10.90		11.10	0.4291		0.4370
E2			2.90			0.1142
E3	5.80		6.20	0.2283		0.2441
e		0.65			0.0256	
e3		11.05			0.4350	
G	0		0.10			0.0039
H	15.50		15.90	0.6102		0.6260
h			1.10			0.0433
L	0.8		1.10	0.0315		0.0433
N	10˚ (max)					
s	8˚ (max)					

Note: “D and E1” do not include mold flash or protusions.
- Mold flash or protusions shall not exceed 0.15mm (0.006”)
- Critical dimensions are "a3", "E" and "G".

OUTLINE AND MECHANICAL DATA



PowerSO-36



8 Revision history

Table 13. Document revision history

Date	Revision	Changes
25-Mar-2003	1	Initial release.
04-Sep-2007	2	Layout changes and text mofifications.

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