

## 4-Mbit (256K x 16) Pseudo Static RAM

### Features

- **Wide voltage range: 2.70V–3.30V**
- **Access time: 55 ns, 60 ns and 70 ns**
- **Ultra-low active power**
  - Typical active current: 1 mA @ f = 1 MHz
  - Typical active current: 8 mA @ f = f<sub>max</sub> (70-ns speed)
- **Ultra low standby power**
- **Automatic power-down when deselected**
- **CMOS for optimum speed/power**
- **Offered in a 48-ball BGA package**

### Functional Description<sup>[1]</sup>

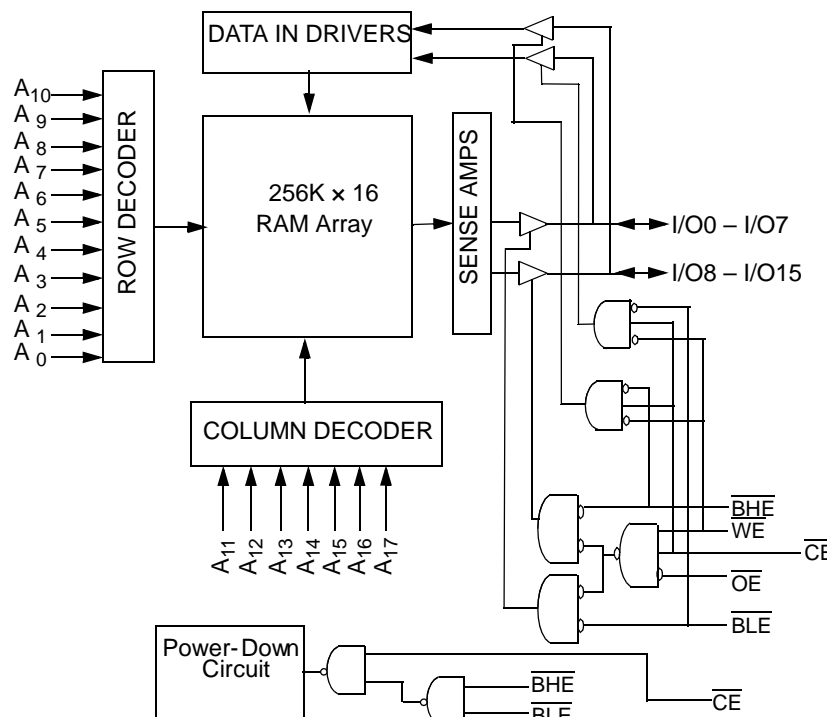
The CYK256K16MCCB is a high-performance CMOS Pseudo static RAM organized as 256K words by 16 bits that supports an asynchronous memory interface. This device features advanced circuit design to provide ultra-low active current. This is ideal for providing More Battery Life™ (MoBL®) in portable applications such as cellular telephones. The device

can be put into standby mode when deselected ( $\overline{\text{CE}}$  HIGH or both  $\overline{\text{BHE}}$  and  $\overline{\text{BLE}}$  are HIGH). The input/output pins ( $\text{I/O}_0$  through  $\text{I/O}_{15}$ ) are placed in a high-impedance state when: deselected ( $\overline{\text{CE}}$  HIGH), outputs are disabled ( $\overline{\text{OE}}$  HIGH), both Byte High Enable and Byte Low Enable are disabled ( $\overline{\text{BHE}}$ ,  $\overline{\text{BLE}}$  HIGH), or during a write operation ( $\overline{\text{CE}}$  LOW and  $\overline{\text{WE}}$  LOW).

Writing to the device is accomplished by taking Chip Enable ( $\overline{\text{CE}}$  LOW) and Write Enable ( $\overline{\text{WE}}$ ) input LOW. If Byte Low Enable ( $\overline{\text{BLE}}$ ) is LOW, then data from  $\text{I/O}$  pins ( $\text{I/O}_0$  through  $\text{I/O}_7$ ) is written into the location specified on the address pins ( $\text{A}_0$  through  $\text{A}_{17}$ ). If Byte High Enable ( $\overline{\text{BHE}}$ ) is LOW, then data from  $\text{I/O}$  pins ( $\text{I/O}_8$  through  $\text{I/O}_{15}$ ) is written into the location specified on the address pins ( $\text{A}_0$  through  $\text{A}_{17}$ ).

Reading from the device is accomplished by taking Chip Enable ( $\overline{\text{CE}}$  LOW) and Output Enable ( $\overline{\text{OE}}$ ) LOW while forcing the Write Enable ( $\overline{\text{WE}}$ ) HIGH. If Byte Low Enable ( $\overline{\text{BLE}}$ ) is LOW, then data from the memory location specified by the address pins will appear on  $\text{I/O}_0$  to  $\text{I/O}_7$ . If Byte High Enable ( $\overline{\text{BHE}}$ ) is LOW, then data from memory will appear on  $\text{I/O}_8$  to  $\text{I/O}_{15}$ . Refer to the truth table for a complete description of read and write modes.

### Logic Block Diagram



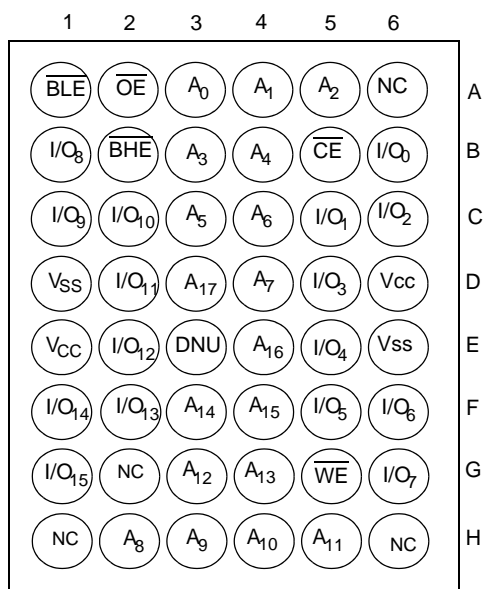
#### Note:

1. For best practice recommendations, please refer to the CY application note *System Design Guidelines* on <http://www.cypress.com>.

## Pin Configuration<sup>[2, 3, 4]</sup>

### VFBGA

#### Top View



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## Product Portfolio

Product	V <sub>CC</sub> Range (V)			Speed (ns)	Power Dissipation					
					Operating I <sub>CC</sub> (mA)				Standby I <sub>SB2</sub> (μA)	
					f = 1MHz		f = f <sub>max</sub>			
	Min.	Typ. <sup>[5]</sup>	Max.		Typ. <sup>[5]</sup>	Max.	Typ. <sup>[5]</sup>	Max.	Typ. <sup>[5]</sup>	Max.
	CYK256K16MCCB	2.70	3.0		3.30	55	1	5	14	22
60										
70						8		15		

### Notes:

- Ball H1, G2 and ball H6 for the VFBGA package can be used to upgrade to an 8-Mbit, 16-Mbit and 32-Mbit density, respectively.
- NC "no connect" – not connected internally to the die.
- DNU (Do Not Use) pins have to be left floating or tied to V<sub>ss</sub> to ensure proper application.
- Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at V<sub>CC</sub> = V<sub>CC(typ.)</sub>, T<sub>A</sub> = 25°C.

## Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ..... -65°C to + 150°C

Ambient Temperature with

Power Applied ..... -55°C to + 125°C

Supply Voltage to Ground Potential ..... -0.4V to 4.6V

DC Voltage Applied to Outputs

in High-Z State<sup>[6, 7, 8]</sup> ..... -0.4V to 3.7V

DC Input Voltage<sup>[6, 7, 8]</sup> ..... -0.4V to 3.7V

Output Current into Outputs (LOW) ..... 20 mA

Static Discharge Voltage ..... > 2001V  
(per MIL-STD-883, Method 3015)

Latch-up Current ..... > 200 mA

## Operating Range

Range	Ambient Temperature	V <sub>CC</sub>
Industrial	-25°C to +85°C	2.70V to 3.30V

## Electrical Characteristics Over the Operating Range

Parameter	Description	Test Conditions	CYK256K16MCCB -55, 60, 70			Unit
			Min.	Typ. <sup>[5]</sup>	Max.	
V <sub>CC</sub>	Supply Voltage		2.7	3.0	3.3	V
V <sub>OH</sub>	Output HIGH Voltage	I <sub>OH</sub> = -0.1 mA V <sub>CC</sub> = 2.70V	V <sub>CC</sub> - 0.4			V
V <sub>OL</sub>	Output LOW Voltage	I <sub>OL</sub> = 0.1 mA V <sub>CC</sub> = 2.70V			0.4	V
V <sub>IH</sub>	Input HIGH Voltage		0.8 * V <sub>CC</sub>		V <sub>CC</sub> + 0.4V	V
V <sub>IL</sub>	Input LOW Voltage		-0.4		0.6	V
I <sub>IX</sub>	Input Leakage Current	GND ≤ V <sub>IN</sub> ≤ V <sub>CC</sub>	-1		+1	μA
I <sub>OZ</sub>	Output Leakage Current	GND ≤ V <sub>OUT</sub> ≤ V <sub>CC</sub> , Output Disabled	-1		+1	μA
I <sub>CC</sub>	V <sub>CC</sub> Operating Supply Current	f = f <sub>MAX</sub> = 1/t <sub>RC</sub> V <sub>CC</sub> = V <sub>CCmax</sub> I <sub>OUT</sub> = 0 mA CMOS levels		14 for -55 14 for -60 8 for -70	22 for -55 22 for -60 15 for -70	mA
		f = 1 MHz		1 for all speeds	5 for all speeds	mA
I <sub>SB1</sub>	Automatic CE Power-Down Current—CMOS Inputs	CE ≥ V <sub>CC</sub> - 0.2V V <sub>IN</sub> ≥ V <sub>CC</sub> - 0.2V, V <sub>IN</sub> ≤ 0.2V f = f <sub>MAX</sub> (Address and Data Only), f = 0 (OE, WE, BHE and BLE), V <sub>CC</sub> = 3.30V	V <sub>CC</sub> = 3.3V	150	250	μA
I <sub>SB2</sub>	Automatic CE Power-Down Current—CMOS Inputs	CE ≥ V <sub>CC</sub> - 0.2V V <sub>IN</sub> ≥ V <sub>CC</sub> - 0.2V or V <sub>IN</sub> ≤ 0.2V, f = 0, V <sub>CC</sub> = 3.30V	V <sub>CC</sub> = 3.3V	17	40	μA

## Thermal Resistance<sup>[9]</sup>

Parameter	Description	Test Conditions	BGA	Unit
Θ <sub>JA</sub>	Thermal Resistance (Junction to Ambient)	Test conditions follow standard test methods and procedures for measuring thermal impedance, per EIA/JESD51.	55	°C/W
Θ <sub>JC</sub>	Thermal Resistance (Junction to Case)		17	°C/W

## Capacitance<sup>[9]</sup>

Parameter	Description	Test Conditions	Max.	Unit
C <sub>IN</sub>	Input Capacitance	T <sub>A</sub> = 25°C, f = 1 MHz, V <sub>CC</sub> = V <sub>CC(typ)</sub>	8	pF
C <sub>OUT</sub>	Output Capacitance		8	pF

### Notes:

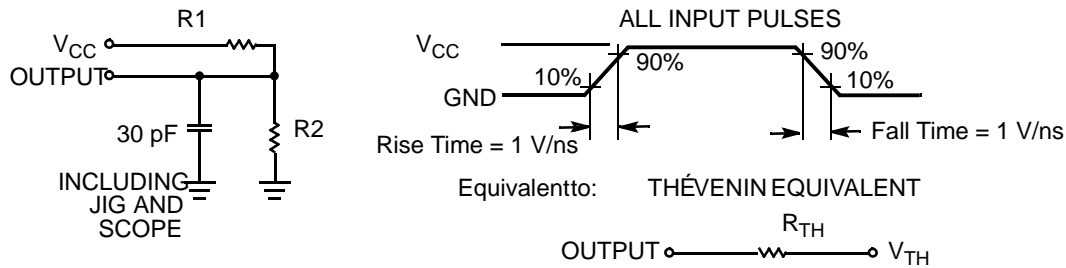
6. V<sub>IL(MIN)</sub> = -0.5V for pulse durations less than 20 ns.

7. V<sub>IH(Max)</sub> = V<sub>CC</sub> + 0.5V for pulse durations less than 20 ns.

8. Overshoot and undershoot specifications are characterized and are not 100% tested.

9. Tested initially and after any design or process changes that may affect these parameters.

## AC Test Loads and Waveforms



Parameters	3.0V V <sub>CC</sub>	Unit
R1	22000	Ω
R2	22000	Ω
R <sub>TH</sub>	11000	Ω
V <sub>TH</sub>	1.50	V

## Switching Characteristics Over the Operating Range<sup>[10]</sup>

Parameter	Description	55 ns <sup>[14]</sup>		60 ns		70 ns		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
Read Cycle								
t <sub>RC</sub>	Read Cycle Time	55		60		70		ns
t <sub>AA</sub>	Address to Data Valid		55		60		70	ns
t <sub>OHA</sub>	Data Hold from Address Change	5		8		10		ns
t <sub>ACE</sub>	$\overline{CE}$ LOW to Data Valid		55		60		70	ns
t <sub>DOE</sub>	$\overline{OE}$ LOW to Data Valid		25		25		35	ns
t <sub>LZOE</sub>	$\overline{OE}$ LOW to LOW Z <sup>[11, 13]</sup>	5		5		5		ns
t <sub>HZOE</sub>	$\overline{OE}$ HIGH to High Z <sup>[11, 13]</sup>		25		25		25	ns
t <sub>LZCE</sub>	$\overline{CE}$ LOW to Low Z <sup>[11, 13]</sup>	2		2		5		ns
t <sub>HZCE</sub>	$\overline{CE}$ HIGH to High Z <sup>[11, 13]</sup>		25		25		25	ns
t <sub>DBE</sub>	BLE/BHE LOW to Data Valid		55		60		70	ns
t <sub>LZBE</sub>	$\overline{BLE/BHE}$ LOW to Low Z <sup>[11, 13]</sup>	5		5		5		ns
t <sub>HZBE</sub>	$\overline{BLE/BHE}$ HIGH to HIGH Z <sup>[11, 13]</sup>		10		10		25	ns
t <sub>SK</sub> <sup>[14]</sup>	Address Skew		0		5		10	ns
Write Cycle <sup>[12]</sup>								
t <sub>WC</sub>	Write Cycle Time	55		60		70		ns
t <sub>SCE</sub>	$\overline{CE}$ LOW to Write End	45		45		60		ns
t <sub>AW</sub>	Address Set-Up to Write End	45		45		55		ns
t <sub>HA</sub>	Address Hold from Write End	0		0		0		ns
t <sub>SA</sub>	Address Set-Up to Write Start	0		0		0		ns
t <sub>PWE</sub>	WE Pulse Width	40		40		45		ns

### Notes:

10. Test conditions for all parameters other than tri-state parameters assume signal transition time of 1 ns/V, timing reference levels of V<sub>CC(typ)</sub>/2, input pulse levels of 0V to V<sub>CC(typ)</sub>, and output loading of the specified I<sub>OL</sub>/I<sub>OH</sub> as shown in the "AC Test Loads and Waveforms" section.

11. t<sub>HZOE</sub>, t<sub>HZCE</sub>, t<sub>HZBE</sub>, and t<sub>HZWE</sub> transitions are measured when the outputs enter a high impedance state.

12. The internal Write time of the memory is defined by the overlap of  $\overline{WE}$ ,  $\overline{CE} = V_{IL}$ , BHE and/or BLE = V<sub>IL</sub>. All signals must be ACTIVE to initiate a write and any of these signals can terminate a write by going INACTIVE. The data input set-up and hold timing should be referenced to the edge of the signal that terminates the write.

13. High-Z and Low-Z parameters are characterized and are not 100% tested.

14. To achieve 55-ns performance, the read access should be  $\overline{CE}$  controlled. In this case t<sub>ACE</sub> is the critical parameter and t<sub>SK</sub> is satisfied when the addresses are stable prior to chip enable going active. For the 70-ns cycle, the addresses must be stable within 10 ns after the start of the read cycle.

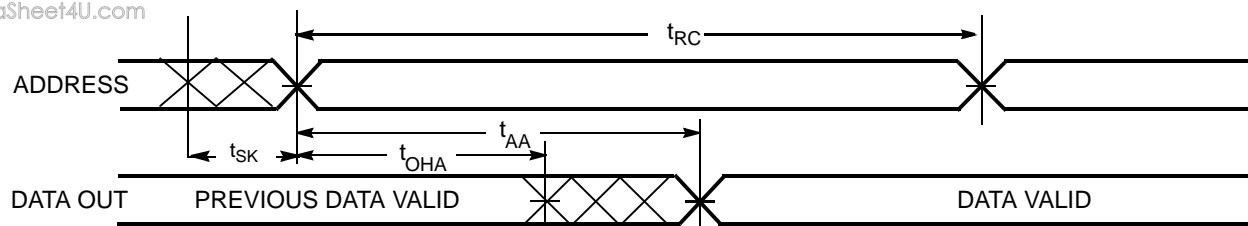
## Switching Characteristics Over the Operating Range<sup>[10]</sup> (continued)

Parameter	Description	55 ns <sup>[14]</sup>		60 ns		70 ns		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
$t_{BW}$	BLE/BHE LOW to Write End	50		50		55		ns
$t_{SD}$	Data Set-Up to Write End	25		25		25		ns
$t_{HD}$	Data Hold from Write End	0		0		0		ns
$t_{HZWE}$	$\overline{WE}$ LOW to High-Z <sup>[11, 13]</sup>		25		25		25	ns
$t_{LZWE}$	$\overline{WE}$ HIGH to Low-Z <sup>[11, 13]</sup>	5		5		5		ns

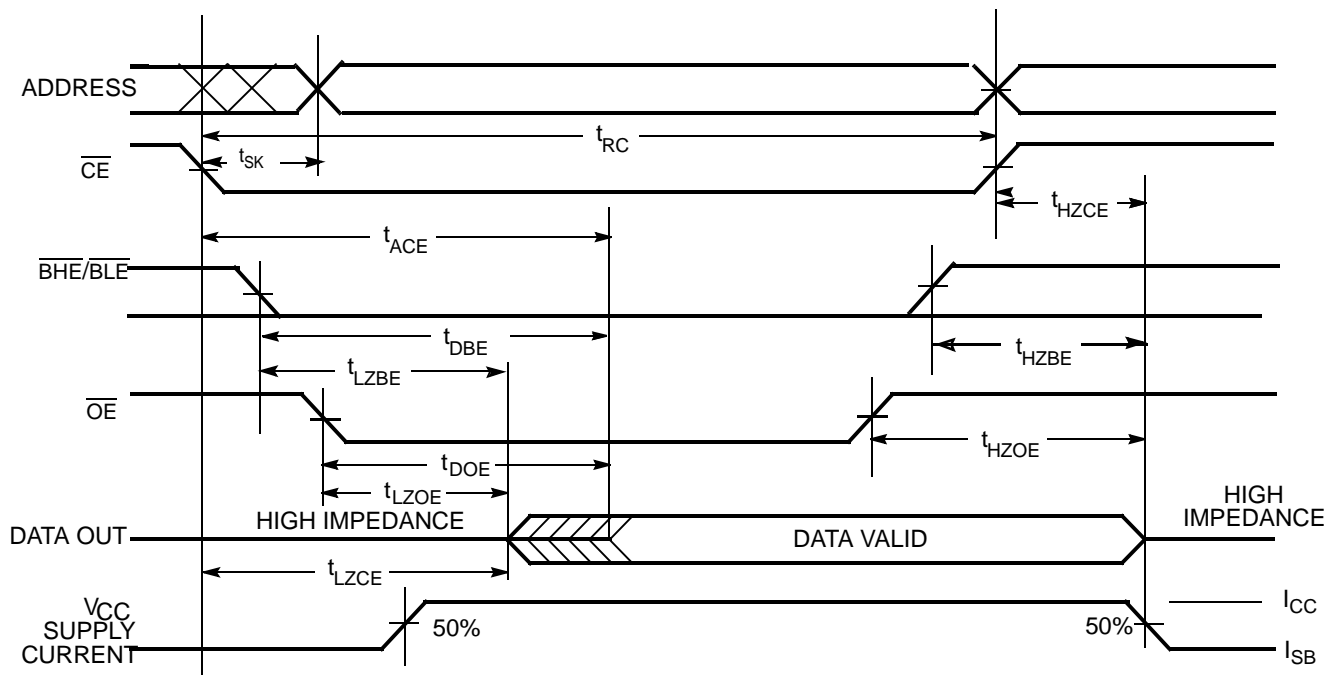
## Switching Waveforms

### Read Cycle 1 (Address Transition Controlled)<sup>[14, 15, 16]</sup>

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### Read Cycle 2 ( $\overline{OE}$ Controlled)<sup>[14, 16]</sup>

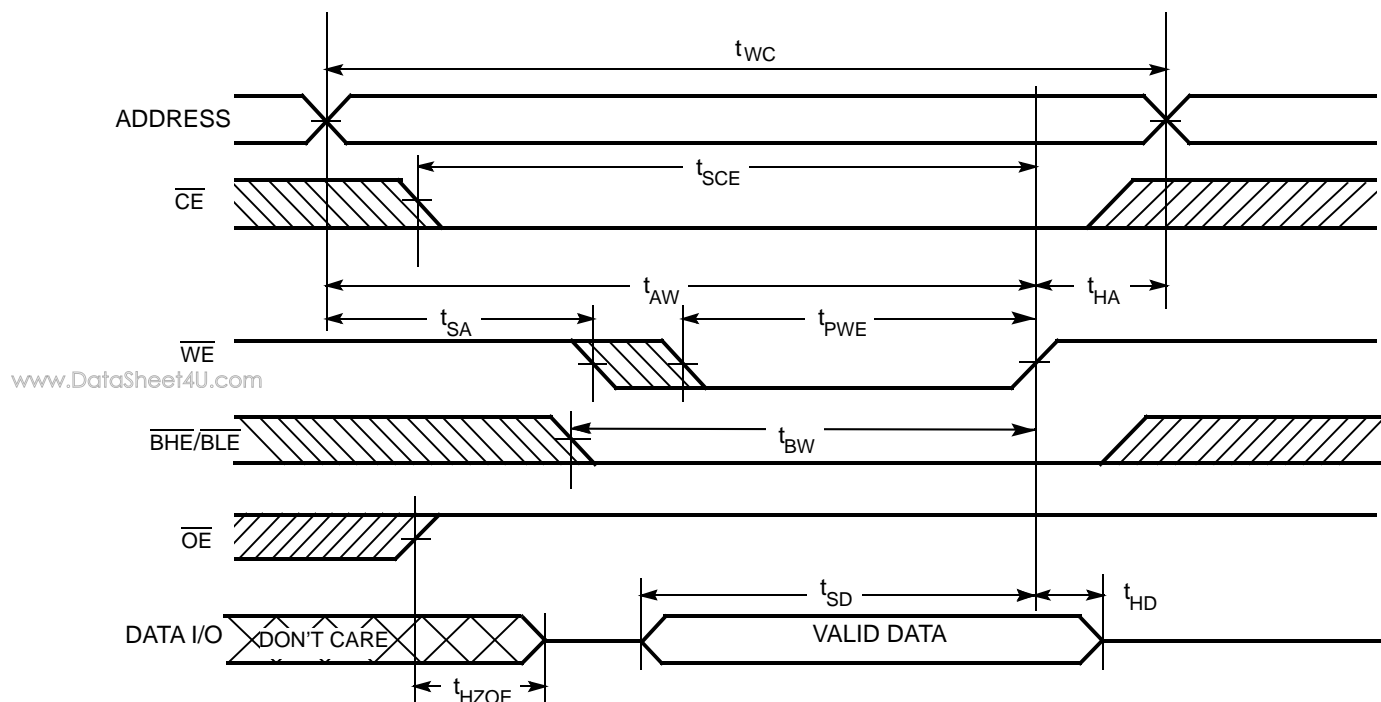


#### Notes:

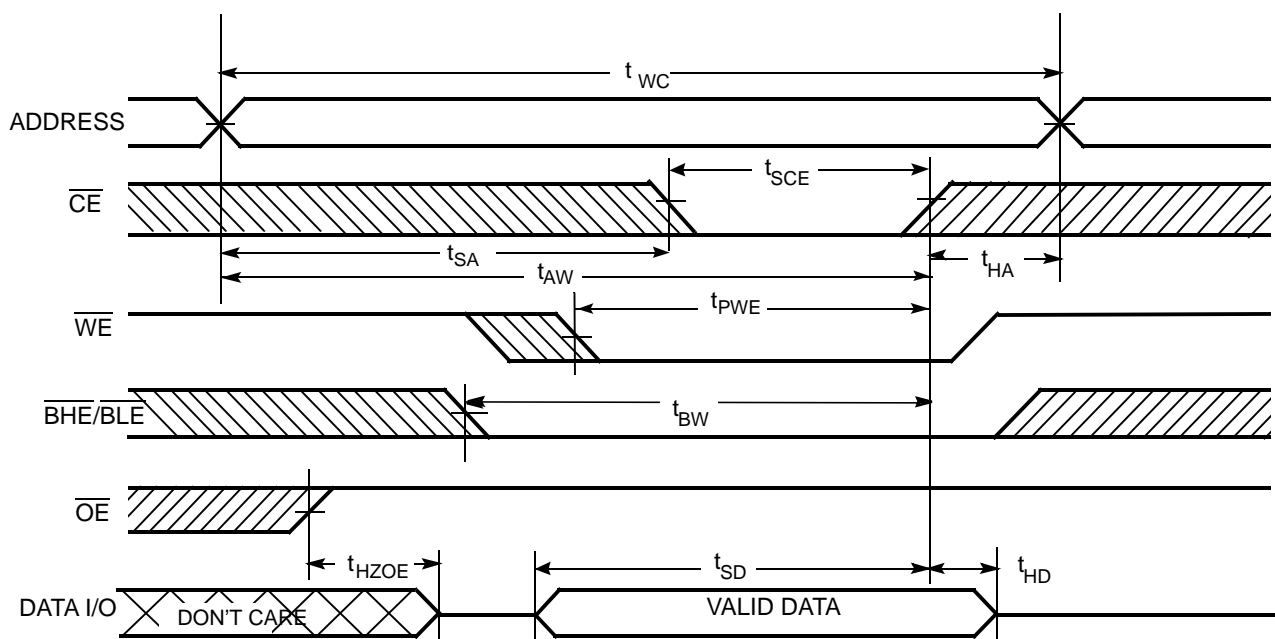
15. Device is continuously selected.  $\overline{OE}$ ,  $\overline{CE} = V_{IL}$ .  
16.  $\overline{WE}$  is HIGH for Read Cycle.

## Switching Waveforms (continued)

### Write Cycle 1 (WE Controlled) [12, 13, 17, 18, 19]



### Write Cycle 2 (CE Controlled) [12, 13, 17, 18, 19]

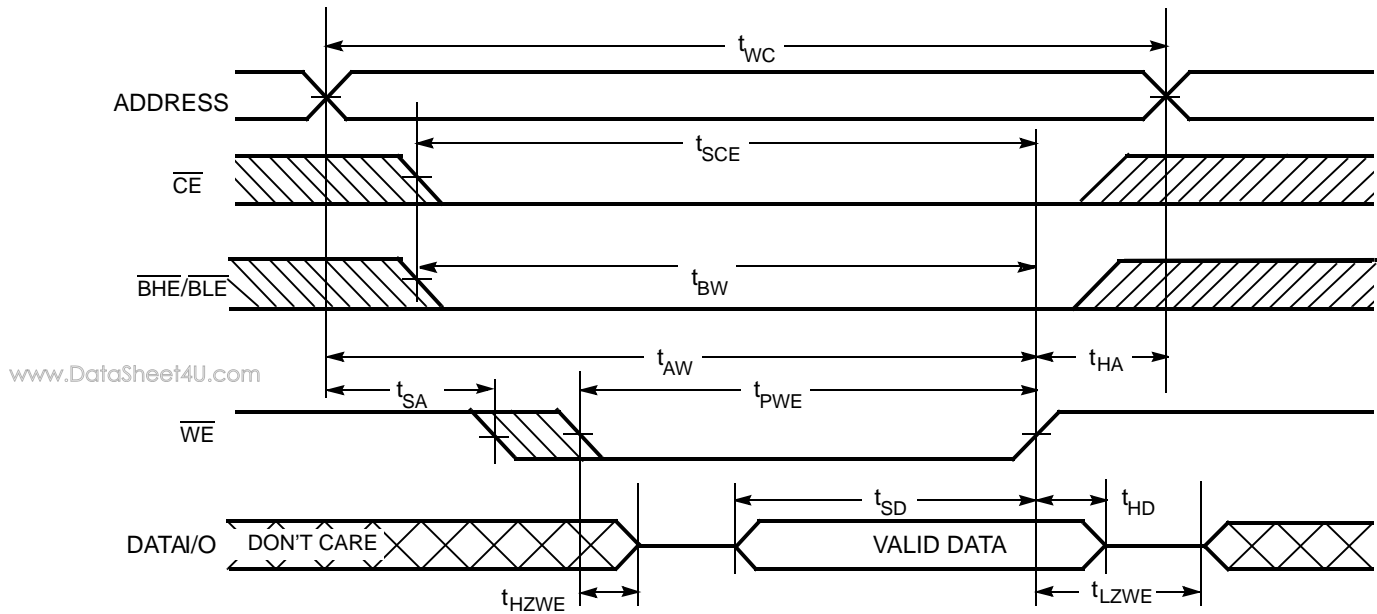


#### Notes:

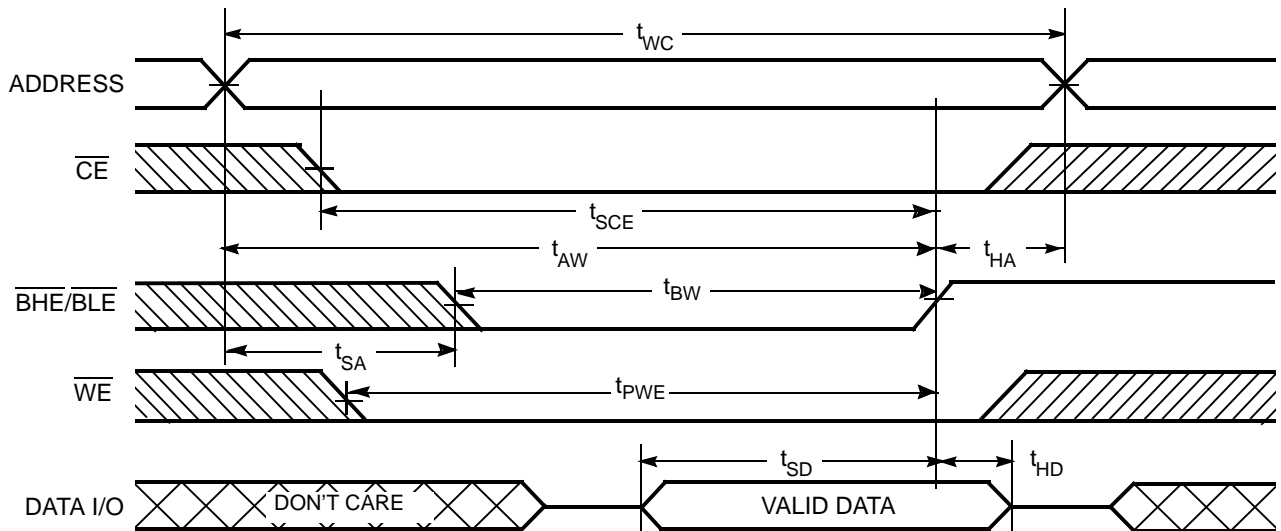
17. Data I/O is high-impedance if  $\overline{OE} \geq V_{IH}$ .
18. If Chip Enable goes INACTIVE with  $\overline{WE} = V_{IH}$ , the output remains in a high-impedance state.
19. During this period in the DATA I/O waveform, the I/Os could be in the output state and input signals should not be applied.

## Switching Waveforms (continued)

### Write Cycle 3 ( $\overline{\text{WE}}$ Controlled, $\overline{\text{OE}}$ LOW)<sup>[18, 19]</sup>



### Write Cycle 4 ( $\overline{\text{BHE/BLER}}$ Controlled, $\overline{\text{OE}}$ LOW)<sup>[18, 19]</sup>



**Truth Table** <sup>[20]</sup>

CE	WE	OE	BHE	BLE	Inputs/Outputs	Mode	Power
H	X	X	X	X	High Z	Deselect/Power-Down	Standby ( $I_{SB}$ )
X	X	X	H	H	High Z	Deselect/Power-Down	Standby ( $I_{SB}$ )
L	H	L	L	L	Data Out (I/O0 – I/O15)	Read	Active ( $I_{CC}$ )
L	H	L	H	L	Data Out (I/O0 – I/O7); High Z (I/O8 – I/O15)	Read	Active ( $I_{CC}$ )
L	H	L	L	H	High Z (I/O0 – I/O7); Data Out (I/O8 – I/O15)	Read	Active ( $I_{CC}$ )
L	H	H	L	H	High Z	Output Disabled	Active ( $I_{CC}$ )
L	H	H	H	L	High Z	Output Disabled	Active ( $I_{CC}$ )
L	H	H	L	L	High Z	Output Disabled	Active ( $I_{CC}$ )
L	L	X	L	L	Data In (I/O0 – I/O15)	Write	Active ( $I_{CC}$ )
L	L	X	H	L	Data In (I/O0 – I/O7); High Z (I/O8 – I/O15)	Write	Active ( $I_{CC}$ )
L	L	X	L	H	High Z (I/O0 – I/O7); Data In (I/O8 – I/O15)	Write	Active ( $I_{CC}$ )

## Ordering Information

Speed (ns)	Ordering Code	Package Diagram	Package Type	Operating Range
55	CYK256K16MCCBU-55BVI	51-85150	48-ball Fine Pitch BGA (6 mm × 8mm × 1.0 mm)	Industrial
	CYK256K16MCBU-55BVXI		48-ball Fine Pitch BGA (6 mm × 8mm × 1.0 mm) (Pb-Free)	
60	CYK256K16MCCBU-60BVI	51-85150	48-ball Fine Pitch BGA (6 mm × 8mm × 1.0 mm)	Industrial
70	CYK256K16MCCBU-70BVI	51-85150	48-ball Fine Pitch BGA (6 mm × 8mm × 1.0 mm)	Industrial
	CYK256K16MCBU-70BVXI		48-ball Fine Pitch BGA (6 mm × 8mm × 1.0 mm) (Pb-Free)	

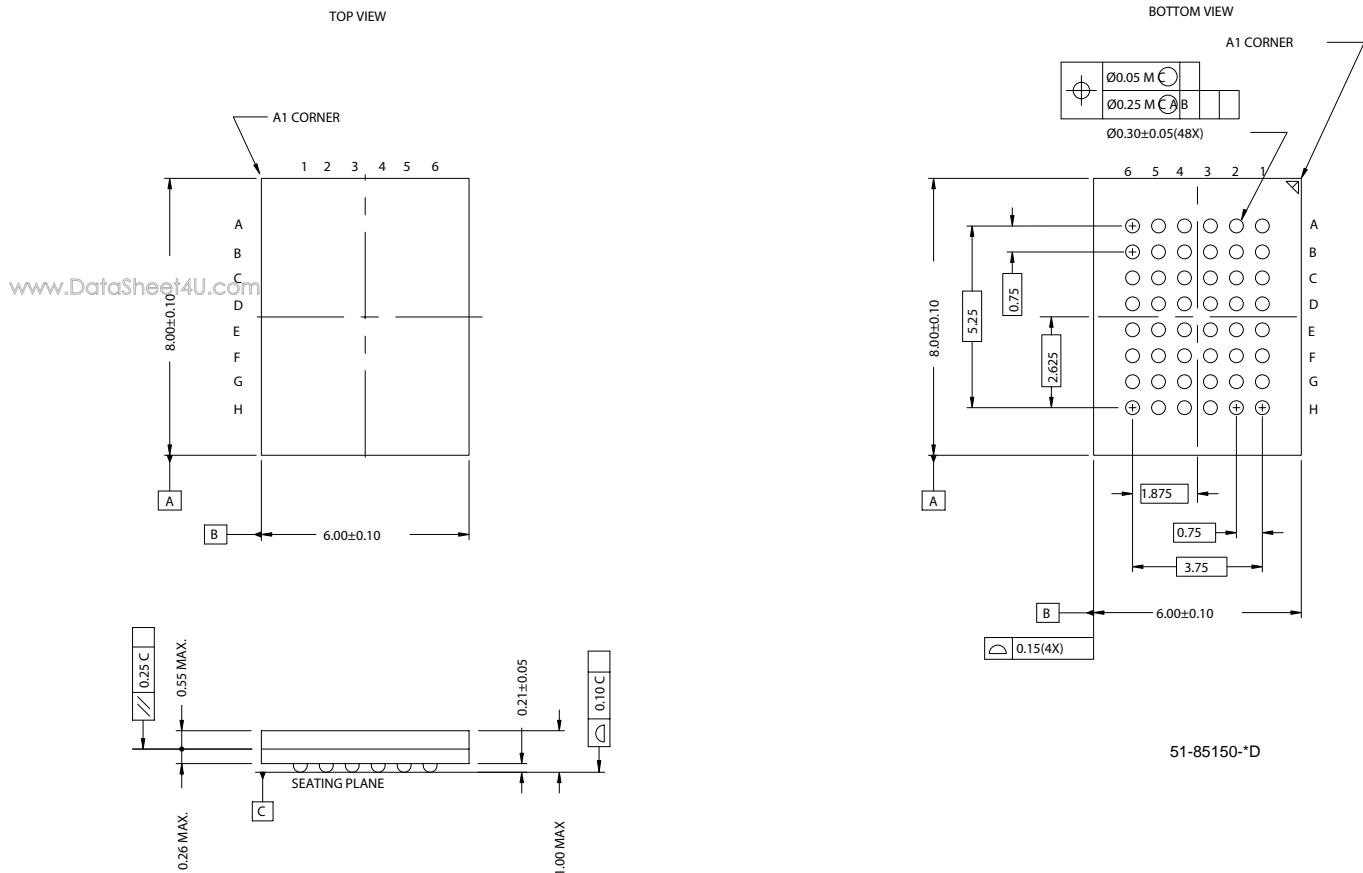
**Note:**

20. H = Logic HIGH, L = Logic LOW, X = Don't Care.



## Package Diagram

### 48-ball VFBGA (6 x 8 x 1 mm) (51-85150)



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## Document History Page

**Document Title: CYK256K16MCCB MoBL3™4-Mbit (256K x 16) Pseudo Static RAM**  
**Document Number: 38-05585**

REV.	ECN NO.	Issue Date	Orig. of Change	Description of Change
**	223482	See ECN	REF	New data sheet
*A	234474	See ECN	SYT	Changed ball E3 on package pinout from NC to DNU
*B	260330	See ECN	PCI	Changed from preliminary to final
*C	298651	See ECN	PCI	Added 60-ns speed bin
*D	314013	See ECN	RKF	Added Pb-Free parts to the Ordering information
*E	397852	See ECN	SYT	Changed address of Cypress Semiconductor Corporation on Page# 1 from "3901 North First Street" to "198 Champion Court" Changed typo in ordering code from CYK256K16MCCB to CYK256K16MCCBU in the "Ordering Information" on Page#8 Updated the revision of package diagram of Spec 51-85150 from *B to *D
*F	522566	See ECN	NXR	Changed $V_{IL}$ Max spec from 0.4 V to 0.6 V in DC Electrical Characteristics table