LOW SKEW, DUAL, PROGRAMMABLE 1-TO-2 DIFFERENTIAL-TO-LVDS, LVPECL FANOUT BUFFER

ICS854S204I

General Description

The ICS854S204I is a low skew, high performance dual, programmable 1-to-2 Differential-to-LVDS, LVPECL Fanout Buffer and a member of the HiPerClockS™ family of High Performance Clock Solutions from IDT. The PCLKx, nPCLKx pairs can accept most standard differential input levels. With the selection of SEL_OUT signal, outputs can be selected be to either LVDS or LVPECL levels. The ICS854S204I is characterized to operate from either a 2.5V or a 3.3V power supply. Guaranteed output and bank skew characteristics make the ICS854S204I ideal for those clock distribution applications demanding well defined performance and repeatability.

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Features

- Two programmable differential LVDS or LVPECL output banks
- Two differential clock input pairs
- PCLKx, nPCLKx pairs can accept the following differential input levels: LVDS, LVPECL, SSTL, CML
- Maximum output frequency: 3GHz
- Translates any single ended input signal to LVDS levels with resistor bias on nPCLKx inputs
- Output skew: 15ps (maximum)
- Bank skew: 15ps (maximum)
- Propagation delay: 500ps (maximum)
- Additive phase jitter, RMS: 0.15ps (typical)
- Full 3.3V or 2.5V power supply
- -40°C to 85°C ambient operating temperature
- Available in lead-free (RoHS 6) package

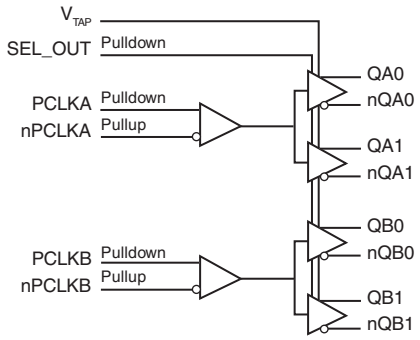
Power Supply Configuration Table

3.3V Operation	V_{DD} = 3.3V
	V_{TAP} = nc
2.5V Operation	V_{DD} = 2.5V
	V_{TAP} = 2.5V

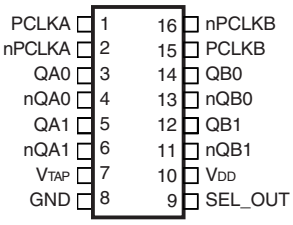
SEL_OUT Function Table

SEL_OUT	Output Level
0	LVDS
1	LVPECL

Block Diagram



Pin Assignment



ICS854S204I
16-Lead TSSOP
4.4mm x 5.0mm x 0.925mm package body
G Package
Top View

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TABLE 1. PIN DESCRIPTIONS

Number	Name	Type		Description
1	PCLKA	Input	Pulldown	Non-inverting differential clock input.
2	nPCLKA	Input	Pullup	Inverting differential clock input.
3, 4	QA0, nQA0	Output		Differential output pair. LVDS or LVPECL interface levels.
5, 6	QA1, nQA1	Output		Differential output pair. LVDS or LVPECL interface levels.
7	V_{TAP}	Power		Power supply pin. Tie to V_{DD} for 2.5V operation. For 3.3V operation, do not connect.
8	GND	Power		Power supply ground.
9	SEL_OUT	Input	Pulldown	Selects between LVDS or LVPECL outputs.
10	V_{DD}	Power		Power supply pin.
11, 12	nQB1, QB1	Output		Differential output pair. LVDS or LVPECL interface levels.
13, 14	nQB0, QB0	Output		Differential output pair. LVDS or LVPECL interface levels.
15	PCLKB	Input	Pulldown	Non-inverting differential clock input.
16	nPCLKB	Input	Pullup	Inverting differential clock input.

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NOTE: *Pullup* and *Pulldown* refer to internal input resistors. See Table 2, Pin Characteristics, for typical values.

TABLE 2. PIN CHARACTERISTICS

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
C_{IN}	Input Capacitance			1		pF
R_{PULLUP}	Input Pullup Resistor			51		kΩ
$R_{PULLDOWN}$	Input Pulldown Resistor			51		kΩ

TABLE 3. CLOCK INPUT FUNCTION TABLE

Inputs		Outputs		Input to Output Mode	Polarity
PCLKA or PCLKB	nPCLKA or nPCLKB	QA0, QA1, QB0, QB1	nQA0, nQA1, nQB0, nQB1		
0	1	LOW	HIGH	Differential to Differential	Non Inverting
1	0	HIGH	LOW	Differential to Differential	Non Inverting
0	Biased; NOTE 1	LOW	HIGH	Single Ended to Differential	Non Inverting
1	Biased; NOTE 1	HIGH	LOW	Single Ended to Differential	Non Inverting
Biased; NOTE 1	0	HIGH	LOW	Single Ended to Differential	Inverting
Biased; NOTE 1	1	LOW	HIGH	Single Ended to Differential	Inverting

NOTE 1: Please refer to the Application Information, "Wiring the Differential Input to Accept Single Ended Levels".

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Absolute Maximum Ratings

Supply Voltage, V_{DD} 4.6V

Inputs, V_I -0.5V to V_{DD} + 0.5 V

Outputs, I_O (LVPECL)
Continuous Current 50mA
Surge Current 100mA

Outputs, I_O (LVDS)
Continuous Current 10mA
Surge Current 15mA

Package Thermal Impedance, θ_{JA} 92°C/W (0 mps)
(Junction-to-Ambient)

Storage Temperature, T_{STG} -65°C to 150°C

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NOTE: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the *DC Characteristics* or *AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

Table 4A. LVDS Power Supply DC Characteristics, V_{DD} = 3.3V±5%, T_A = -40°C to 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{DD}	Power Supply Voltage		3.135	3.3	3.465	V
I_{DD}	Power Supply Current				120	mA

Table 4B. LVDS Power Supply DC Characteristics, V_{DD} = V_{TAP} = 2.5V±5%, T_A = -40°C to 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{DD}	Power Supply Voltage		2.375	2.5	2.625	V
V_{TAP}	Power Supply Voltage		2.375	2.5	2.625	V
I_{DD}	Power Supply Current				115	mA
I_{TAP}	Power Supply Current				5	mA

Table 4C. LVPECL Power Supply DC Characteristics, V_{DD} = 3.3V±5%, T_A = -40°C to 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{DD}	Power Supply Voltage		3.135	3.3	3.465	V
I_{DD}	Power Supply Current				66	mA

Table 4D. LVPECL Power Supply DC Characteristics, V_{DD} = V_{TAP} = 2.5V±5%, T_A = -40°C to 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{DD}	Power Supply Voltage		2.375	2.5	2.625	V
V_{TAP}	Power Supply Voltage		2.375	2.5	2.625	V
I_{DD}	Power Supply Current				60	mA
I_{TAP}	Power Supply Current				5	mA

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TABLE 4E. LVCMOS / LVTTL DC CHARACTERISTICS, V_{DD} = 3.3V±5% OR $V_{DD} = V_{TAP}$ = 2.5V±5%, T_A = -40°C TO 85°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
V_{IH}	Input High Voltage		V_{DD} = 3.3V	2		V_{CC} + 0.3	V
			V_{DD} = 2.625V	1.7		V_{CC} + 0.3	V
V_{IL}	Input Low Voltage		V_{DD} = 3.3V	-0.3		0.8	V
			V_{DD} = 2.625V	-0.3		0.7	V
I_{IH}	Input High Current	SEL_OUT	$V_{DD} = V_{IN}$ = 3.465V or 2.625V			150	µA
I_{IL}	Input Low Current	SEL_OUT	V_{DD} = 3.465V or 2.625V, V_{IN} = 0V	-10			µA

TABLE 4F. DIFFERENTIAL DC CHARACTERISTICS, V_{DD} = 3.3V±5% OR $V_{DD} = V_{TAP}$ = 2.5V±5%, T_A = -40°C TO 85°C

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Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
I_{IH}	Input High Current	PCLKA, PCLKB	$V_{DD} = V_{IN}$ = 3.465V or 2.625V			150	µA
		nPCLKA, nPCLKB	V_{DD} = 3.465V or 2.625V, V_{IN} = 0V			10	µA
I_{IL}	Input Low Current	PCLKA, PCLKB	$V_{DD} = V_{IN}$ = 3.465V or 2.625V	-10			µA
		nPCLKA, nPCLKB	V_{DD} = 3.465V or 2.625V, V_{IN} = 0V	-150			µA
V_{PP}	Peak-to-Peak Input Voltage; NOTE 1			0.15		1.3	V
V_{CMR}	Common Mode Input Voltage; NOTE 1, 2			GND + 0.5		V_{DD} - 0.85	V

NOTE 1: V_{IL} should not be less than -0.3V.
NOTE 2: Common mode voltage is defined as V_{IH}.

TABLE 4G. LVDS DC CHARACTERISTICS, V_{DD} = 3.3V±5%, T_A = -40°C TO 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{OD}	Differential Output Voltage	SEL_OUT = 0	247	350	454	mV
ΔV_{OD}	V_{OD} Magnitude Change	SEL_OUT = 0			50	mV
V_{OS}	Offset Voltage	SEL_OUT = 0	1.11	1.25	1.38	V
ΔV_{OS}	V_{OS} Magnitude Change	SEL_OUT = 0			50	mV

NOTE: Please refer to Parameter Measurement Information for output information.

TABLE 4H. LVDS DC CHARACTERISTICS, $V_{DD} = V_{TAP}$ = 2.5V±5%, T_A = -40°C TO 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{OD}	Differential Output Voltage	SEL_OUT = 0	247	350	454	mV
ΔV_{OD}	V_{OD} Magnitude Change	SEL_OUT = 0			50	mV
V_{OS}	Offset Voltage	SEL_OUT = 0	1.08	1.21	1.34	V
ΔV_{OS}	V_{OS} Magnitude Change	SEL_OUT = 0			50	mV

NOTE: Please refer to Parameter Measurement Information for output information.

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TABLE 4I. LVPECL DC CHARACTERISTICS, V_{DD} = 3.3V±5%, TA = -40°C TO 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{OH}	Output High Voltage; NOTE 1	SEL_OUT = 1	V_{DD} - 1.3		V_{DD} - 0.8	V
V_{OL}	Output Low Voltage; NOTE 1	SEL_OUT = 1	V_{DD} - 2.0		V_{DD} - 1.6	V
V_{SWING}	Peak-to-Peak Output Voltage Swing	SEL_OUT = 1	0.6		0.9	V

NOTE 1: Outputs terminated with 50Ω to V_{DD} - 2V.

TABLE 4J. LVPECL DC CHARACTERISTICS, V_{DD} = V_{TAP} = 2.5V±5%, TA = -40°C TO 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{OH}	Output High Voltage; NOTE 1	SEL_OUT = 1	V_{DD} - 1.3		V_{DD} - 0.8	V
V_{OL}	Output Low Voltage; NOTE 1	SEL_OUT = 1	V_{DD} - 2.0		V_{DD} - 1.55	V
V_{SWING}	Peak-to-Peak Output Voltage Swing	SEL_OUT = 1	0.6		0.9	V

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NOTE 1: Outputs terminated with 50Ω to V_{DD} - 2V.

TABLE 5A. LVDS AC CHARACTERISTICS, V_{DD} = 3.3V ± 5%, TA = -40°C TO 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
f_{MAX}	Output Frequency				3	GHz
t_{PD}	Propagation Delay; NOTE 1				500	ps
*t*sk(o)	Output Skew; NOTE 2, 4				15	ps
*t*sk(b)	Bank Skew; NOTE 3, 4				15	ps
*t*jit	Buffer Additive Phase Jitter, RMS; refer to Additive Phase Jitter Section	100MHz, Integration Range: 12kHz – 20MHz		0.15		ps
t_R / t_F	Output Rise/Fall Time	20% to 80%	100		200	ps
odc	Output Duty Cycle		49		51	%

All parameters measured at 550MHz unless noted otherwise.
NOTE 1: Measured from the differential input crossing point to the differential output crossing point.
NOTE 2: Defined as skew between outputs at the same supply voltage and with equal load conditions.
Measured from the output differential cross points.
NOTE 3: Defined as skew within a bank of outputs at the same supply voltage and with equal load conditions.
NOTE 4: This parameter is defined in accordance with JEDEC Standard 65.

TABLE 5B. LVDS AC CHARACTERISTICS, V_{DD} = V_{TAP} = 2.5V ± 5%, TA = -40°C TO 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
f_{MAX}	Output Frequency				3	GHz
t_{PD}	Propagation Delay; NOTE 1				500	ps
*t*sk(o)	Output Skew; NOTE 2, 4				15	ps
*t*sk(b)	Bank Skew; NOTE 3, 4				15	ps
*t*jit	Buffer Additive Phase Jitter, RMS; refer to Additive Phase Jitter Section	100MHz, Integration Range: 12kHz – 20MHz		0.13		ps
t_R / t_F	Output Rise/Fall Time	20% to 80%	100		200	ps
odc	Output Duty Cycle		49		51	%

For NOTES, see Table 5A above.

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TABLE 5C. LVPECL AC CHARACTERISTICS, V_{DD} = 3.3V ± 5%, T_A = -40°C TO 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
f_{MAX}	Output Frequency				3	GHz
t_{PD}	Propagation Delay; NOTE 1				500	ps
*t*sk(o)	Output Skew; NOTE 2, 4				15	ps
*t*sk(b)	Bank Skew; NOTE 3, 4				15	ps
*t*jit	Buffer Additive Phase Jitter, RMS; refer to Additive Phase Jitter Section	100MHz, Integration Range: 12kHz – 20MHz		0.12		ps
t_R / t_F	Output Rise/Fall Time	20% to 80%	100		200	ps
odc	Output Duty Cycle		49		51	%

All parameters measured at 550MHz unless noted otherwise.
NOTE 1: Measured from the differential input crossing point to the differential output crossing point.
NOTE 2: Defined as skew between outputs at the same supply voltage and with equal load conditions.
Measured from the output differential cross points.
NOTE 3: Defined as skew within a bank of outputs at the same supply voltage and with equal load conditions.
NOTE 4: This parameter is defined in accordance with JEDEC Standard 65.

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TABLE 5D. LVPECL AC CHARACTERISTICS, V_{DD} = V_{TAP} = 2.5V ± 5%, T_A = -40°C TO 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
f_{MAX}	Output Frequency				3	GHz
t_{PD}	Propagation Delay; NOTE 1				500	ps
*t*sk(o)	Output Skew; NOTE 2, 4				15	ps
*t*sk(b)	Bank Skew; NOTE 3, 4				15	ps
*t*jit	Buffer Additive Phase Jitter, RMS; refer to Additive Phase Jitter Section	100MHz, Integration Range: 12kHz – 20MHz		0.07		ps
t_R / t_F	Output Rise/Fall Time	20% to 80%	100		200	ps
odc	Output Duty Cycle		49		51	%

All parameters measured at 550MHz unless noted otherwise.
NOTE 1: Measured from the differential input crossing point to the differential output crossing point.
NOTE 2: Defined as skew between outputs at the same supply voltage and with equal load conditions.
Measured from the output differential cross points.
NOTE 3: Defined as skew within a bank of outputs at the same supply voltage and with equal load conditions.
NOTE 4: This parameter is defined in accordance with JEDEC Standard 65.

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Additive Phase Jitter

The spectral purity in a band at a specific offset from the fundamental compared to the power of the fundamental is called the ***dBc Phase Noise.*** This value is normally expressed using a Phase noise plot and is most often the specified plot in many applications. Phase noise is defined as the ratio of the noise power present in a 1Hz band at a specified offset from the fundamental frequency to the power value of the fundamental. This ratio is expressed in decibels (dBm) or a ratio of the power in the 1Hz band to the power in the fundamental. When the required offset is specified, the phase noise is called a ***dBc*** value, which simply means dBm at a specified offset from the fundamental. By investigating jitter in the frequency domain, we get a better understanding of its effects on the desired application over the entire time record of the signal. It is mathematically possible to calculate an expected bit error rate given a phase noise plot.

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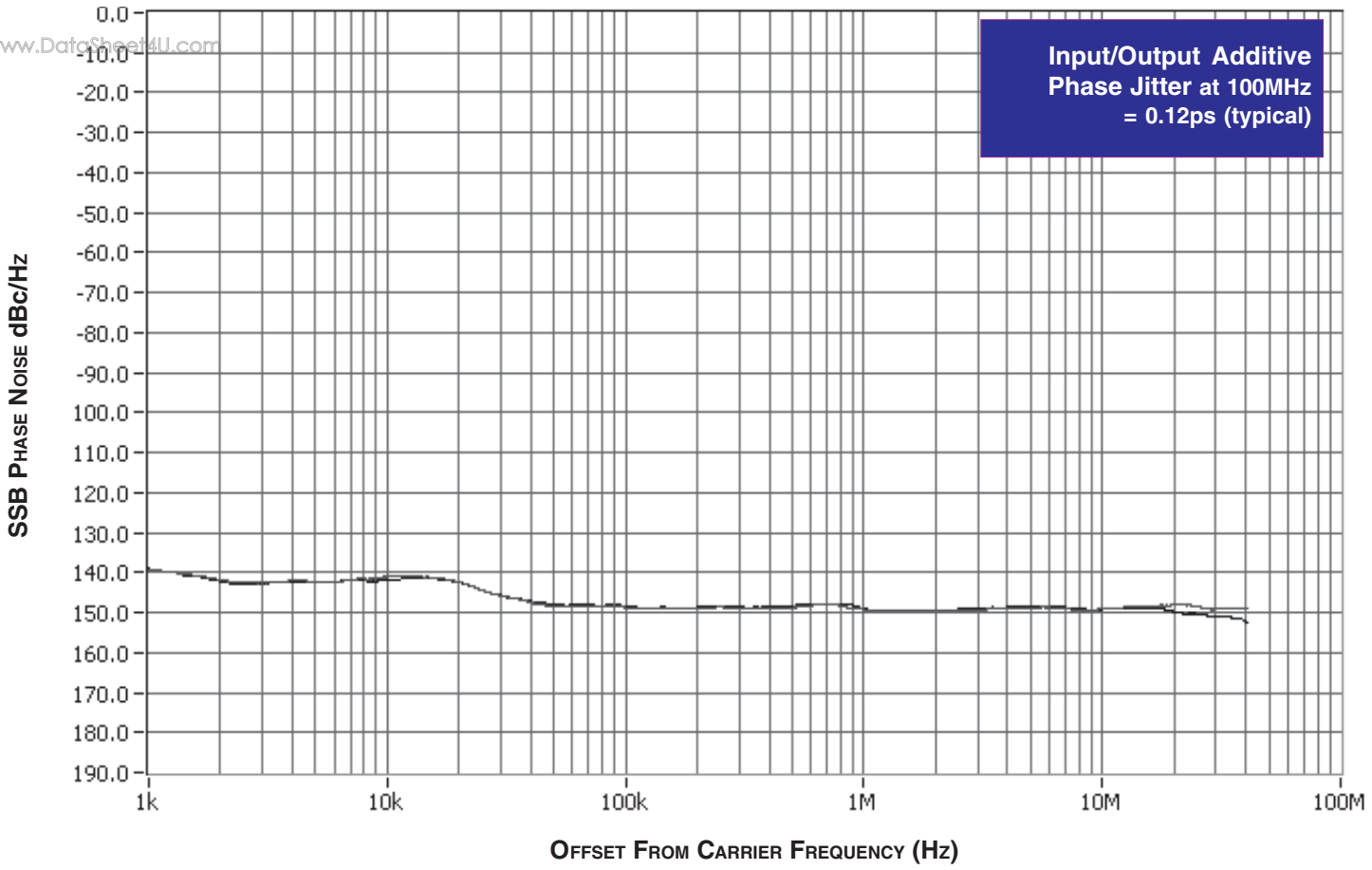

As with most timing specifications, phase noise measurements has issues relating to the limitations of the equipment. Often the noise floor of the equipment is higher than the noise floor of the device. This is illustrated above. The device meets the noise floor of what is shown, but can actually be lower. The phase noise is dependent on the input source and measurement equipment.

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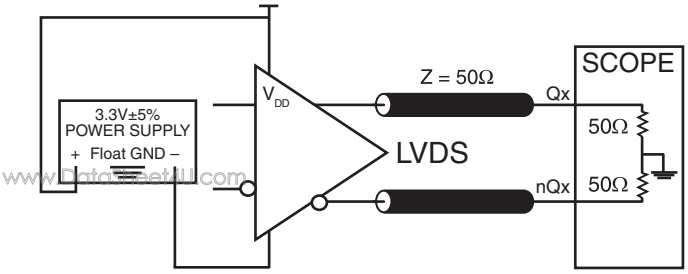
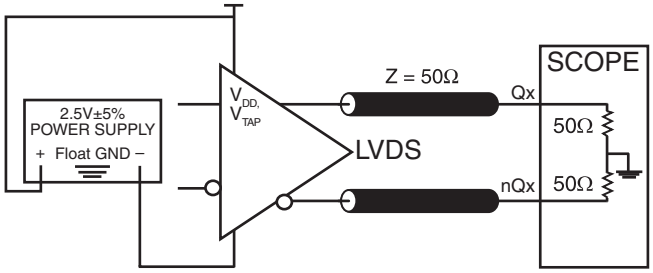
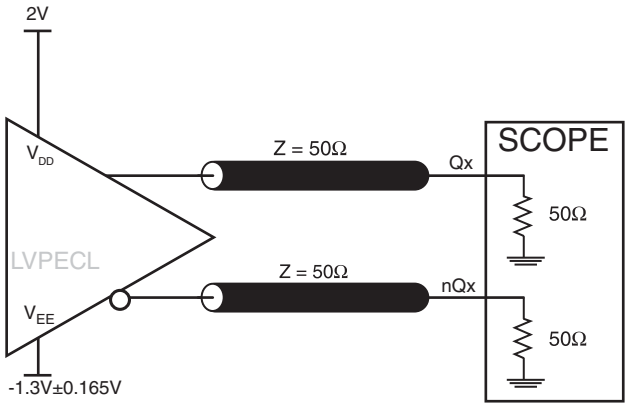
PARAMETER MEASUREMENT INFORMATION



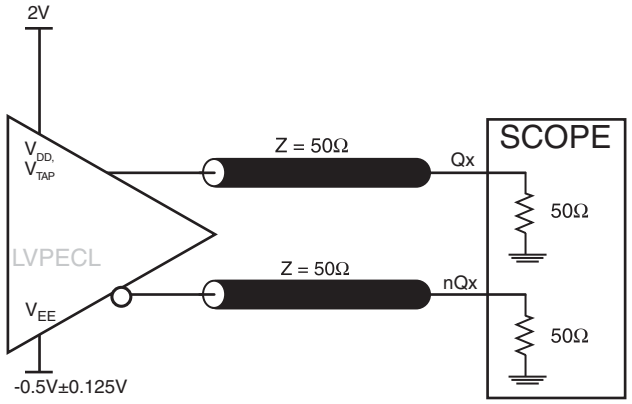
3.3V LVDS OUTPUT LOAD AC TEST CIRCUIT



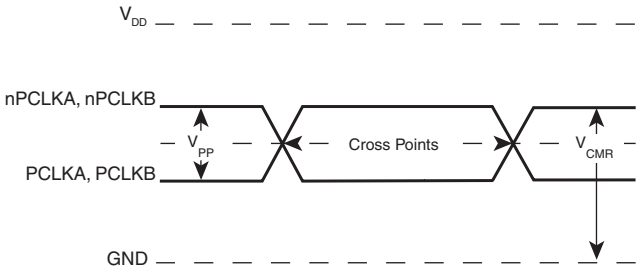
2.5V LVDS OUTPUT LOAD AC TEST CIRCUIT



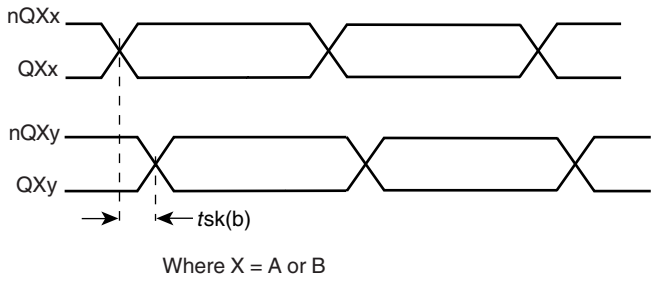
3.3V LVPECL OUTPUT LOAD AC TEST CIRCUIT



2.5V LVPECL OUTPUT LOAD AC TEST CIRCUIT



DIFFERENTIAL INPUT LEVEL



BANK SKEW

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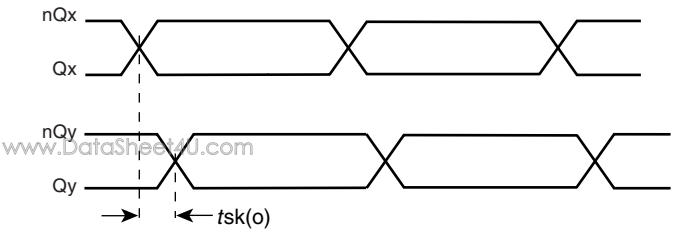
PARAMETER MEASUREMENT INFORMATION, CONTINUED



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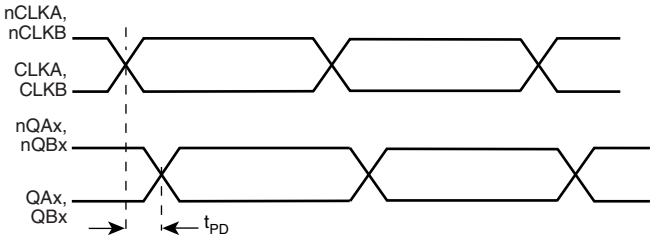
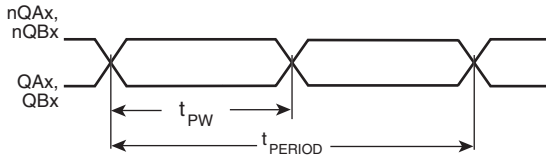
OUTPUT SKEW

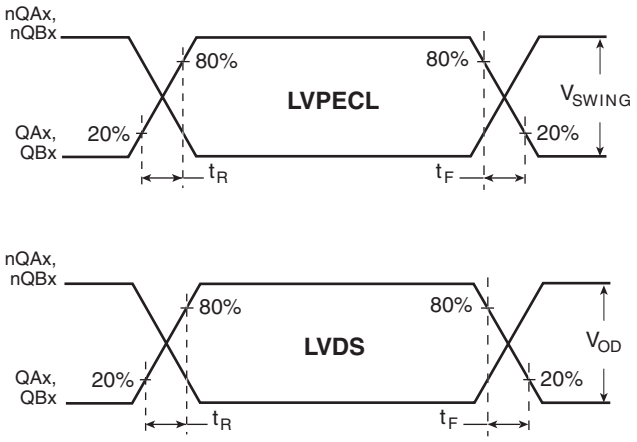


PROPAGATION DELAY

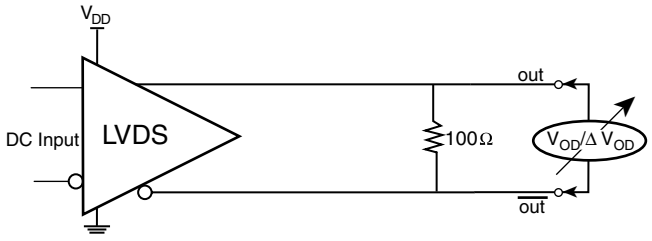


$$odc = \frac{t_{PW}}{t_{PERIOD}} \times 100\%$$

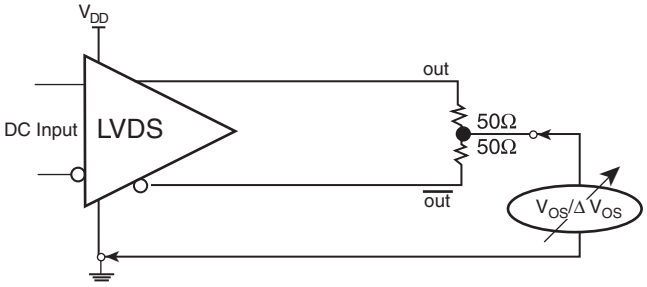
OUTPUT DUTY CYCLE/PULSE WIDTH/PERIOD



OUTPUT RISE/FALL TIME



DIFFERENTIAL OUTPUT VOLTAGE SETUP



OFFSET VOLTAGE SETUP

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APPLICATION INFORMATION

WIRING THE DIFFERENTIAL INPUT TO ACCEPT SINGLE ENDED LEVELS

Figure 1 shows how the differential input can be wired to accept single ended levels. The reference voltage V_REF ~ V_{DD}/2 is generated by the bias resistors R1, R2 and C1. This bias circuit should be located as close as possible to the input pin. The ratio of R1 and R2 might need to be adjusted to position the V_REF in the center of the input voltage swing. For example, if the input clock swing is only 2.5V and V_{DD} = 3.3V, V_REF should be 1.25V and R2/R1 = 0.609.

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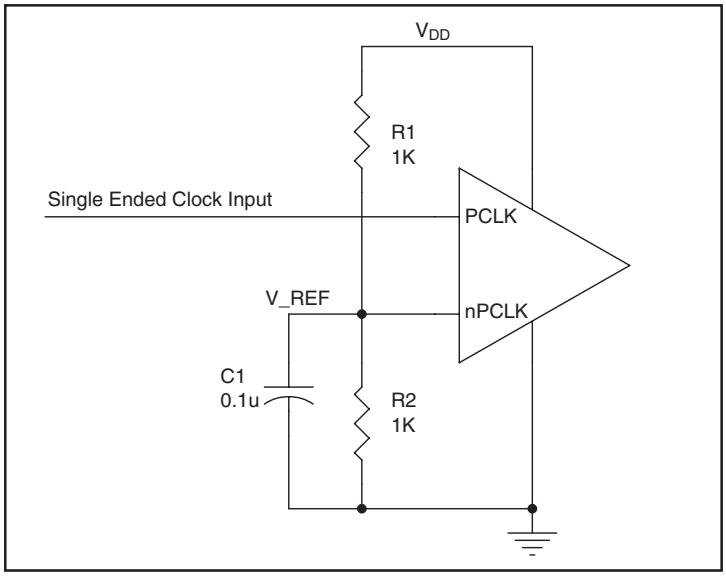

FIGURE 1. SINGLE ENDED SIGNAL DRIVING DIFFERENTIAL INPUT

RECOMMENDATIONS FOR UNUSED INPUT AND OUTPUT PINS

INPUTS:

PCLK/nPCLK INPUTS
For applications not requiring the use of the differential input, both PCLK and nPCLK can be left floating. Though not required, but for additional protection, a 1kΩ resistor can be tied from PCLK to ground.

OUTPUTS:

LVDS OUTPUTS
All unused LVDS output pairs can be either left floating or terminated with 100Ω across. If they are left floating, there should be no trace attached.

LVPECL OUTPUTS
All unused LVPECL outputs can be left floating. We recommend that there is no trace attached. Both sides of the differential output pair should either be left floating or terminated.

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LVPECL Clock Input Interface

The PCLK /nPCLK accepts LVPECL, LVDS, CML, SSTL and other differential signals. Both V_{SWING} and V_{OH} must meet the V_{PP} and V_{CMR} input requirements. *Figures 2A to 2F* show interface examples for the HiPerClockS PCLK/nPCLK input driven by the most common driver types. The input interfaces suggested here are examples only. If the driver is from another vendor, use their termination recommendation. Please consult with the vendor of the driver component to confirm the driver termination requirements.

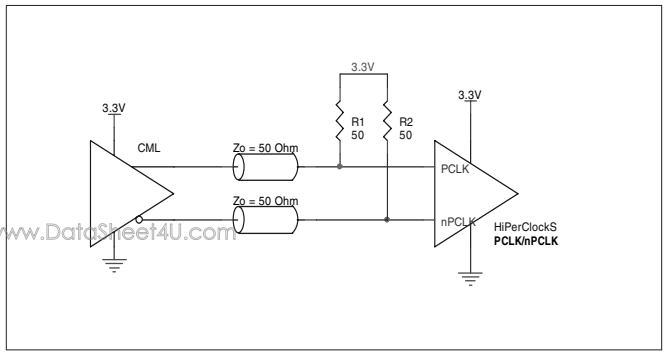

Figure 2A. HiPerClockS PCLK/nPCLK Input Driven By a CML Driver

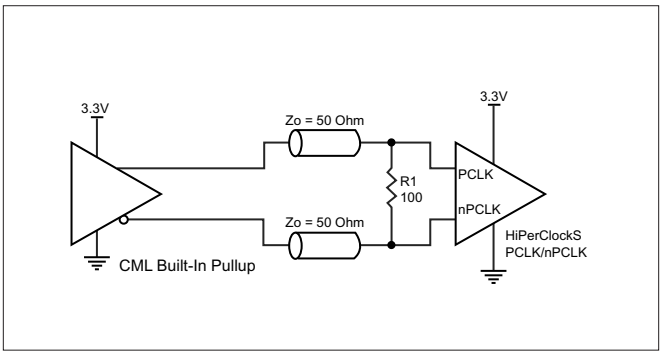

Figure 2B. HiPerClockS PCLK/nPCLK Input Driven By a Built-In Pullup CML Driver

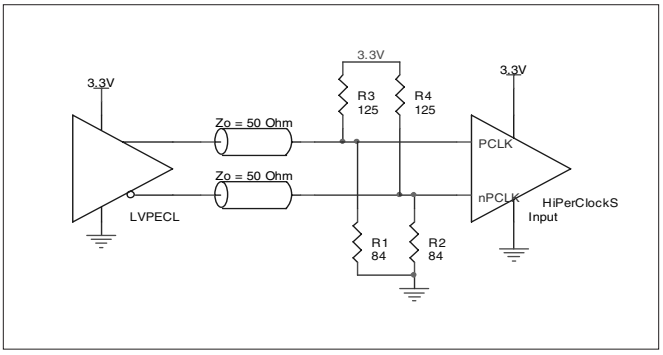

Figure 2C. HiPerClockS PCLK/nPCLK Input Driven By a 3.3V LVPECL Driver

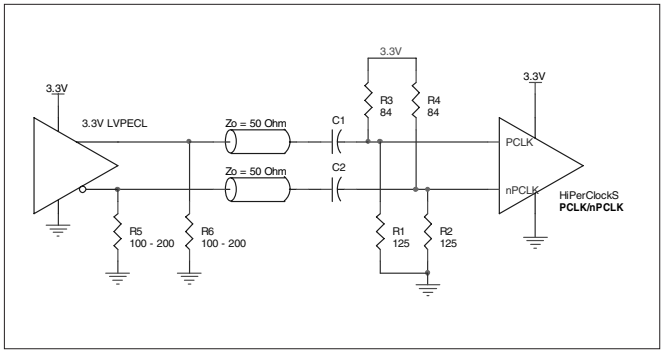

Figure 2D. HiPerClockS PCLK/nPCLK Input Driven By a 3.3V LVPECL Driver with AC Couple

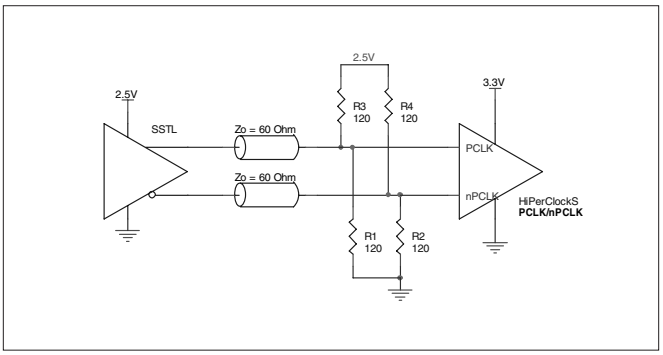

Figure 2E. HiPerClockS PCLK/nPCLK Input Driven By an SSTL Driver

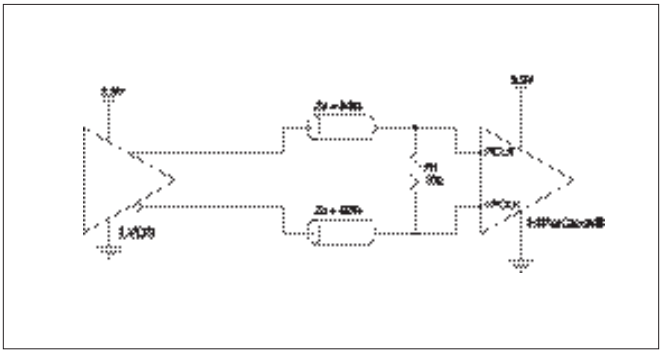

Figure 2F. HiPerClockS PCLK/nPCLK Input Driven By a 3.3V LVDS Driver

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3.3V, 2.5V LVDS Driver Termination

A general LVDS interface is shown in *Figure 3.* In a 100Ω differential transmission line environment, LVDS drivers require a matched load termination of 100Ω across near the receiver input. For a multiple LVDS outputs buffer, if only partial outputs are used, it is recommended to terminate the unused outputs.

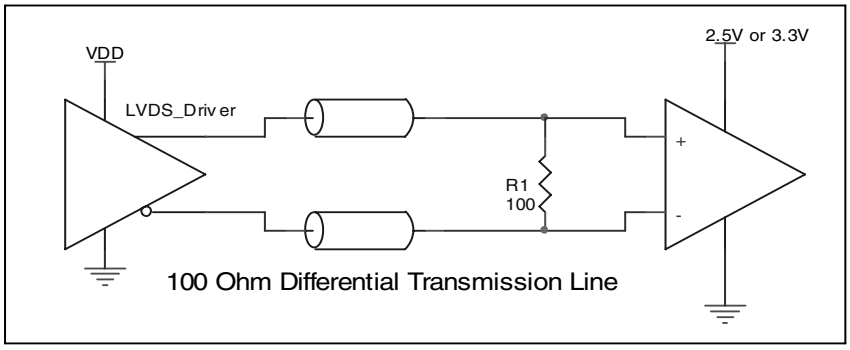

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Figure 3. Typical LVDS Driver Termination

Termination for 3.3V LVPECL Outputs

The clock layout topology shown below is a typical termination for LVPECL outputs. The two different layouts mentioned are recommended only as guidelines.

FOUT and nFOUT are low impedance follower outputs that generate ECL/LVPECL compatible outputs. Therefore, terminating resistors (DC current path to ground) or current sources must be used for functionality. These outputs are designed to drive 50Ω transmission lines. Matched impedance techniques should be used to maximize operating frequency and minimize signal distortion. *Figures 4A and 4B* show two different layouts which are recommended only as guidelines. Other suitable clock layouts may exist and it would be recommended that the board designers simulate to guarantee compatibility across all printed circuit and clock component process variations.

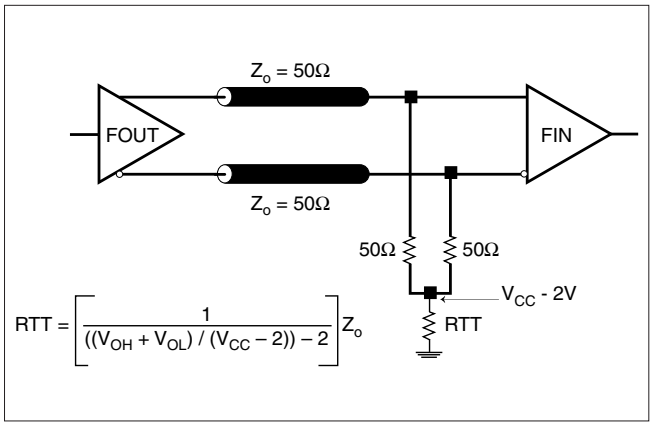

Figure 4A. LVPECL Output Termination

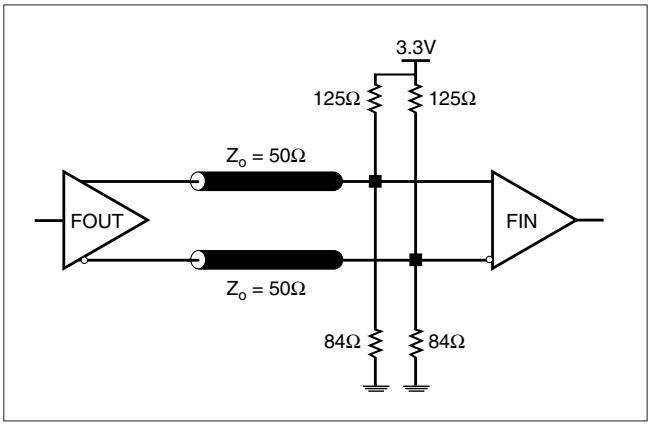

Figure 4B. LVPECL Output Termination

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TERMINATION FOR 2.5V LVPECL OUTPUTS

Figure 5A and *Figure 5B* show examples of termination for 2.5V LVPECL driver. These terminations are equivalent to terminating 50Ω to V_{DD} – 2V. For V_{DD} = 2.5V, the V_{DD} – 2V is very close to ground level. The R3 in Figure 5B can be eliminated and the termination is shown in *Figure 5C.*

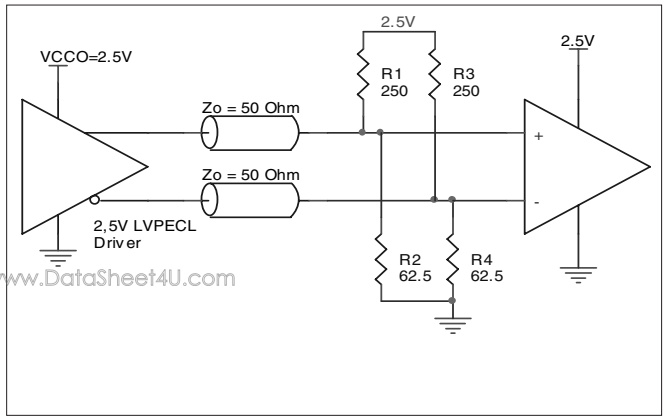

FIGURE 5A. 2.5V LVPECL DRIVER TERMINATION EXAMPLE

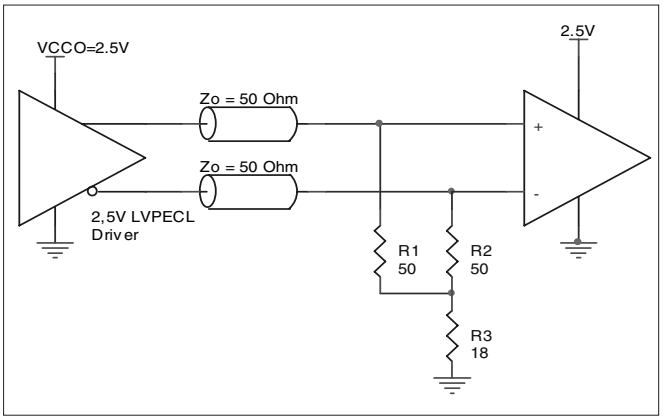

FIGURE 5B. 2.5V LVPECL DRIVER TERMINATION EXAMPLE

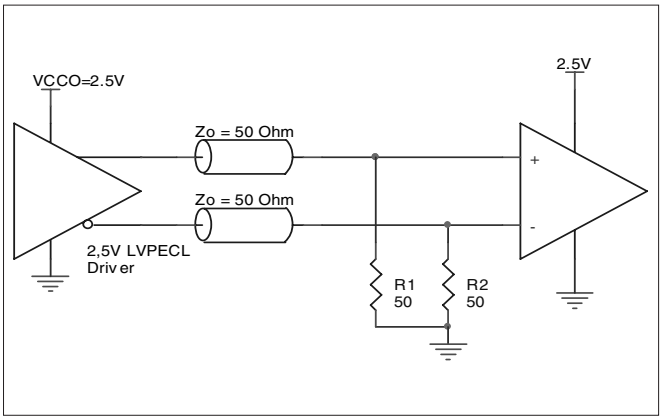

FIGURE 5C. 2.5V LVPECL TERMINATION EXAMPLE

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POWER CONSIDERATIONS (LVPECL OUTPUTS)

This section provides information on power dissipation and junction temperature for the ICS854S204I.
Equations and example calculations are also provided.

1. Power Dissipation.
The total power dissipation for the ICS854S204I is the sum of the core power plus the power dissipated in the load(s).
The following is the power dissipation for V_{DD} = 3.3V + 5% = 3.465V, which gives worst case results.
NOTE: Please refer to Section 3 for details on calculating power dissipated in the load.

- Power (core)$_{MAX}$ = V_{DD_MAX} * I_{DD_MAX} = 3.465V * 66mA = **228.69mW**
- Power (outputs)$_{MAX}$ = **32mW/Loaded Output pair**
  If all outputs are loaded, the total power is 4 * 32mW = **128mW**

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Total Power$_{_MAX}$ (3.465V, with all outputs switching) = 228.69mW + 128mW = **356.69mW**

2. Junction Temperature.
Junction temperature, Tj, is the temperature at the junction of the bond wire and bond pad and directly affects the reliability of the device. The maximum recommended junction temperature for HiPerClockS™ devices is 125°C.

The equation for Tj is as follows: $Tj = \theta_{JA} * Pd\_total + T_A$

Tj = Junction Temperature

θ_{JA} = Junction-to-Ambient Thermal Resistance

Pd_total = Total Device Power Dissipation (example calculation is in section 1 above)

T_A = Ambient Temperature

In order to calculate junction temperature, the appropriate junction-to-ambient thermal resistance θ_{JA} must be used. Assuming no air flow and a multi-layer board, the appropriate value is 92°C/W per Table 6A below.

Therefore, Tj for an ambient temperature of 85°C with all outputs switching is:
85°C + 0.357W * 92°C/W = 117.8°C. This is below the limit of 125°C.

TABLE 6A. THERMAL RESISTANCE θ_{JA} FOR 16-LEAD TSSOP, FORCED CONVECTION

θ_{JA} by Velocity (Meters per Second)			
	0	**1**	**2.5**
Multi-Layer PCB, JEDEC Standard Test Boards	92°C/W	87.6°C/W	85.5°C/W

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3. Calculations and Equations.

The purpose of this section is to derive the power dissipated into the load.

LVPECL output driver circuit and termination are shown in *Figure 6.*

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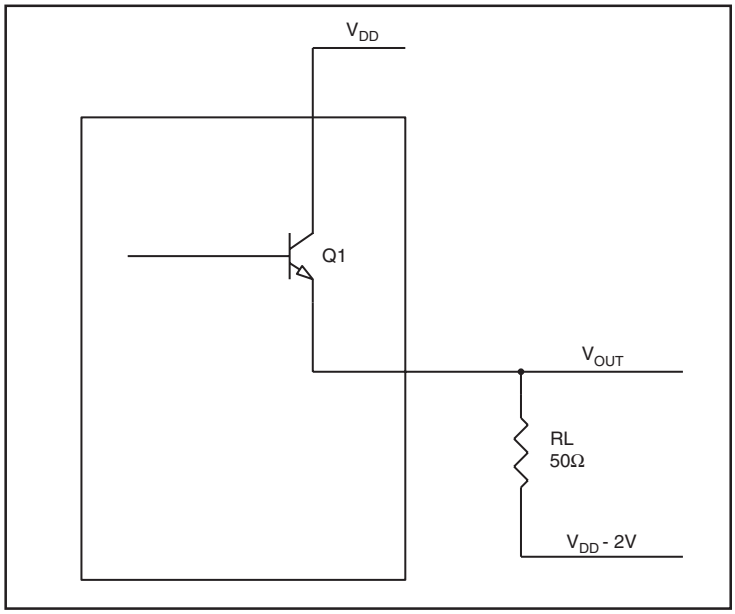

FIGURE 6. LVPECL DRIVER CIRCUIT AND TERMINATION

To calculate worst case power dissipation into the load, use the following equations which assume a 50Ω load, and a termination voltage of V_{DD} – 2V.

- For logic high, $V_{OUT} = V_{OH\_MAX} = \mathbf{V_{DD\_MAX} – 0.8V}$

  $(V_{DD\_MAX} – V_{OH\_MAX}) = \mathbf{0.8V}$

- For logic low, $V_{OUT} = V_{OL\_MAX} = \mathbf{V_{DD\_MAX} – 1.6V}$

  $(V_{DD\_MAX} – V_{OL\_MAX}) = \mathbf{1.6V}$

Pd_H is power dissipation when the output drives high.
Pd_L is the power dissipation when the output drives low.

$Pd\_H = [(V_{OH\_MAX} – (V_{DD\_MAX} – 2V))/R_L] * (V_{DD\_MAX} – V_{OH\_MAX}) = [(2V – (V_{DD\_MAX} – V_{OH\_MAX}))/R_L] * (V_{DD\_MAX} – V_{OH\_MAX}) =$
$[(2V – 0.8V)/50\Omega] * 0.8V =$ **19.2mW**

$Pd\_L = [(V_{OL\_MAX} – (V_{DD\_MAX} – 2V))/R_L] * (V_{DD\_MAX} – V_{OL\_MAX}) = [(2V – (V_{DD\_MAX} – V_{OL\_MAX}))/R_L] * (V_{DD\_MAX} – V_{OL\_MAX}) =$
$[(2V – 1.6V)/50\Omega] * 1.6V =$ **12.8mW**

Total Power Dissipation per output pair = Pd_H + Pd_L = **32mW**

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POWER CONSIDERATIONS (LVDS OUTPUTS)

This section provides information on power dissipation and junction temperature for the ICS854S204I.
Equations and example calculations are also provided.

1. Power Dissipation.
The total power dissipation for the ICS854S204I is the sum of the core power plus the power dissipated in the load(s).
The following is the power dissipation for V_{DD} = 3.3V + 5% = 3.465V, which gives worst case results.

- Power$_{_MAX}$ = V_{DD_MAX} * I_{DD_MAX} = 3.465V * 120mA = **415.8mW**

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2. Junction Temperature.
Junction temperature, Tj, is the temperature at the junction of the bond wire and bond pad and directly affects the reliability of the device. The maximum recommended junction temperature for HiPerClockS™ devices is 125°C.

The equation for Tj is as follows: $Tj = \theta_{JA} * Pd\_total + T_A$

Tj = Junction Temperature

θ_{JA} = Junction-to-Ambient Thermal Resistance

Pd_total = Total Device Power Dissipation (example calculation is in section 1 above)

T_A = Ambient Temperature

In order to calculate junction temperature, the appropriate junction-to-ambient thermal resistance θ_{JA} must be used. Assuming no air flow and a multi-layer board, the appropriate value is 92°C/W per Table 6B below.

Therefore, Tj for an ambient temperature of 85°C with all outputs switching is:

85°C + 0.416W * 92°C/W = 123.3°C. This is below the limit of 125°C.

TABLE 6B. THERMAL RESISTANCE θ_{JA} FOR 16-LEAD TSSOP, FORCED CONVECTION

θ_{JA} by Velocity (Meters per Second)			
	0	**1**	**2.5**
Multi-Layer PCB, JEDEC Standard Test Boards	92°C/W	87.6°C/W	85.5°C/W

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Reliability Information

Table 7. θ_{JA} vs. Air Flow Table for 16 Lead TSSOP

θ_{JA} by Velocity (Meters per Second)			
	0	**1**	**2.5**
Multi-Layer PCB, JEDEC Standard Test Boards	92°C/W	87.6°C/W	85.5°C/W

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Transistor Count

The transistor count for ICS854S204I is: 454

Package Outline and Dimensions

Package Outline - G Suffix for 16 Lead TSSOP

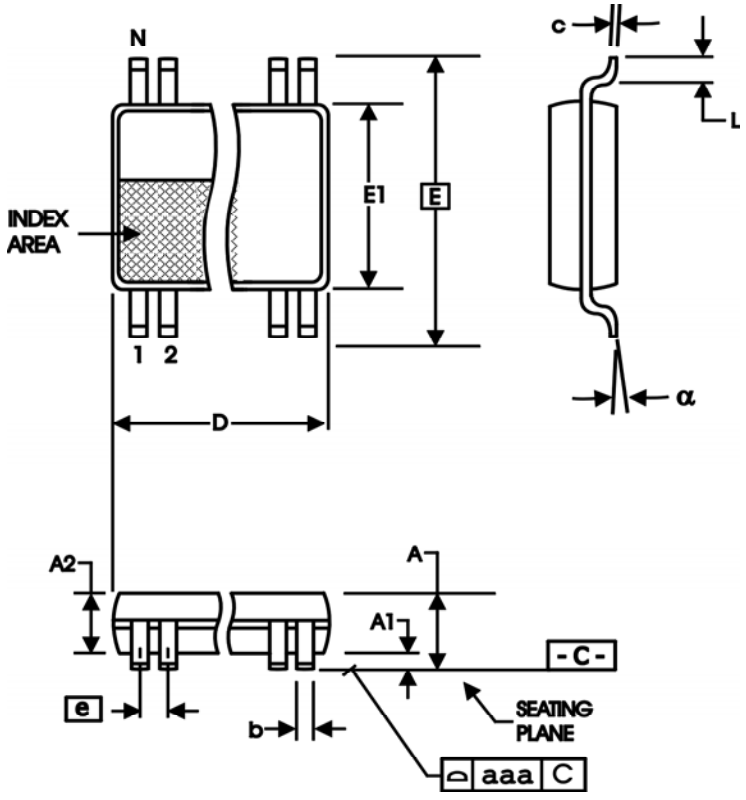

Table 8. Package Dimensions

SYMBOL	Millimeters	
	Minimum	Maximum
N	16	
A	--	1.20
A1	0.05	0.15
A2	0.80	1.05
b	0.19	0.30
c	0.09	0.20
D	4.90	5.10
E	6.40 BASIC	
E1	4.30	4.50
e	0.65 BASIC	
L	0.45	0.75
α	0°	8°
aaa	--	0.10

Reference Document: JEDEC Publication 95, MO-153

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TABLE 8. ORDERING INFORMATION

Part/Order Number	Marking	Package	Shipping Packaging	Temperature
ICS854S204BGILF	4S204BIL	16 lead "Lead-Free" TSSOP	tube	-40°C to 85°C
ICS854S204BGILFT	4S204BIL	16 lead "Lead-Free" TSSOP	2500 tape & reel	-40°C to 85°C

NOTE: Parts that are ordered with an "LF" suffix to the part number are the Pb-Free configuration and are RoHS compliant.

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