



PRELIMINARY

SOLID STATE DEVICES, INC

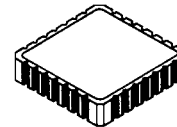
14849 Firestone Boulevard · La Mirada, CA 90638
 Phone: (714) 670-SSDI (7734) · Fax: (714) 522-7424

Designer's Data Sheet**FEATURES:**

- Rugged construction with poly silicon gate
- Low RDS(on) and high transconductance
- Excellent high temperature stability
- Very fast switching speed
- Fast recovery and superior dv/dt performance
- Increased reverse energy capability
- Low input and transfer capacitance for easy paralleling
- Hermetically sealed surface mount package
- TX, TXV and Space Level screening available
- Replaces: IRF340 Types

SFF340-28

**10 AMP
 400 VOLTS
 0.58Ω
 N-CHANNEL
 POWER MOSFET**

28 PIN CLCC**MAXIMUM RATINGS**

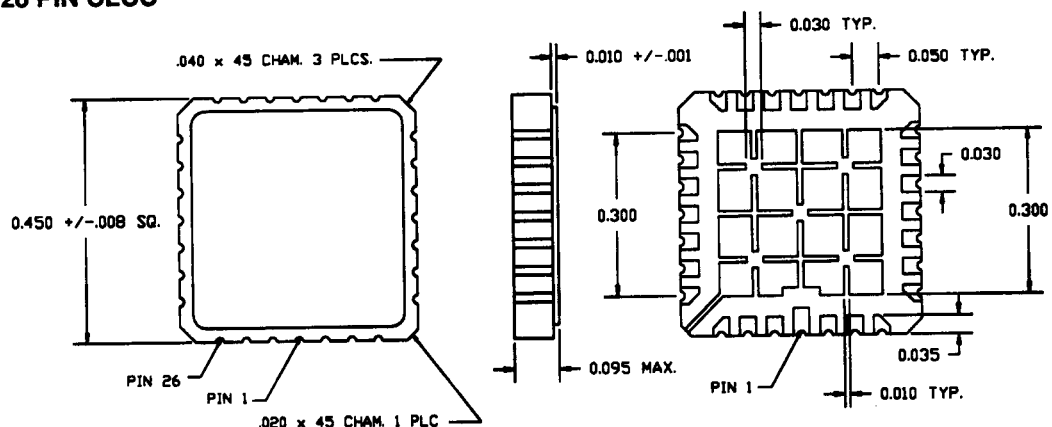
CHARACTERISTIC	SYMBOL	VALUE	UNIT
Drain to Source Voltage	V _{DS}	400	Volts
Gate to Source Voltage	V _{GS}	±20	Volts
Continuous Drain Current	I _D	10*	Amps
Operating and Storage Temperature	Top & Tstg	-55 to +150	°C
Thermal Resistance, Junction to Case	RθJC	3.5	°C/W
Total Device Dissipation @ TC=25°C Total Device Dissipation @ TC=80°C	P _D	36 27	Watts

PACKAGE OUTLINE: 28 PIN CLCC

PIN OUT:
SOURCE: 1, 15-28
DRAIN: 5-11
GATE: 2, 3, 13, 14

NOTE:

All Drain/Source Pins must be connected on the PC Board in order to maximize current capability and minimize RDS(on)



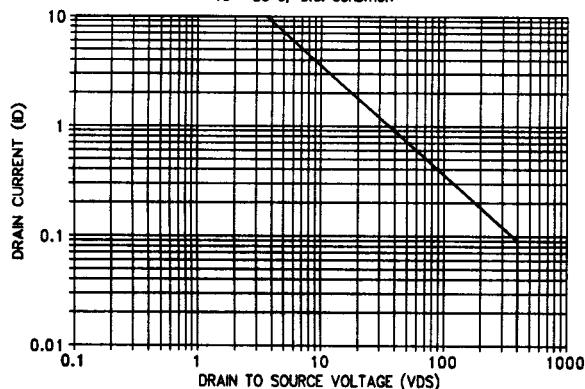
* Rating based on size of chip. Device rating may vary depending on mounting and heatsink conditions. Consult SSDI Marketing department for thermal derating details.

NOTE: All specifications are subject to change without notification. SCD's for these devices should be reviewed by SSDI prior to release.

DATA SHEET #: F00073 A**MED**

SFF340-28
 14849 Firestone Boulevard · La Mirada, CA 90638
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ELECTRICAL CHARACTERISTICS @ T_J=25 °C (Unless Otherwise Specified)

RATING		SYMBOL	MIN	TYP	MAX	UNIT
Drain to Source Breakdown Voltage (V _{GS} =0 V, I _D =250μA)		BV_{DSS}	400	---	---	V
Drain to Source on State Resistance (V _{GS} =10 V, I _D =60% Rated I _D)		R_{DS(on)}	---	0.42	0.58**	Ω
On State Drain Current (V _{DS} > I _{D(on)} X R _{DS(on)} Max, V _{GS} =10 V)		I_{D(on)}	10*	---	---	A
Gate Threshold Voltage (V _{DS} =V _{GS} , I _D =250μA)		V_{GS(th)}	2.0	---	4.0	V
Forward Transconductance (V _{DS} ≥ 50V, I _{DS} =60% rated I _D)		g_{fs}	5.8	8.7	---	S(Ω)
Zero Gate Voltage Drain Current (V _{DS} =max rated voltage, V _{GS} =0 V) (V _{DS} =80% rated V _{DS} , V _{GS} =0 V, T _A =125°C)		I_{DSS}	---	---	250 1000	μA
Gate to Source Leakage Forward Gate to Source Leakage Reverse	At rated V _{GS}	I_{GSS}	---	---	100 -100	nA
Total Gate Charge Gate to Source Charge Gate to Drain Charge	V _{GS} =10 Volts 80% rated V _{DS} I _D =10A	Q_g Q_{gs} Q_{gd}	---	43 6 22	65 9.3 33	nC
Turn on Delay Time Rise Time Turn Off Delay Time Fall Time	V _{DD} =50% rated V _{DS} I _D =10A R _G =9.1Ω R _D =20Ω	t_{d(on)} t_r t_{d(off)} t_f	---	14 27 50 24	9 30 74 36	nsec
Diode Forward Voltage (I _S =rated I _D , V _{GS} =0 V, T _J =25°C)		V_{SD}	---	---	2.0	V
Diode Reverse Recovery Time Reverse Recovery Charge	T _J =25°C I _F =rated I _D di/dt=100 A/μsec	t_{rr} Q_{RR}	170 1.6	370 3.8	790 8.2	nsec μC
Input Capacitance Output Capacitance Reverse Transfer Capacitance	V _{GS} =0 Volts V _{DS} =25 Volts f=1 MHz	C_{iss} C_{oss} C_{rss}	---	1300 210 37	---	pF

 SAFE OPERATING AREA (S.O.A.)
 T_C = 25 °C, D.C. CONDITION
**NOTES:**

* Rating based on size of chip. Device rating may vary depending on mounting and heatsink conditions. Consult SSDI Marketing department for thermal derating details.

** Due to package resistance; all Source/Drain pins must be connected on the PC Board in order to obtain the lowest R_{DS(on)} possible.