

Solid State Devices, Inc.

14830 Valley View Blvd * La Mirada, Ca 90638

Phone: (562) 404-7855 * Fax: (562) 404-1773

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DESIGNER'S DATA SHEET

Part Number / Ordering Information ^{1/}

SFF24N50

+ Screening ^{2/} ___ = Not Screen
 TX = TX Level
 TXV = TXV Level
 S = S Level
 + Lead Option ^{3/} ___ = Straight Leads
 DB = Down Bend
 UB = Up Bend
 + Package ^{3/} M = TO-254
 Z = TO-254Z

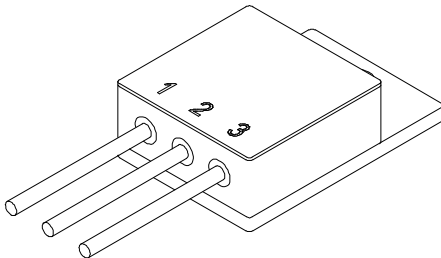
SFF24N50M
SFF24N50Z
24 AMP / 500 Volts
0.2 W
N-Channel MOSFET

Features:

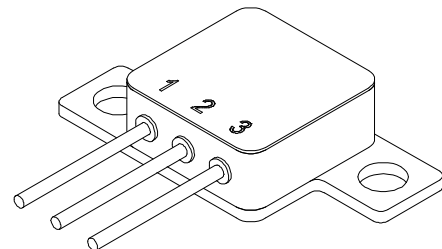
- Rugged Construction with Polysilicon Gate Cell
- Low $R_{DS(ON)}$ and High Transconductance
- Excellent High Temperature Stability
- Very Fast Switching Speed
- Fast Recovery and Superior dV/dt Performance
- Increased Reverse Energy Capability
- Low Input and Transfer Capacitance for Easy Paralleling
- Ceramic Seals for Improved Hermeticity
- Hermetically Sealed Surface Mount Power Package
- TX, TXV, Space Level Screening Available
- Replacement for IXTH24N50 Types

Maximum Ratings		Symbol	Value	Units
Drain – Source Voltage		V_{DS}	500	Volts
Gate – Source Voltage		V_{GS}	± 20	Volts
Continuous Collector Current		I_D	24	Amps
Avalanche Current	Repetitive	I_{AR}	21	Amps
Avalanche Energy	Repetitive Single Pulse	E_{AR} E_{AS}	1 690	mJ
Power Dissipation	$T_C = 25^\circ C$ $T_C = 55^\circ C$	P_D	150 114	W
Operating & Storage Temperature		Top & Tstg	-55 to +150	$^\circ C$
Maximum Thermal Resistance Junction to Case		R_{qJC}	0.83	$^\circ C/W$

TO-254 (M)



TO-254Z (Z)



NOTE: All specifications are subject to change without notification.
 SCD's for these devices should be reviewed by SSDI prior to release.

DATA SHEET #: F00165F

DOC


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SFF24N50M **SFF24N50Z**

Electrical Characteristics @ T _J = 25°C (Unless Otherwise Specified)		Symbol	Min	Typ	Max	Units
Drain to Source Breakdown Voltage (VGS=0 V, ID=250 μA)		BV _{DSS}	500	—	—	Volts
Drain to Source On State Resistance (VGS=10 V, ID=50% Rated ID)		R _{DS(on)}	—	—	0.2	W
On State Drain Current (VDS>ID(on) X RDS(on) Max, VGS=10V)		I _{D(on)}	24	—	—	A
Gate Threshold Voltage (VDS=VGS, ID= 4mA)		V _{GS(th)}	2.0	—	4.0	V
Forward Transconductance (VDS>ID(on) X RDS(on) Max, IDS= 50% Rated ID)		g _{fs}	8	12	—	mho
Zero Gate Voltage Drain Current (VDS=max rated voltage, VGS=0 V) (VDS=80% rated VDS, VGS=0 V, TA=125°C)		I _{DSS}	— —	— —	250 1000	mA
Gate to Source Leakage Forward Gate to Source Leakage Reverse	At rated VGS	I _{GSS}	— —	— —	+100 -100	nA
Total Gate Charge Gate to Source Charge Gate to Drain Charge	VGS=10 Volts 50% rated VDS 50% Rated ID	Q _g Q _{gs} Q _{gd}	— — —	135 28 62	180 40 85	nC
Turn on Delay Time Rise Time Turn on Delay Time Fall Time	VDD=50% Rated VDS 50% Rated ID RG= 6.2Ω VGS=10 Volts	td(on) tr td(off) tf	— — — —	16 33 65 30	30 45 130 40	nsec
Diode Forward Voltage (IS= Rated ID, VGS=0 V, TJ=25°C)		V _{SD}	—	—	1.5	V
Diode Reverse Recovery Time Reverse Recovery Charge	T _J =25°C IF=10A Di/dt=100A/μsec	t _{rr} Q _{RR}	— —	— —	500 —	nsec nC
Input Capacitance Input Capacitance Reverse Transfer Capacitance	VGS=0 Volts VDS=25 Volts f=1 MHz	C _{iss} C _{oss} C _{rss}	— — —	4200 450 135	— — —	pF

For thermal derating curves and other characteristics please contact SSDI Marketing Department.

Available Part Numbers:
SFF24N50M; SFF24N50MDB; SFF24N50MUB;
SFF24N50Z; SFF24N50ZDB; SFF24N50ZUB;
PIN ASSIGNMENT (Standard)

Package	Drain	Source	Gate
TO-254 (M)	Pin 1	Pin 2	Pin 3
TO-254Z (Z)	Pin 1	Pin 2	Pin 3

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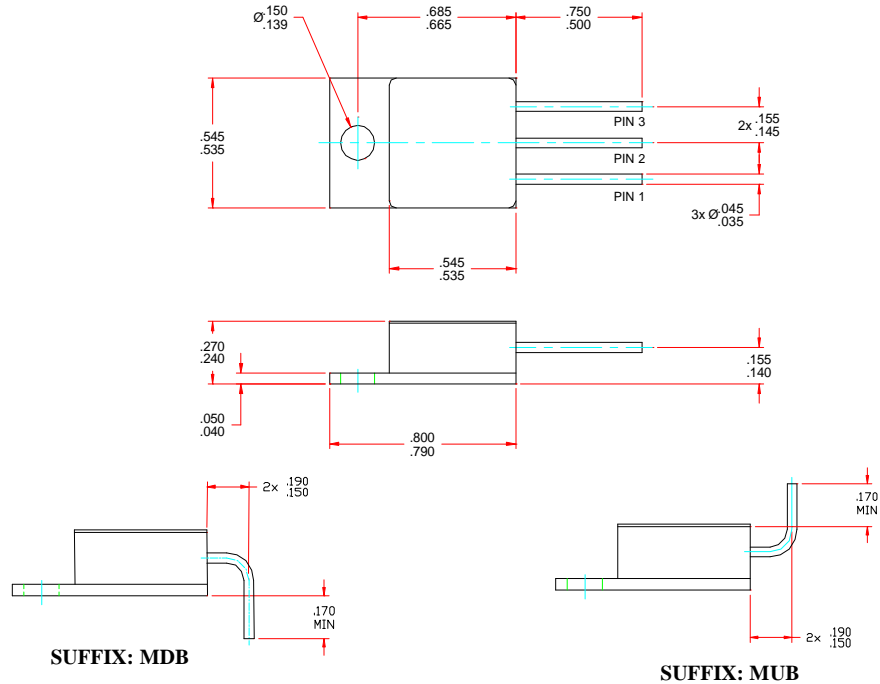
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SFF24N50M
SFF24N50Z
Case Outline: TO-254 (M)

Case Outline: TO-254Z (Z)
