

**MICRO MINI**
**T0805BM –  
T0805MM TRIACS**
**8.0A 200–600 V  
5/5/5/5 mA**

The T0805 series TRIAC's are high performance glass passivated PNPN devices. These parts are intended for hybrid applications.

**Absolute Maximum Ratings**  $T_A = 25^\circ\text{C}$  unless otherwise noted

Parameter	Part Nr.	Symbol	Min.	Max.	Unit	Test Conditions
Repetitive Peak Off State Voltage	<b>T0805BM</b>	$V_{DRM}$ $V_{RRM}$	200		V	$T_j = -40^\circ\text{C}$ to $125^\circ\text{C}$ $R_{GK} = 1\text{K}\Omega$
	<b>T0805DM</b>		400		V	
	<b>T0805MM</b>		600		V	
On-State Current		$I_{T(RMS)}$	8		A	All Conduction Angles $T_C = 85^\circ\text{C}$
Nonrept. On-State Current		$I_{TSM}$	77		A	Half Cycle, 60 Hz
Nonrept. On-State Current		$I_{TSM}$	70		A	Half Cycle, 50 Hz
Fusing Current		$I_{\text{ft}}$	24		$\text{A}^2\text{s}$	$t = 10\text{ ms}$
Peak Gate Current		$I_{GM}$	4		A	$10\mu\text{s}$ max.
Peak Gate Dissipation		$P_{GM}$	10		W	$10\mu\text{s}$ max.
Gate Dissipation		$P_{G(AV)}$	1		W	20 ms max.
Operating Temperature		$T_j$	$-40$	$125$	$^\circ\text{C}$	
Storage Temperature		$T_{stg}$	$-40$	$150$	$^\circ\text{C}$	
Case Temperature		$T_C$			$^\circ\text{C}$	Temperature measured on the substrate immediately adjacent to the Chip

**Electrical Characteristics**  $T_A = 25^\circ\text{C}$  unless otherwise noted

Parameter	Symbol	Min.	Max.	Unit	Test Conditions
Off-State Leakage Current	$I_{DRM}/I_{RRM}$		2	mA	@ $V_{DRM} + V_{RRM}$ , $R_{GK} = 1\text{K}\Omega$ , $T_j = 125^\circ\text{C}$
Off-State Leakage Current	$I_{DRM}/I_{RRM}$		5	$\mu\text{A}$	@ $V_{DRM} + V_{RRM}$ , $R_{GK} = 1\text{K}\Omega$ , $T_j = 25^\circ\text{C}$
On-State Voltage	$V_T$		1.85	V	at $I_T = 12\text{ A}$ , $T_j = 25^\circ\text{C}$
On-State Threshold Voltage	$V_{T(TO)}$		1.0	V	$T_j = 125^\circ\text{C}$
On-State Slope Resistance	$r_T$		80	m $\Omega$	$T_j = 125^\circ\text{C}$
Gate Trigger Current	$I_{GT} \text{ I} + (1)$		5	mA	$V_D = 12\text{ V}$
Gate Trigger Current	$I_{GT} \text{ I} - (2)$		5	mA	$V_D = 12\text{ V}$
Gate Trigger Current	$I_{GT} \text{ III} - (3)$		5	mA	$V_D = 12\text{ V}$
Gate Trigger Current	$I_{GT} \text{ III} + (4)$		5	mA	$V_D = 12\text{ V}$
Gate Trigger Voltage	$V_{GT}$		2.5	V	$V_D = 12\text{ V}$ , All Quadrants
Holding Current	$I_H$		5	mA	$R_{GK} = 1\text{K}\Omega$
Critical Rate of Voltage Rise	$dv/dt$	10		V/ $\mu\text{s}$	$V_D = .67 \times V_{DRM}$ , $R_{GK} = 1\text{K}\Omega$ , $T_j = 125^\circ\text{C}$
Critical Rate of Rise, Off-State	$dv/dt_c$	1		V/ $\mu\text{s}$	$I_T = 8\text{ A}$ , $di/dt = 3.55\text{ A/ms}$ , $T_j = 85^\circ\text{C}$
Thermal Resistance junc. to case	$R_{\theta jc}$		1.2	K/W	50 micron solder on backside of Chip

Parts are 100% tested in Chip form with visual inspection after assembly.

Per MIL-STD-105-D, parts will pass AQL 4.0 income inspection.