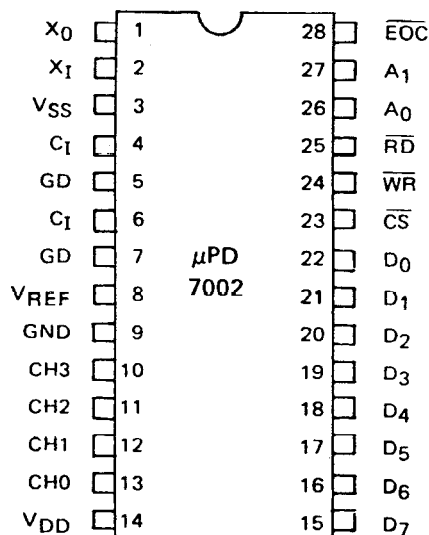


## 12-BIT BINARY A/D CONVERTER

**DESCRIPTION** The μPD7002 is a high performance, low power, monolithic CMOS A/D converter designed for microprocessor applications. The analog input voltage is applied to one of the four analog inputs. By loading the input register with the multiplexer channel and the desired resolution (8 or 12 bits) the integrating A/D conversion sequence is started. At the end of conversion  $\overline{EOC}$  signal goes low and if connected to the interrupt line of microprocessor it will cause an interrupt. At this point the digital data can be read in two bytes from the output registers. The μPD7002 also features a status register that can be read at any time.

- FEATURES**
- Single Chip CMOS LSI
  - Resolution: 8 or 12 Bits
  - 4 Channel Analog Multiplexer
  - Auto-Zeroscale and Auto-Fullscale Corrections without any External Components
  - High Input Impedance: 1000MΩ
  - Readout of Internal Status Register Through Data Bus
  - Single +5V Power Supply
  - Interfaces to Most 8-Bit Microprocessors
  - Conversion Speed: 5 ms
  - Power Consumption: 20 mW
  - Available in a 28 Pin Plastic Package

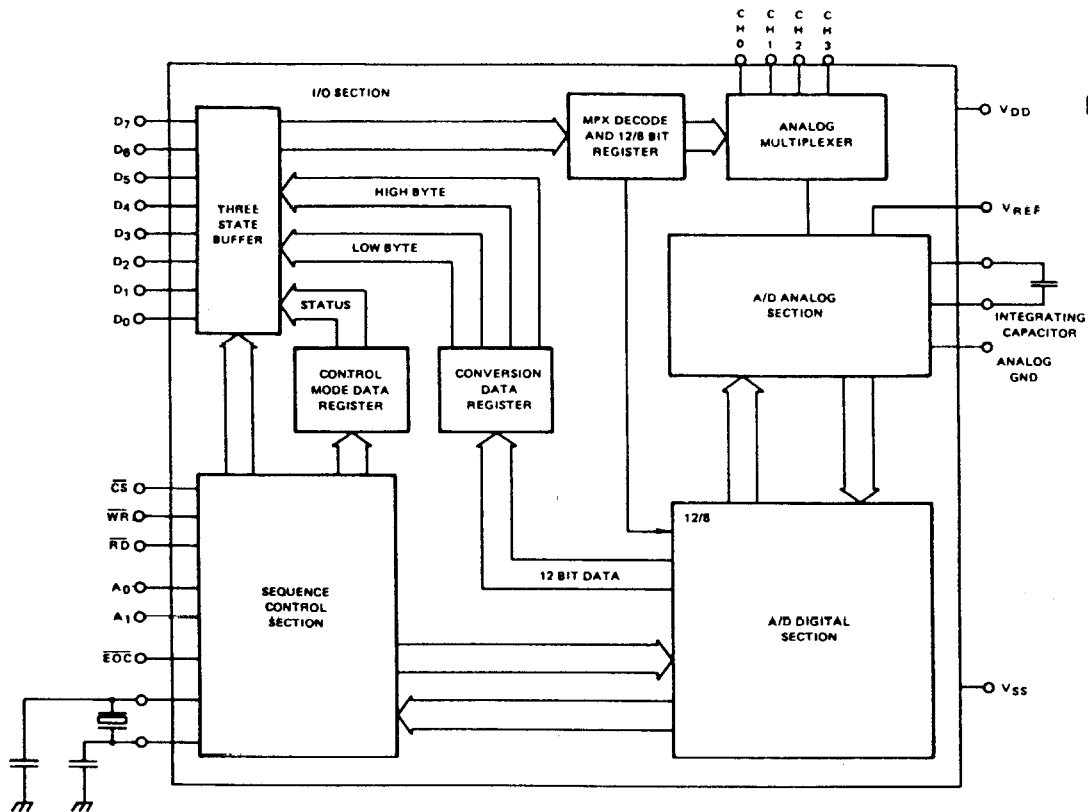
### PIN CONFIGURATION



### PIN NAMES

X0, XI	External Clock Input
VSS	TTL Ground
CI	Integrating Capacitor
GD	Guard
VREF	Reference Voltage Input
GND	Analog Ground
CH3	Analog Channel 3
CH2	Analog Channel 2
CH1	Analog Channel 1
CH0	Analog Channel 0
VDD	TTL Voltage (+5V)
D0-D7	Data Bus
CS	Chip Select
WR, RD	Control Bus
A0, A1	Address Bus
EOC	End of Conversion Interrupt

BLOCK DIAGRAM



## DC CHARACTERISTICS

$T_a = 25 \pm 2^\circ\text{C}$ ;  $V_{DD} = +5 \pm 0.25\text{V}$ ,  $V_{REF} = +2.50\text{V}$ ,  $f_{CK} = 1\text{ MHz}$

PARAMETER	SYMBOL	LIMITS			UNIT	TEST CONDITIONS
		MIN	TYP	MAX		
Resolution			12		Bits	$V_{DD} = 5\text{V}$ , $V_{REF} = 2.5 \pm 0.25\text{V}$
Non Linearity			0.05	0.08	%FSR	$V_{DD} = 5\text{V}$ , $V_{REF} = 2.5 \pm 0.25\text{V}$
Fullscale Error			0.05	0.08	%FSR	$V_{DD} = 5\text{V}$ , $V_{REF} = 2.5 \pm 0.25\text{V}$
Zeroscale Error			0.05	0.08	%FSR	$V_{DD} = 5\text{V}$ , $V_{REF} = 2.5 \pm 0.25\text{V}$
Fullscale Temperature Coefficient			10		PPM/ $^\circ\text{C}$	$V_{DD} = 5\text{V}$
Zeroscale Temperature Coefficient			10		PPM/ $^\circ\text{C}$	$V_{DD} = 5\text{V}$
Analog Input Voltage Range	$V_{IA}$	0		$V_{REF}$	V	
Analog Input Resistance	$R_{IA}$		1000		M $\Omega$	$V_{IA} = V_{SS}$ to $V_{DD}$
Total Unadjusted Error 1	T.U.E. 1		0.05	0.08	%FSR	$V_{REF} = 2.25$ to $2.75\text{V}$ , $V_{DD} = 5\text{V}$
Total Unadjusted Error 2	T.U.E. 2		0.05	0.08	%FSR	$V_{REF} = 2.5\text{V}$ , $V_{DD} = 4.75$ to $5.25\text{V}$
Clock Input Current	$I_{XI}$		5	50	$\mu\text{A}$	
Clock Input High Level	$V_{XIH}$	$V_{DD}-1.4$			V	
Clock Input Low Level	$V_{XIL}$			$V_{SS}+1.4$	V	
High Level Input Voltage	$V_{IH}$	2.2			V	$T_a = -20^\circ\text{C}$ to $+70^\circ\text{C}$
Low Level Input Voltage	$V_{IL}$			0.8	V	$T_a = -20^\circ\text{C}$ to $+70^\circ\text{C}$
High Level Output Voltage	$V_{OH}$	3.5			V	$I_O = -1.6\text{ mA}$ $T_a = -20^\circ\text{C}$ to $+70^\circ\text{C}$
Low Level Output Voltage	$V_{OL}$			0.4	V	$I_O = +16\text{ mA}$ $T_a = -20^\circ\text{C}$ to $+70^\circ\text{C}$
Digital Input Leakage Current	$I_{I}$		1	10	$\mu\text{A}$	$V_I = V_{SS}$ to $V_{DD}$
High-Z Output Leakage Current	$I_{Leak}$		1	10	$\mu\text{A}$	$V_O = V_{SS}$ to $V_{DD}$
Power Dissipation	$P_d$		15	25	mW	$f_{CK} < 1\text{ MHz}$

# **μPD7002**

## **ABSOLUTE MAXIMUM RATINGS\***

Operating Temperature	-20°C to +70°C
Storage Temperature	-65°C to +125°C
All Input Voltages	-0.3 to $V_{DD} + 0.3$ Volts
Power Supply	-0.3 to +7 Volts
Power Dissipation	300 mW
Analog GND Voltage	$V_{SS} \pm 0.3$ Volts

COMMENT: Stress above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

\* $T_a = 25^\circ\text{C}$

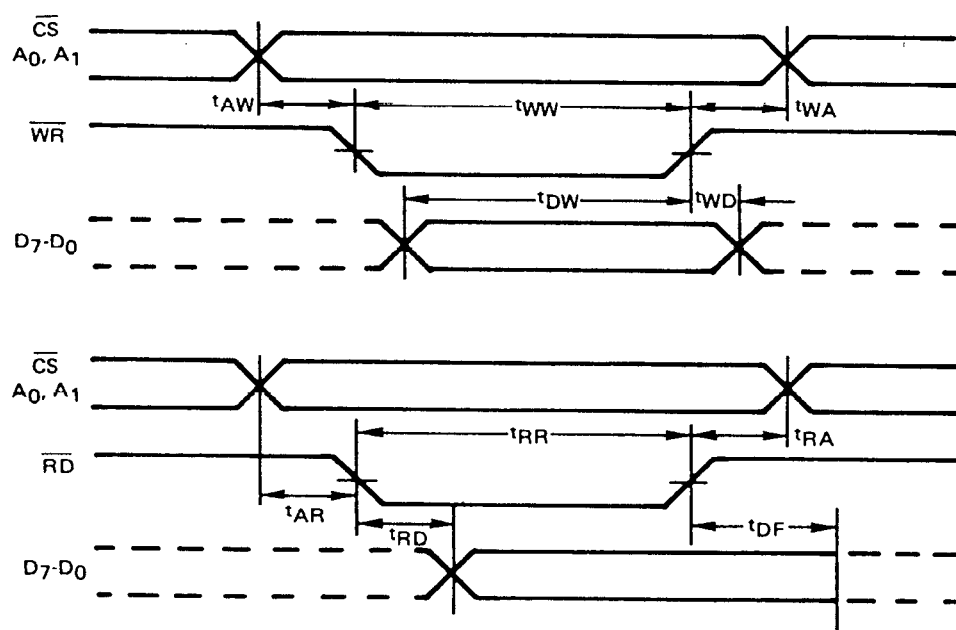
## **AC CHARACTERISTICS**

$T_a = 25^\circ \pm 2^\circ\text{C}$ ;  $V_{DD} = +5 \pm 0.25\text{V}$ ;  $V_{REF} = 2.5\text{V}$ ;  $f_{CK} = 1\text{ MHz}$ ;  $C_{INT} = 0.033\text{ }\mu\text{F}$

PARAMETER	SYMBOL	LIMITS			UNIT	TEST CONDITIONS
		MIN	TYP	MAX		
Conversion Speed (12 bit)	$t_{CONV}$	8.5	10	15	ms	$f_{CK} = 1\text{ MHz}$
Conversion Speed (8 bit)	$t_{CONV}$	2.4	4	5	ms	$f_{CK} = 1\text{ MHz}$
Clock Frequency Range	$f_{CK}$	0.1	1	3	MHz	
Integrating Capacitor Value	$C_{INT}^*$	0.029			$\mu\text{F}$	$V_{REF} = 2.50\text{V}$ , $f_{CK} = 1\text{ MHz}$
Address Setup Time $\overline{CS}$ , $A_0$ , $A_1$ , to $\overline{WR}$	$t_{AW}$	50			ns	
Address Setup Time $\overline{CS}$ , $A_0$ , $A_1$ , to $\overline{RD}$	$t_{AR}$	50			ns	
Address Hold Time $\overline{WR}$ to $\overline{CS}$ , $A_0$ , $A_1$	$t_{WA}$	50			ns	
Address Hold Time $\overline{RD}$ to $\overline{CS}$ , $A_0$ , $A_1$	$t_{RA}$	50			ns	
Low Level $\overline{WR}$ Pulse Width	$t_{WW}$	400			ns	
Low Level $\overline{RD}$ Pulse Width	$t_{RR}$	400			ns	
Data Setup Time Input Data to $\overline{WR}$	$t_{DW}$	300			ns	
Data Hold Time $\overline{WR}$ to Input Data	$t_{WD}$	50			ns	
Output Delay Time $\overline{RD}$ to Output Data	$t_{RD}$			300	ns	1TTL + 100 pF
Delay Time to High Z Output $\overline{RD}$ to Floating Output	$t_{DF}$			150	ns	

\*  $C_{INT}(\mu\text{F})(\text{Min}) = 0.029/f_{CK}(\text{MHz})$

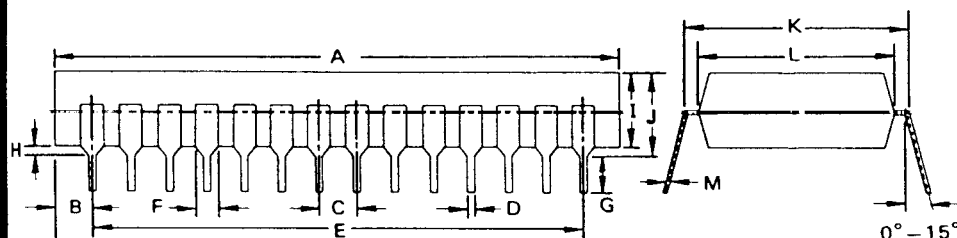
## **TIMING WAVEFORMS**



CONTROL TERMINALS					MODE	INTERNAL FUNCTION	DATA INPUT-OUTPUT TERMINALS
CS	RD	WR	A <sub>1</sub>	A <sub>0</sub>			
H	x	x	x	x	Not selected		High impedance
L	H	H	x	x	Not selected	—	
L	H	L	L	L	Write mode	Data latch A/D start	Input status, D <sub>1</sub> , D <sub>0</sub> = MPX address D <sub>3</sub> = 8 bit/12 bit conversion designation. ① D <sub>2</sub> = Flag Input
L	H	L	L	H	Not selected	—	High Impedance
L	H	L	H	L	Not selected	—	
L	H	L	H	H	Test mode	Test status	Input status ②
L	L	H	L	L	Read mode	Internal status	D <sub>7</sub> = $\overline{EOC}$ , D <sub>6</sub> = $\overline{BUSY}$ , D <sub>5</sub> = MSB, D <sub>4</sub> = 2nd MSB, D <sub>3</sub> = 8/12, D <sub>2</sub> = Flag Output D <sub>1</sub> = MPX, D <sub>0</sub> = MPX
L	L	H	L	H	Read mode	High data byte	D <sub>7</sub> -D <sub>0</sub> = MSB — 8th bit
L	L	H	H	L	Read mode	Low data byte	D <sub>7</sub> -D <sub>4</sub> = 9th — 12th bit, D <sub>3</sub> -D <sub>0</sub> = L
L	L	H	H	H	Read mode	Low data byte	

Notes: ① Designation of number of conversion bits: 8 bit = L; 12 bit = H

② Test Mode: Used for inspecting the device. The data input-output terminals assume an input state and are connected to the A/D counter. Therefore, the A/D conversion data read out after this is meaningless.



PACKAGE OUTLINE  
μPD7002C

ITEM	MILLIMETERS	INCHES
A	38.0 MAX.	1.496 MAX.
B	2.49	0.098
C	2.54	0.10
D	0.5 ± 0.1	0.02 ± 0.004
E	33.02	1.3
F	1.5	0.059
G	2.54 MIN.	0.10 MIN.
H	0.5 MIN.	0.02 MIN.
I	5.22 MAX.	0.205 MAX.
J	5.72 MAX.	0.225 MAX.
K	15.24	0.6
L	13.2	0.52
M	0.25 <sup>+0.10</sup> <sub>-0.05</sub>	0.01 <sup>+0.004</sup> <sub>-0.002</sub>