

## Linear Integrated Systems

**LS OP-07**

### FEATURES:

- Replaces ..... PMI-OP07, 725, 108A/308A, 741  
..... AD 510, MPS Op-07
- Ultra-Low Vos ..... 10 $\mu$ V
- Ultra-Low VOS Drift ..... 0.2 $\mu$ V/°C
- Lowest Noise ..... 0.25 $\mu$ Vpp
- Wide Input Voltage Range .....  $\pm$ 14V
- Wide Supply Voltage Range .....  $\pm$ 3V to  $\pm$ 18V
- High Open-loop gain ..... 300V/mV

### DESCRIPTION:

The LS OP-07 is an ultra-low offset voltage op amp with outstanding noise and input bias (I bias) characteristics. This makes the device ideal for instrumentation applications and other low level signal conditioning circuits. The device is internally compensated and has fully protected input and outputs so no additional components are normally needed.

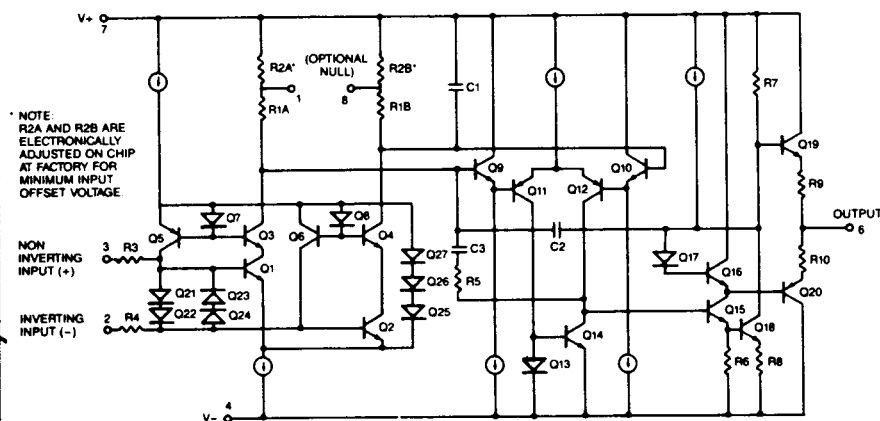
A Vos of 10 $\mu$ V and TC Vos of 0.2 $\mu$ V/°C degrees are achieved through permanent alteration of an on-chip offset trimming network during factory test. This allows for extremely low offset and drift making the device ideal for applications requiring minimal recalibration.

Careful processing and circuit design has virtually eliminated low frequency noise, giving the LS OP-07 a major advantage in limited bandwidth applications. Input bias currents are available with as low as 1na over the full military temperature range. This is achieved through an internal bias cancellation circuit which supplies most of the input bias current needed. The LS OP-07 is an excellent choice for precision amplification of low level transducer signals. Stable integrators, analog computation functions, and precise threshold detectors are easily implemented. It is a superior replacement for many chopperstabilized amplifiers, and a direct replacement for the Op-07, Op-05, 725, and 108A/308A.

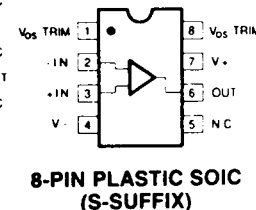
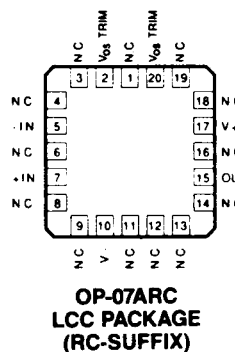
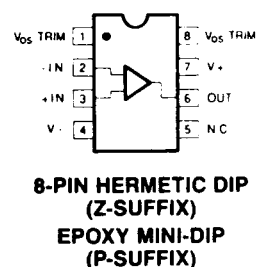
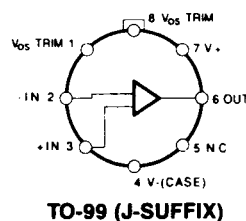
### PRODUCT HIGHLIGHTS:

1. Offset trimming during wafer testing for extremely low input offsets.
2. Ultra-stable over full temperature range.
3. Ultra-low input bias current (I bias) of only 1na available.
4. Low offset and high open-loop gain is ideal for instrumentation applications.
5. Minimal need for external components.
6. Radiation hardenable; consult factory for details.

### SIMPLIFIED SCHEMATIC



### PIN CONNECTIONS



## ABSOLUTE MAXIMUM RATINGS (Note 2)

Supply Voltage	±22
Internal Power Dissipation (Note 1)	500mW
Differential Input Voltage	±30V
Input Voltage (Note 3)	±22V
Output Short-Circuit Duration	Indefinite
Storage Temperature Range	
J, RC and Z Packages	–65°C to +150°C
P Package	–65°C to +125°C
Operating Temperature	
OP-07A, OP-07, OP-07RC	–55°C to +125°C
OP-07E, OP-07C, OP-07D	0°C to +70°C
Lead Temperature Range (Soldering, 60 sec)	300°C
DICE Junction Temperature	–65°C to +150°C

## NOTES:

1. See table for maximum ambient temperature rating and derating factor.

PACKAGE TYPE	MAXIMUM AMBIENT TEMPERATURE FOR RATING	DERATE ABOVE MAXIMUM AMBIENT TEMPERATURE
T0-99 (J)	80°C	7.1mW/°C
8-Pin Hermetic DIP (Z)	75°C	6.7mW/°C
8-Pin Plastic SOIC(S)	62°C	5.6mW/°C
8-Pin Plastic DIP (P)	62°C	5.7mW/°C
LCC (RC)	72°C	7.8mW/°C

- The OP-07's inputs are protected by back-to-back diodes. Current limiting resistors are not used in order to achieve low noise. If differential input voltage exceeds ±0.7V, the input current should be limited to 25mA.
- For supply voltages less than ±22V, the absolute maximum input voltage is equal to the supply voltage.
- Absolute maximum ratings apply to both DICE and packaged parts, unless otherwise noted.

## ELECTRICAL CHARACTERISTICS at $V_S = \pm 15V$ , $T_A = 25^\circ C$ , unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	OP-07A			OP-07			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
Input Offset Voltage	$V_{OS}$	(Note 1)	—	10	25	—	30	75	$\mu V$
Long-Term Input Offset Voltage Stability	$\Delta V_{OS}/\text{Time}$	(Note 2)	—	0.2	1.0	—	0.2	1.0	$\mu V/\text{Mo}$
Input Offset Current	$I_{OS}$		—	0.3	2.0	—	0.4	2.8	nA
Input Bias Current	$I_B$		—	±0.7	±2.0	—	±1.0	±3.0	nA
Input Noise Voltage	$e_{n-p-p}$	0.1Hz to 10Hz (Note 3)	—	0.35	0.6	—	0.35	0.6	$\mu V_{p-p}$
Input Noise Voltage Density	$e_n$	$f_0 = 10\text{Hz}$ (Note 3)	—	10.3	18.0	—	10.3	18.0	$nV/\sqrt{\text{Hz}}$
		$f_0 = 100\text{Hz}$ (Note 3)	—	10.0	13.0	—	10.0	13.0	
		$f_0 = 1000\text{Hz}$ (Note 3)	—	9.6	11.0	—	9.6	11.0	
Input Noise Current	$i_{n-p-p}$	0.1Hz to 10Hz (Note 3)	—	14	30	—	14	30	$pA_{p-p}$
Input Noise Current Density	$i_n$	$f_0 = 10\text{Hz}$ (Note 3)	—	0.32	0.80	—	0.32	0.80	$pA/\sqrt{\text{Hz}}$
		$f_0 = 100\text{Hz}$ (Note 3)	—	0.14	0.23	—	0.14	0.23	
		$f_0 = 1000\text{Hz}$ (Note 3)	—	0.12	0.17	—	0.12	0.17	
Input Resistance — Differential-Mode	$R_{IN}$	(Note 4)	30	80	—	20	60	—	M $\Omega$
Input Resistance — Common-Mode	$R_{INCM}$		—	200	—	—	200	—	G $\Omega$
Input Voltage Range	IVR		±13	±14	—	±13	±14	—	V
Common-Mode Rejection Ratio	CMRR	$V_{CM} = \pm 13V$	110	126	—	110	126	—	dB
Power Supply Rejection Ratio	PSSR	$V_S \pm 3V$ to $\pm 18V$	—	4	10	—	4	10	$\mu V/V$
Large-Signal Voltage Gain	$A_{VO}$	$R_L \geq 2k\Omega$ , $V_O = \pm 10V$	300	500	—	200	500	—	V/mV
		$R_L \geq 500\Omega$ , $V_O = \pm 0.5V$ $V_S = \pm 3V$ (Note 4)	150	400	—	150	400	—	
Output Voltage Swing	$V_O$	$R_L \geq 10k\Omega$	±12.5	±13.0	—	±12.5	±13.0	—	V
		$R_L \geq 2k\Omega$	±12.0	±12.8	—	±12.0	±12.8	—	
		$R_L \geq 1k\Omega$	±10.5	±12.0	—	±10.5	12.0	—	
Slew Rate	SR	$R_L \geq 2k\Omega$ (Note 3)	0.1	0.3	—	0.1	0.3	—	V/ $\mu s$
Closed-Loop Bandwidth	BW	$A_{VCL} = +1$ (Note 3)	0.4	0.6	—	0.4	0.6	—	MHz
Open-Loop Output Resistance	$R_O$	$V_O = 0$ , $I_O = 0$	—	60	—	—	60	—	$\Omega$
Power Consumption	$P_d$	$V_S = \pm 15V$ , No Load	—	75	120	—	75	120	mW
		$V_S = \pm 3V$ , No Load	—	4	6	—	4	6	
Offset Adjustment Range		$R_p = 20k\Omega$	—	±4	—	—	±4	—	mV

## NOTES:

- OP-07A grade  $V_{OS}$  is measured approximately one minute after application of power. For all other grades  $V_{OS}$  is measured approximately 0.5 seconds after application of power.
- Long-Term Input Offset Voltage Stability refers to the averaged trend line of  $V_{OS}$  vs. Time over extended periods after the first 30 days of operation.

Excluding the initial hour of operation, changes in  $V_{OS}$  during the first 30 operating days are typically 2.5 $\mu V$ .

- Sample tested.
- Guaranteed by design.

## ELECTRICAL CHARACTERISTICS at $V_S = \pm 15V$ , $T_A = 25^\circ C$ , unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	OP-07E			OP-07C			OP-07D			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
Input Offset Voltage	$V_{OS}$	(Note 1)	—	30	75	—	60	150	—	60	150	$\mu V$
Long-Term $V_{OS}$ Stability	$\Delta V_{OS}/\text{Time}$	(Note 2)	—	0.3	1.5	—	0.4	2.0	—	0.5	3.0	$\mu V/\text{Mo}$
Input Offset Current	$I_{OS}$		—	0.5	3.8	—	0.8	6.0	—	0.8	6.0	nA
Input Bias Current	$I_B$		—	$\pm 1.2$	$\pm 4.0$	—	$\pm 1.8$	$\pm 7.0$	—	$\pm 2.0$	$\pm 12$	nA
Input Noise Voltage	$e_{n-p-p}$	01.Hz to 10Hz (Note 2)	—	0.35	0.6	—	0.38	0.65	—	0.38	0.65	$\mu V_{p-p}$
Input Noise Voltage Density	$e_n$	$f_O = 10\text{Hz}$	—	10.3	18.0	—	10.5	20.0	—	10.5	20.0	$nV/\sqrt{\text{Hz}}$
		$f_O = 100\text{Hz}$ (Note 2)	—	10.0	13.0	—	10.2	13.5	—	10.3	13.5	
		$f_O = 1000\text{Hz}$	—	9.6	11.0	—	9.8	11.5	—	9.8	11.5	
Input Noise Current	$i_{n-p-p}$	0.1Hz to 10Hz (Note 2)	—	14	30	—	15	35	—	15	35	$pA_{p-p}$
Input Noise Current Density	$i_n$	$f_O = 10\text{Hz}$	—	0.32	0.80	—	0.35	0.90	—	0.35	0.90	$pA/\sqrt{\text{Hz}}$
		$f_O = 100\text{Hz}$ (Note 2)	—	0.14	0.23	—	0.15	0.27	—	0.15	0.27	
		$f_O = 1000\text{Hz}$	—	0.12	0.17	—	0.13	0.18	—	0.13	0.18	
Input Resistance—Differential-Mode	$R_{IN}$	(Note 3)	15	50	—	8	33	—	7	31	—	M $\Omega$
Input Resistance—Common-Mode	$R_{INCM}$		—	160	—	—	120	—	—	120	—	G $\Omega$
Input Voltage Range	IVR		$\pm 13$	$\pm 14$	—	$\pm 13$	$\pm 14$	—	$\pm 13$	$\pm 14$	—	V
Common-Mode Rejection Ratio	CMRR	$V_{CM} = \pm 13V$	106	123	—	100	120	—	94	110	—	dB
Power Supply Rejection Ratio	PSRR	$V_S = \pm 3V$ to $\pm 18V$	—	5	20	—	7	32	—	7	32	$\mu V/V$
Large-Signal Voltage Gain	$A_{VO}$	$R_L \geq 2k\Omega$ , $V_O = \pm 10V$	200	500	—	120	400	—	120	400	—	V/mV
		$R_L \leq 500\Omega$	150	400	—	100	400	—	—	400	—	
		$V_O = \pm 0.5V$ $V_S = \pm 3V$ (Note 3)	—	—	—	—	—	—	—	—	—	
Output Voltage Swing	$V_O$	$R_L \geq 10k\Omega$	$\pm 12.5$	$\pm 13.0$	—	$\pm 12.0$	$\pm 13.0$	—	$\pm 12.0$	$\pm 13.0$	—	V
		$R_L \geq 2k\Omega$	$\pm 12.0$	$\pm 12.8$	—	$\pm 11.5$	$\pm 12.8$	—	$\pm 11.5$	$\pm 12.8$	—	
		$R_L \leq 1k\Omega$	$\pm 10.5$	$\pm 12.0$	—	—	$\pm 12.0$	—	—	$\pm 12.0$	—	
Slew Rate	SR	$R_L \geq 2k\Omega$ (Note 2)	0.1	0.3	—	0.1	0.3	—	0.1	0.3	—	V/ $\mu s$
Closed-Loop Bandwidth	BW	$A_{VCL} = +1$ (Note 3)	0.4	0.6	—	0.4	0.6	—	0.4	0.6	—	MHz
Open-Loop Output Resistance	$R_O$	$V_O = 0$ , $I_O = 0$	—	60	—	—	60	—	—	60	—	$\Omega$
Power Consumption	$P_d$	$V_S = \pm 15V$ , No Load	—	75	120	—	80	150	—	80	150	mW
		$V_S = \pm 3V$ , No Load	—	4	6	—	4	8	—	4	8	
Offset Adjustment Range		$R_p = 20k\Omega$	—	$\pm 4$	—	—	$\pm 4$	—	—	$\pm 4$	—	mV

### NOTES:

- Input offset voltage measurements are performed by automated test equipment approximately 0.5 seconds after application of power.
- Sample tested.
- Guaranteed by design.

## ELECTRICAL CHARACTERISTICS at $V_S = \pm 15V$ , $0^\circ C \leq T_A \leq +70^\circ C$ , unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	OP-07E			OP-07C			OP-07D			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
Input Offset Voltage	$V_{OS}$	(Note 1)	—	45	130	—	85	250	—	85	250	$\mu V$
Average Input Offset Voltage Drift	$TCV_{OS}$	(Note 3)	—	0.3	1.3	—	0.5	1.8	—	0.7	2.5	$\mu V/^\circ C$
		$R_p = 20k\Omega$ (Note 3)	—	0.3	1.3	—	0.4	1.6	—	0.7	2.5	
Input Offset Current	$I_{OS}$		—	0.9	5.3	—	1.6	8.0	—	1.6	8.0	nA
Average Input Offset Current Drift	$TCI_{OS}$	(Note 2)	—	8	35	—	12	50	—	12	50	$pA/^\circ C$
Input Bias Current	$I_B$		—	$\pm 1.5$	$\pm 5.5$	—	$\pm 2.2$	$\pm 9.0$	—	$\pm 3.0$	$\pm 14$	nA
Average Input Bias Current Drift	$TCI_B$	(Note 2)	—	13	35	—	18	50	—	18	50	$pA/^\circ C$
Input Voltage Range	IVR		$\pm 13.0$	$\pm 13.5$	—	$\pm 13.0$	$\pm 13.5$	—	$\pm 13.0$	$\pm 13.5$	—	V
Common-Mode Rejection Ratio	CMRR	$V_{CM} = \pm 13V$	103	123	—	97	120	—	94	106	—	dB
Power Supply Rejection Ratio	PSRR	$V_S = \pm 3V$ to $\pm 18V$	—	7	32	—	10	51	—	10	51	$\mu V/V$
Large-Signal Voltage Gain	$A_{VO}$	$R_L \geq 2k\Omega$ , $V_O = \pm 10V$	180	450	—	100	400	—	100	400	—	V/mV
Output Voltage Swing	$V_O$	$R_L \geq 2k\Omega$	$\pm 12$	$\pm 12.6$	—	$\pm 11$	$\pm 12.6$	—	$\pm 11$	$\pm 12.6$	—	V

### NOTES:

- Input offset voltage measurements are performed by automated test equipment approximately 0.5 seconds after application of power.
- Sample tested.
- Guaranteed by design.

**WAFER TEST LIMITS** at  $V_S = \pm 15V$ ,  $T_A = 25^\circ C$  for OP-07N, OP-07G and OP-07GR devices;  $T_A = 125^\circ C$  for OP-07NT and OP-07GT devices, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	OP-07NT LIMIT	OP-07N LIMIT	OP-07GT LIMIT	OP-07G LIMIT	OP-07GR LIMIT	UNITS
Input Offset Voltage	$V_{OS}$		140	40	210	80	150	$\mu V$ MAX
Input Offset Current	$I_{OS}$		4.0	2.0	5.6	2.8	6.0	nA MAX
Input Bias Current	$I_B$		$\pm 4$	$\pm 2$	$\pm 6$	$\pm 3$	$\pm 7$	nA MAX
Input Resistance Differential-Mode	$R_{IN}$	(Note 2)	—	20	—	20	8	M $\Omega$ MIN
Input Voltage Range	IVR		$\pm 13$	$\pm 13$	$\pm 13$	$\pm 13$	$\pm 13$	V MIN
Common-Mode Rejection Ratio	CMRR	$V_{CM} = \pm 13V$	100	110	100	110	100	dB MIN
Power Supply Rejection Ratio	PSRR	$V_S = \pm 3V$ to $\pm 18V$	20	10	20	10	30	$\mu V/V$ MAX
Output Voltage Swing	$V_O$	$R_L = 10k\Omega$	—	$\pm 12.5$	—	$\pm 12.0$	$\pm 12.0$	V MIN
		$R_L = 2k\Omega$	$\pm 12.0$	$\pm 12.0$	$\pm 12.0$	$\pm 11.5$	$\pm 11.5$	
		$R_L = 1k\Omega$	—	$\pm 10.5$	—	$\pm 10.5$	—	
Large-Signal Voltage Gain	$A_{VO}$	$R_L = 2k\Omega$ , $V_O = \pm 10V$	200	200	150	120	120	V/mV MIN
Differential Input Voltage			$\pm 30$	$\pm 30$	$\pm 30$	$\pm 30$	$\pm 30$	V MAX
Power Consumption	$P_d$	$V_{OUT} = 0V$	—	120	—	120	150	mW MAX

## NOTE:

- For  $25^\circ C$  characteristics of OP-07NT and OP-07GT, see OP-07N and OP-07G characteristics, respectively.
- Guaranteed by design.

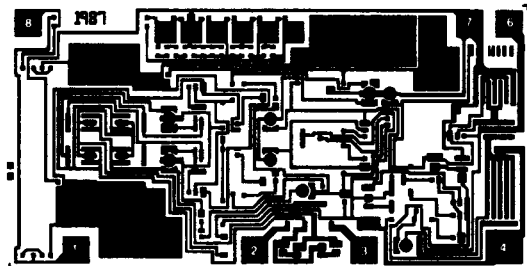
Electrical tests are performed at wafer probe to the limits shown. Due to variations in assembly methods and normal yield loss, yield after packaging is not guaranteed for standard product dice. Consult factory to negotiate specifications based on dice lot qualification through sample lot assembly and testing.

**TYPICAL ELECTRICAL CHARACTERISTICS** at  $V_S = \pm 15V$ ,  $T_A = 25^\circ C$ , unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	OP-07NT TYPICAL	OP-07N TYPICAL	OP-07GT TYPICAL	OP-07G TYPICAL	OP-07GR TYPICAL	UNITS
Average Input Offset Voltage Drift	$TCV_{OS}$	$R_S = 50\Omega$	0.2	0.2	0.3	0.3	0.7	$\mu V/^\circ C$
Nulled Input Offset Voltage Drift	$TCV_{OSn}$	$R_S = 50\Omega$ , $R_P = 20k\Omega$	0.2	0.2	0.3	0.3	0.7	$\mu V/^\circ C$
Average Input Offset Current Drift	$TCI_{OS}$		5	5	8	8	12	pA/ $^\circ C$
Slew Rate	SR	$R_L \geq 2k\Omega$	0.3	0.3	0.3	0.3	0.3	V/ $\mu s$
Closed-Loop Bandwidth	BW	$A_{VCL} = +1$	0.6	0.6	0.6	0.6	0.6	MHz

## DICE CHARACTERISTICS (125°C TESTED DICE AVAILABLE)

DIE SIZE 0.100x0.053 inch, 5300 sq. mils  
(2.54x1.35mm, 3.42 sq. mm)



For additional DICE information contact factory.

- BALANCE
- INVERTING INPUT
- NONINVERTING INPUT
- $V_-$
- OUTPUT
- $V_+$
- BALANCE

## LS OP-07 ORDERING INFORMATION

PACKAGE					OPERATING TEMP. RANGE
HERMETIC TO-99 8-PIN	HERMETIC DIP 8-PIN	PLASTIC DIP 8-PIN	PLASTIC SO-JEDEC 8-PIN	LCC	
OP-07AJ	OP-07AZ	—	—	OP-07ARC	MIL
OP-07J	OP-07E	—	—	—	MIL/IND
OP-07EJ	OP-07EZ	OP-07EP	—	—	IND/COM
OP-07CJ	OP-07CZ	OP-07CP	OP-07CS	—	IND/COM
OP-07DJ	OP-07DZ	OP-07DP	—	—	IND/COM

All commercial and industrial temperature range parts are available with burn-in. For ordering information call the factory.