



MOTOROLA

MCF5307 UART MODULE



UART INTERFACE

OVERVIEW

- TWO INDEPENDENT, FULL DUPLEX ASYNCHRONOUS/SYNCHRONOUS RECEIVER/TRANSMITTER CHANNELS
- INDEPENDENTLY PROGRAMMABLE BAUD RATE GENERATOR FOR EACH RECEIVER AND TRANSMITTER DERIVABLE FROM SYSTEM CLOCK OR EXTERNAL CLOCK ON **TIN** PIN

- PROGRAMMABLE DATA FORMAT, FIVE TO EIGHT DATA BITS PLUS PARITY OR ADDRESS MARK BIT

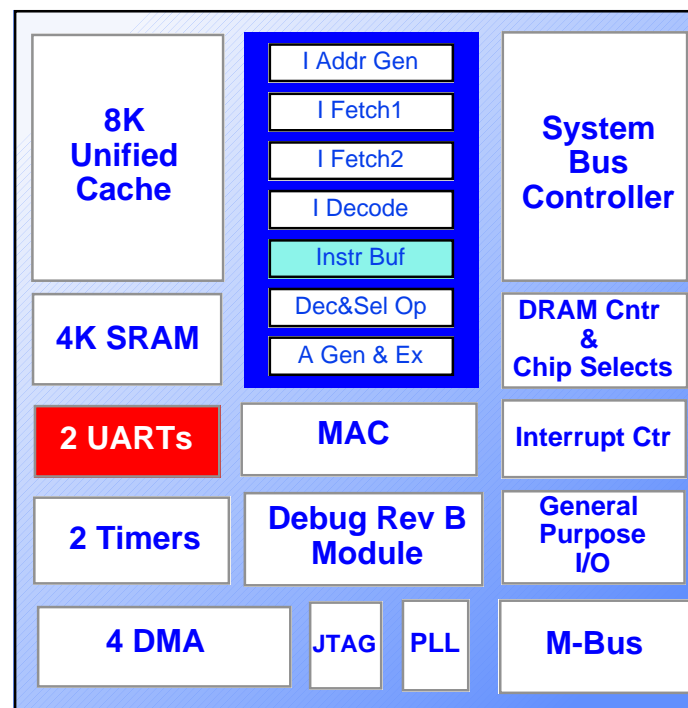
PARITY OPTIONS:

- 1- ODD PARITY
- 2- EVEN PARITY
- 3- FORCE PARITY
- 4- NO PARITY

- PROGRAMMABLE CHANNEL MODES
NORMAL (FULL DUPLEX)
AUTOMATIC ECHO (HALF DUPLEX)
LOCAL LOOPBACK
REMOTE LOOPBACK

- UART CAN BE PROGRAMMED TO DIRECTLY INTERRUPT DMA FOR FAST TRANSFERS

MCF5307





UART RECEIVER

FEATURES :

- AUTOMATIC WAKEUP FOR MULTIDROP APPLICATIONS
- FRAMING, PARITY AND OVERRUN ERROR DETECTIONS
- FALSE START BIT DETECTION
- LINE-BREAK DETECTION
- DETECTION OF A BREAK ORIGINATING IN THE MIDDLE OF A CHARACTER
- START/END BREAK INTERRUPT /STATUS
- FOUR STAGE FIFO RECEIVE BUFFER
- RECEIVER OPERATION MAY BE POLLED OR INTERRUPT DRIVEN



UART TRANSMITTER

FEATURES:

- DOUBLE-BUFFERED OPERATION
- PARITY GENERATION: ODD, EVEN, NO PARITY OR FORCE PARITY
- STOP BIT GENERATION FROM .563 TO 2-BITS
- BREAK GENERATION
- AUTOMATIC NEGATION OF REQUEST-TO-SEND UPON COMPLETION OF MESSAGE TRANSMISSION
- PROGRAMMABLE CHARACTER LENGTH FROM 5 TO 8-BITS



UART BLOCK DIAGRAM AND INTERFACE SIGNALS

RxD - SERIAL RECEIVE DATA PIN, DATA IS SAMPLED ON RISING EDGE OF CLOCK SOURCE.

TxD - SERIAL TRANSMIT DATA PIN, DATA IS SHIFTED OUT ON FALLING EDGE OF CLOCK SOURCE.

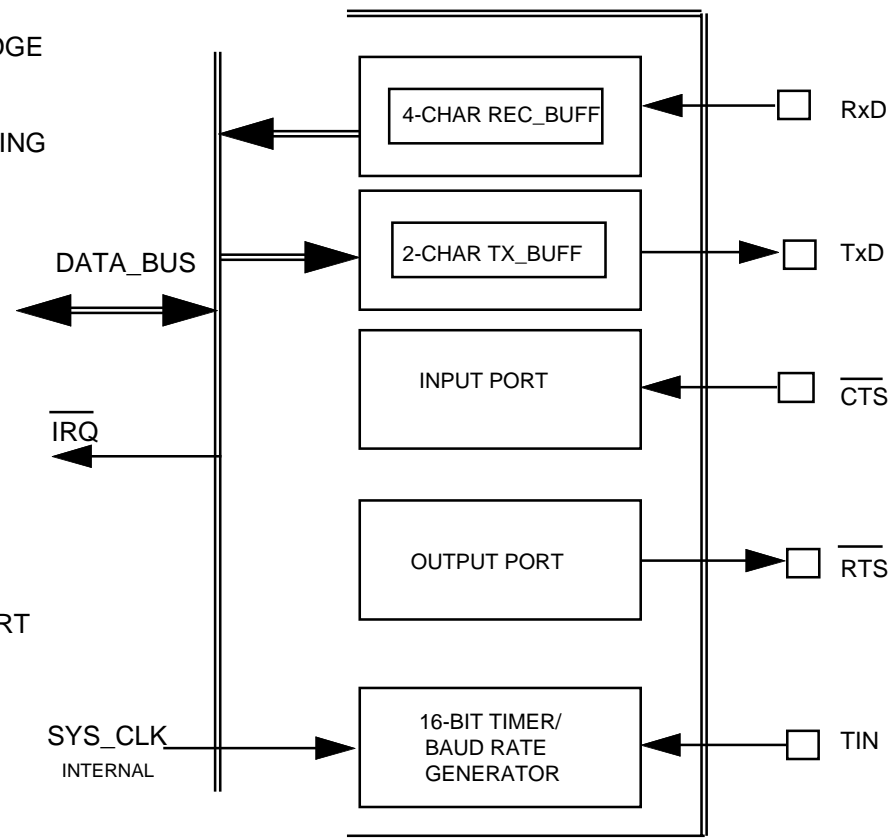
$\overline{\text{RTS}}$ - REQUEST-TO-SEND, THIS PIN MAY BE USED TO CONTROL SERIAL DATA FLOW WHEN CONNECTED TO CTS INPUT PIN OF THE TRANSMITTER.

$\overline{\text{CTS}}$ - CLEAR-TO-SEND, THIS SIGNAL GENERATES INTERRUPT REQUEST TO THE CPU UPON CHANGE OF STATE.

SYS_CLK - CLOCK INPUT TO BAUD RATE GENERATOR OR 16-BIT TIMER TO GENERATE STANDARD BAUD RATES.

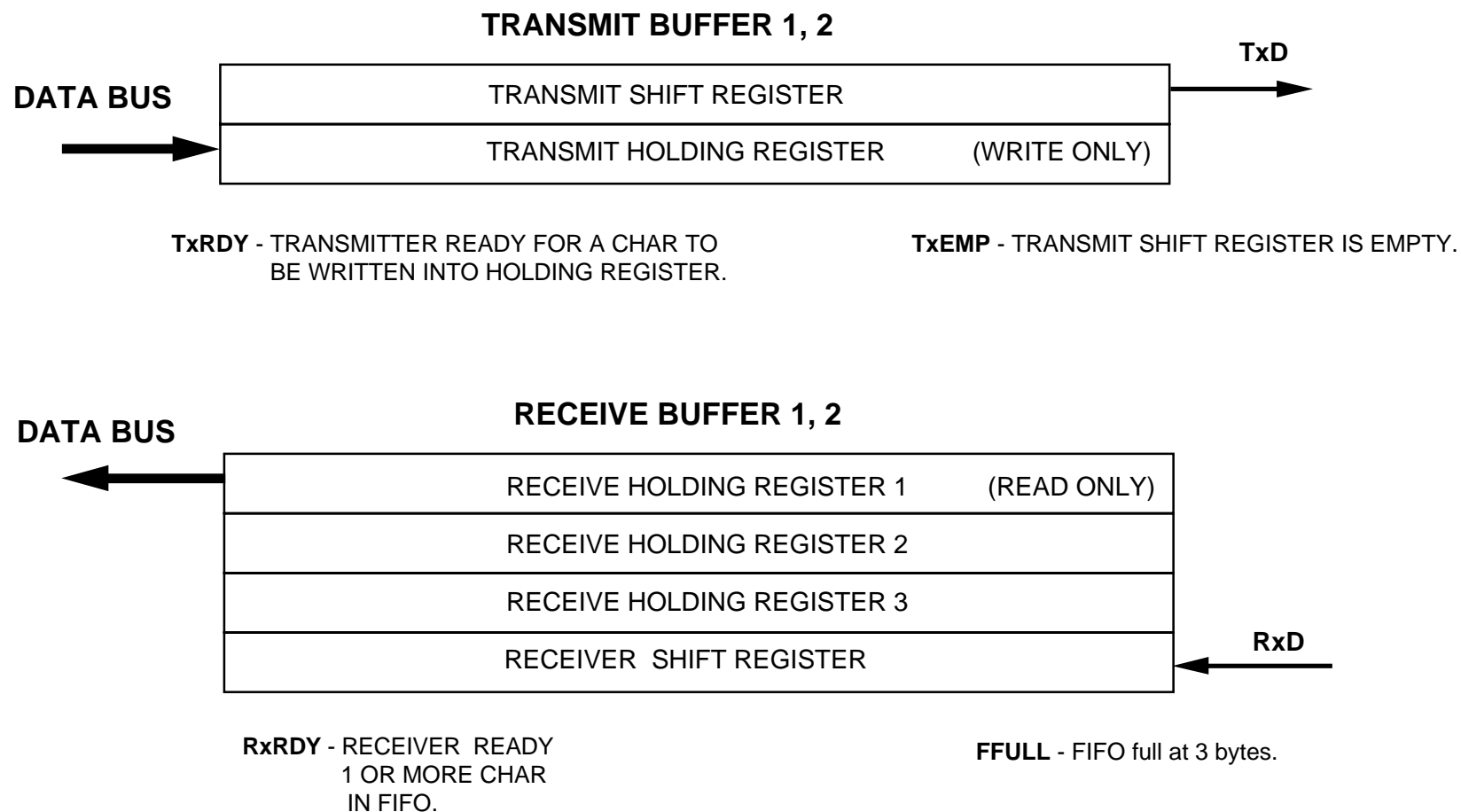
IRQ - AN INTERNAL INTERRUPT REQUEST SIGNAL FROM THE DUART INTERFACE.

TIN - CAN BE USED AS THE CLOCK SOURCE





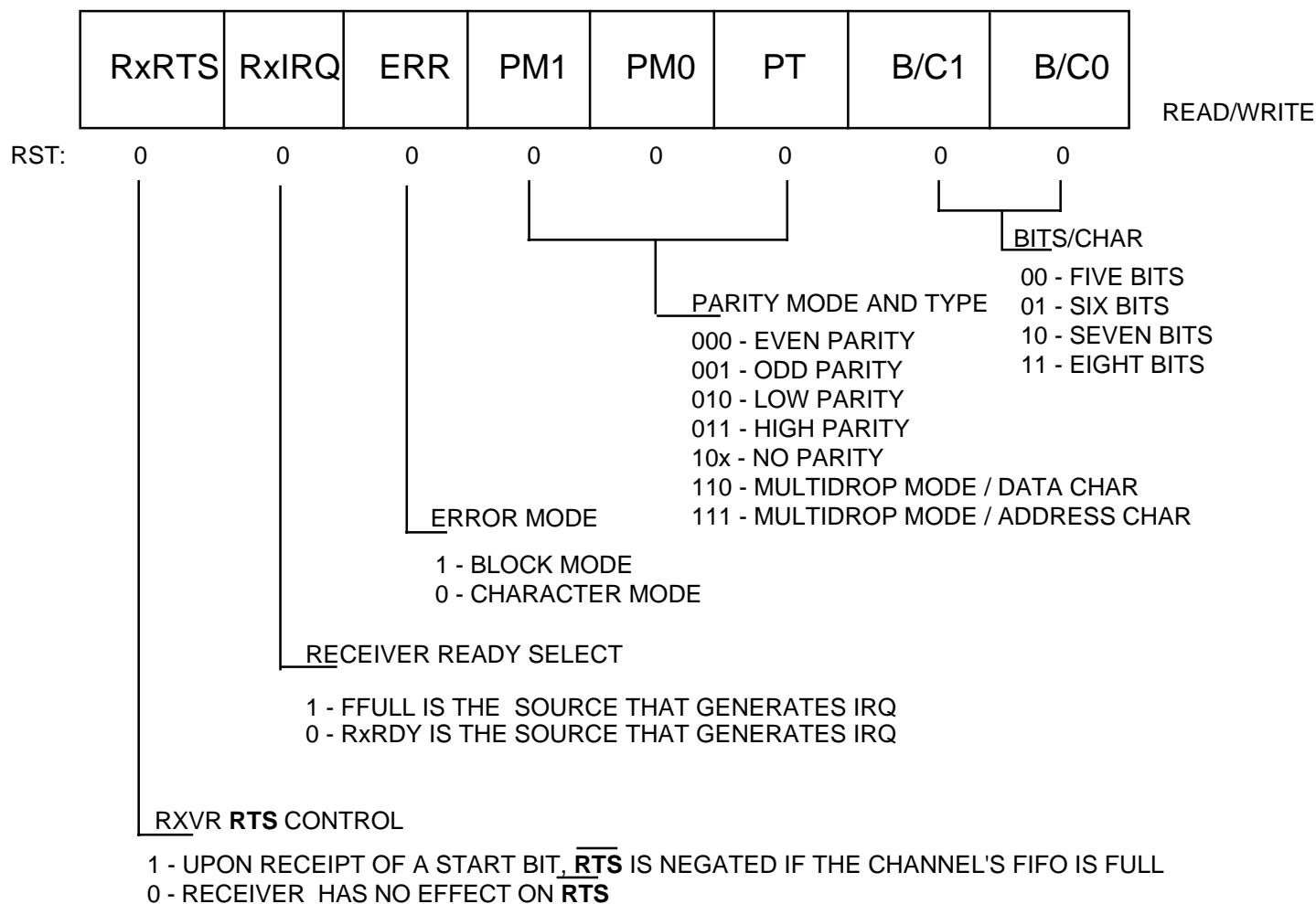
BUFFERED DUART (Rx/Tx Buff)





RECEIVER REGISTERS

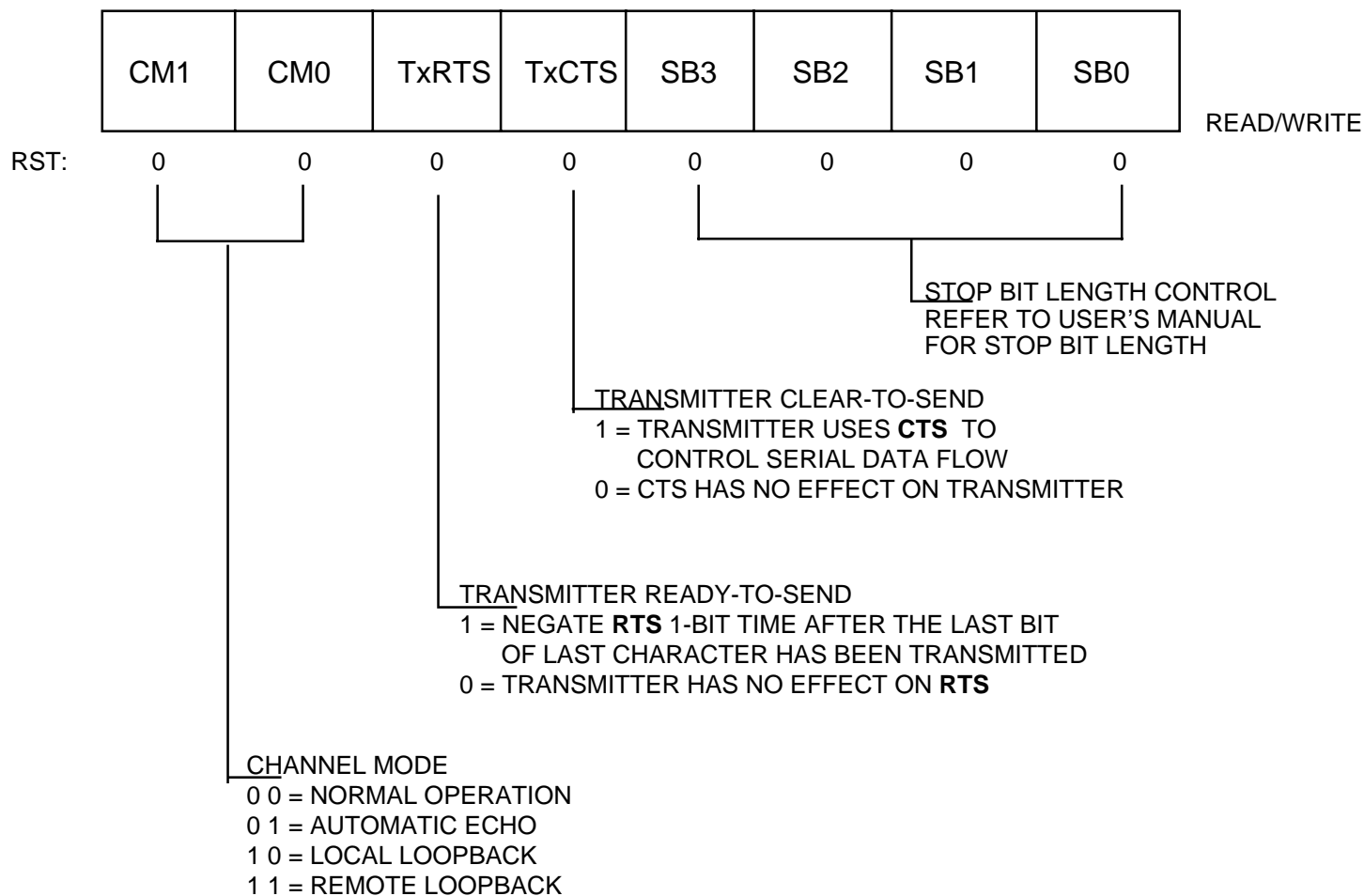
UMR1 - UART MODE REGISTER 1





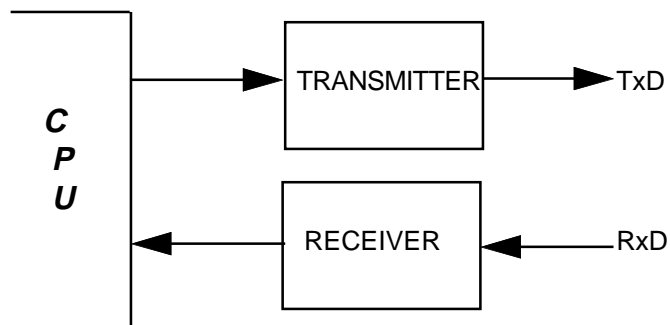
UART REGISTERS

UMR2 - UART MODE REGISTER 2

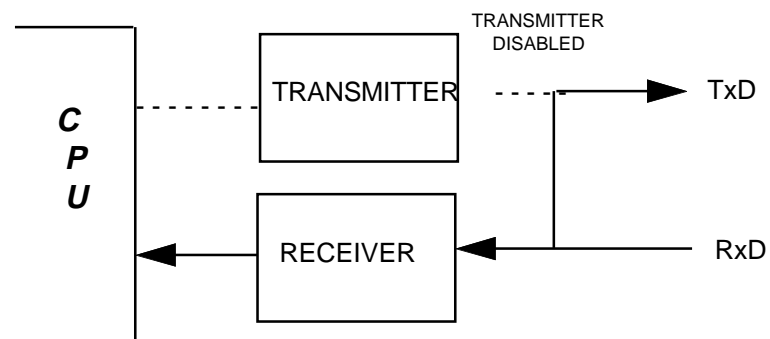




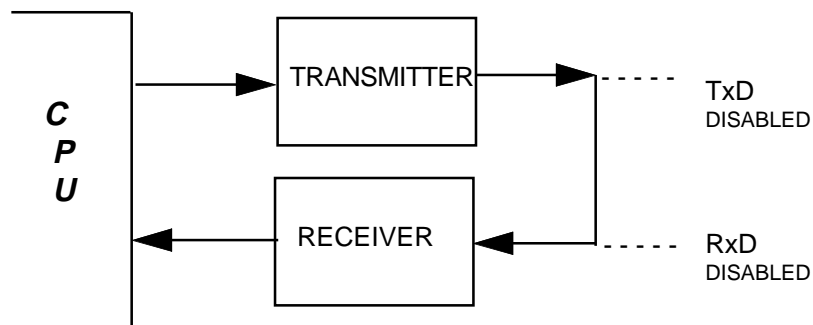
UART MODES



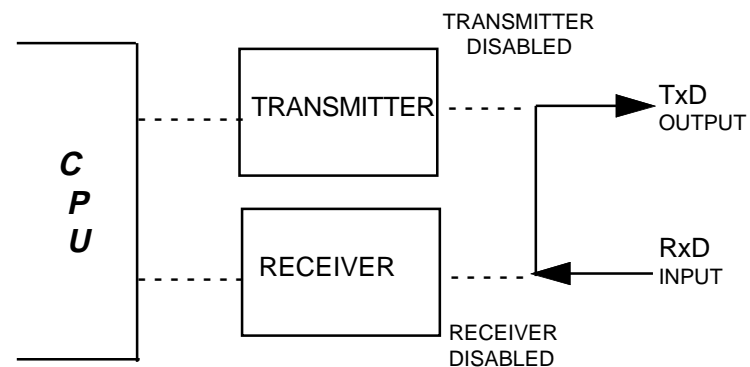
NORMAL OPERATION
UMR2(CM1:0) = 00



AUTOMATIC ECHO
UMR2(CM1:0) = 01



LOCAL LOOPBACK
UMR2(CM1:0) = 10



REMOTE LOOPBACK
UMR2(CM1:0) = 11

**MOTOROLA**

RECEIVER/TRANSMITTER STATUS

USR - STATUS REGISTER

RB	FE	PE	OE	TxEMP	TxRDY	FFULL	RxRDY
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READ ONLY

RST:

0 0 0 0 0 0 0 0

RECEIVER READY

1 = 1 OR MORE CHARACTERS ARE WAITING TO BE READ

0 = CPU READ THE ENTIRE FIFO

FIFO IS FULL

1 = 3-STAGE RECEIVE BUFFER IS FULL

0 = FIFO IS NOT FULL AND MAY CONTAIN UP TO 2-CHAR

TRANSMITTER READY

1 = TRANSMIT HOLDING REGISTER IS EMPTY

0 = TRANSMITTER IS FULL OR DISABLED

TRANSMITTER EMPTY

1 = UNDERRUN CONDITION IS DETECTED

0 = TRANSMITTER IS NOT EMPTY OR DISABLED

OVERRUN ERROR

1 = ONE OR MORE CHARS IN THE
DATA STREAM HAS BEEN LOST

0 = NO OVERRUN CONDITION

PARITY ERROR

1 = PARITY ERROR

0 = NO PARITY ERROR

(IN MULTIDROP MODE, THIS BIT
STORES THE VALUE OF THE A/D BIT)

FRAMING ERROR

1 = NO STOP BIT WAS DETECTED WHEN
CHAR WAS RECEIVED IN THE FIFO.

0 = NO FRAMING ERROR WAS DETECTED

RECEIVED BREAK

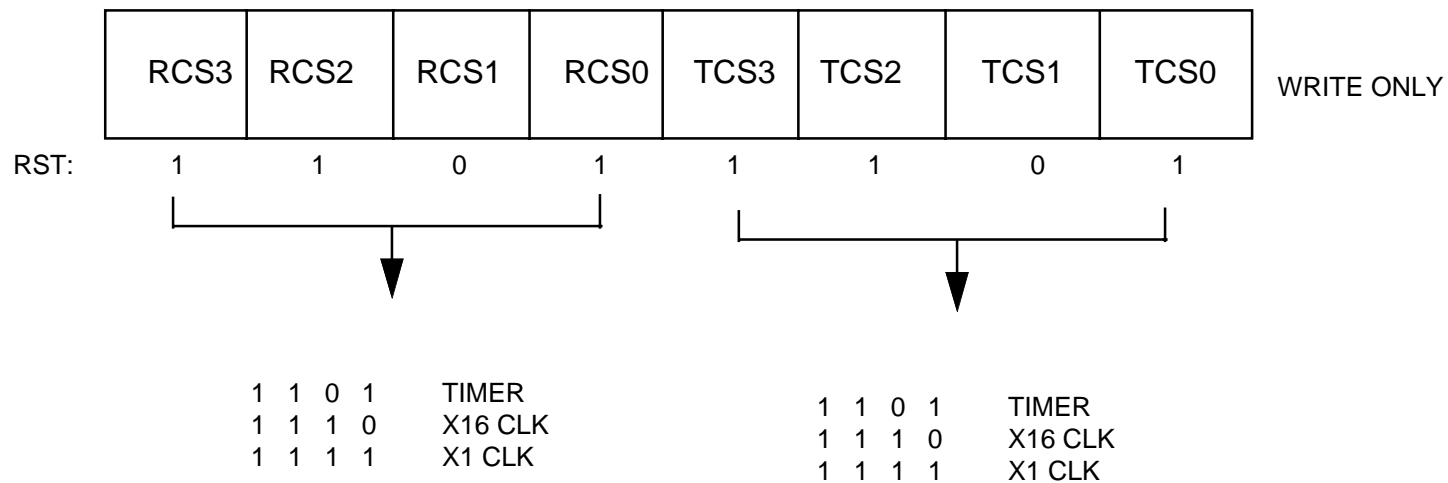
1 = A BREAK CHAR HAS BEEN RECEIVED AND FURTHER ENTRIES TO
THE FIFO ARE INHIBITED UNTIL RxD RETURNS TO THE HIGH
STATE FOR AT LEAST ONE-HALF BIT TIME.

0 = NO BREAK RECEIVED



BAUD RATE SELECTION

UCSR - CLOCK SELECT REGISTER

**RECEIVER BAUD RATE SELECTION****TRANSMITTER BAUD RATE SELECTION**



UART COMMANDS

UCR - COMMAND REGISTER

-	MISC2	MISC1	MISC0	TC1	TC0	RC1	RC0
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WRITE ONLY

RST: 0 0 0 0 0 0 0 0

MISC2	MISC1	MISC0	COMMAND
0	0	0	NO COMMAND
0	0	1	RESET MODE REG PNTR
0	1	0	RESET RECEIVER
0	1	1	RESET TRANSMITTER
1	0	0	RESET ERROR STATUS
1	0	1	RESET BRK CHANGE IRQ
1	1	0	START BREAK
1	1	1	STOP BREAK

MISC COMMANDS

TC1	TC0	COMMAND
0	0	NO COMMAND
0	1	ENABLE TRANSMITTER
1	0	DISABLE TRANSMITTER
1	1	DO NOT USE

TRANSMITTER COMMANDS

RC1	RC0	COMMAND
0	0	NO COMMAND
0	1	ENABLE RECEIVER
1	0	DISABLE RECEIVER
1	1	DO NOT USE

RECEIVER COMMANDS



UART REGISTERS

UIPCR - INPUT PORT CHANGE REGISTER

0	0	0	COS	1	1	1	$\overline{\text{CTS}}$
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READ ONLY

RST: 0 0 0 0 0 1 1 $\overline{\text{CTS}}$

COS - WHEN SET INDICATES A LOW-TO-HIGH OR HIGH-TO-LOW TRANSITION LONGER THAN 25-50uSec HAS OCCURRED ON INPUT PIN. AN IRQ IS GENERATED TO THE CPU, IF ENABLED

CTS - INDICATES THE CURRENT PIN STATE INPUT

UIP - INPUT PORT REGISTER

-	-	-	-	-	-	-	$\overline{\text{CTS}}$
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READ ONLY

RST: 1 1 1 1 1 1 1 $\overline{\text{CTS}}$

CTS - INDICATES THE CURRENT PIN STATE INPUT

UACR - AUXILIARY CONTROL REGISTER

BGR	CTMS2	CTMS1	CTMS0	-	-	-	IEC
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WRITE ONLY

RST: 0 0 0 0 0 0 0 0

BGR=1, SET 2 OF BAUD RATES IS SELECTED
BGR=0, SET 1 OF BAUD RATES IS SELECTED

CTMS[2:0] SHOULD BE SET TO 110

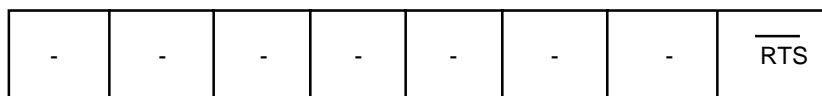
IEC = 1, ENABLE IRQ TO CPU
BY A CHANGE OF STATE
ON CTS INPUT.

IEC = 0, NO IRQ IS GENERATED TO CPU
BECAUSE OF A CHANGE ON CTS



UART REGISTERS

UOP1 - OUTPUT PORT DATA REGISTER



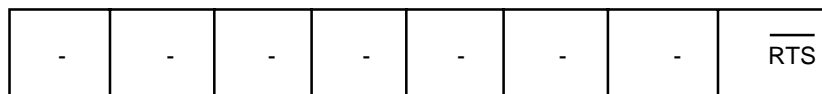
WRITE ONLY

RST: - - - - - - - 0

BIT SET

Write a 1 to force RTS low

UOP0 - OUTPUT PORT DATA REGISTER



WRITE ONLY

RST: - - - - - - - -

BIT RESET

Write a 1 to force RTS high



INTERRUPT ENABLE & STATUS

UISR - INTERRUPT STATUS REGISTER

	COS	-	-	-	-	DB	RxRDY	TxRDY	READ ONLY
RST:	0	0	0	0	0	0	0	0	

UIMR - INTERRUPT MASK REGISTER

	COS	-	-	-	-	DB	RxRDY	TxRDY	WRITE ONLY
RST:	0	0	0	0	0	0	0	0	

CHANGE OF STATE
1 = INPUT PIN CHANGED STATE
0 = NO CHANGE OF STATE

DELTA BREAK
1 = RECEIVER DETECTED BREAK
0 = NO BREAK DETECTED

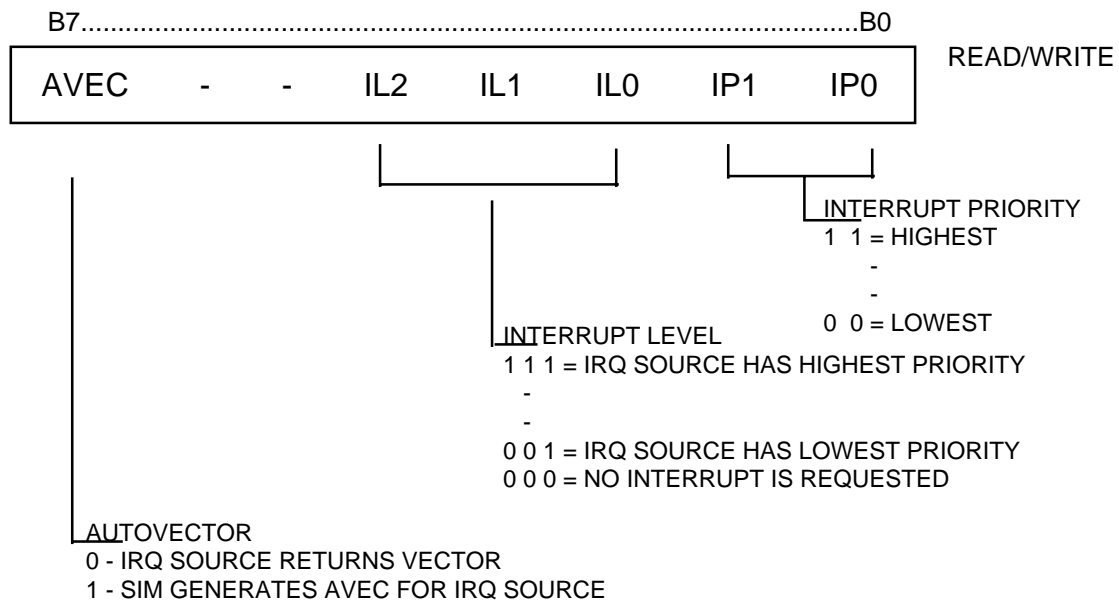
RECEIVER READY OR FIFO FULL. DUPLICATE OF UMR1 BIT6

TRANSMITTER READY
1 = TRANSMIT HOLDING REGISTER IS EMPTY
0 = CPU LOADED TRANSMIT REG.



UART INTERRUPT CONTROL

ICR 3 & 4- UART INTERRUPT CONTROL REGISTER 3 & 4



UIVR - INTERRUPT VECTOR REGISTER

