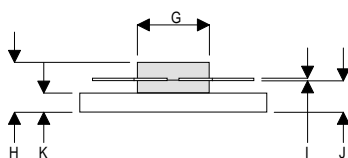
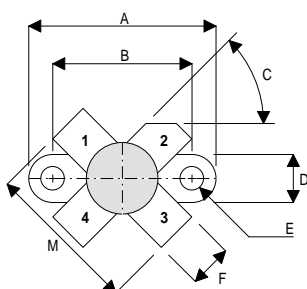


## MECHANICAL DATA



DA

PIN 1 SOURCE      PIN 2 DRAIN  
PIN 3 SOURCE      PIN 4 GATE

DIM	mm	Tol.	Inches	Tol.
A	24.76	0.13	0.975	0.005
B	18.42	0.13	0.725	0.005
C	45°	5°	45°	5°
D	6.35	0.13	0.25	0.005
E	3.17	0.13	0.125 DIA	0.005
F	5.71	0.13	0.225	0.005
G	9.52	0.13	0.375	0.005
H	6.60	REF	0.260	REF
I	0.13	0.02	0.005	0.001
J	4.32	0.13	0.170	0.005
K	2.54	0.13	0.100	0.005
M	20.32	0.25	0.800	0.010

# GOLD METALLISED MULTI-PURPOSE SILICON DMOS RF FET 40W – 28V – 175MHz SINGLE ENDED

## FEATURES

- SIMPLIFIED AMPLIFIER DESIGN
- SUITABLE FOR BROAD BAND APPLICATIONS
- LOW  $C_{rss}$
- SIMPLE BIAS CIRCUITS
- LOW NOISE
- HIGH GAIN – 16 dB MINIMUM

## APPLICATIONS

- HF/VHF/UHF COMMUNICATIONS  
from 1 MHz to 175 MHz

ABSOLUTE MAXIMUM RATINGS ( $T_{case} = 25^{\circ}C$  unless otherwise stated)

$P_D$	Power Dissipation	87W
$BV_{DSS}$	Drain – Source Breakdown Voltage	70V
$BV_{GSS}$	Gate – Source Breakdown Voltage	$\pm 20V$
$I_{D(sat)}$	Drain Current	10A
$T_{stg}$	Storage Temperature	$-65$ to $150^{\circ}C$
$T_j$	Maximum Operating Junction Temperature	$200^{\circ}C$

## ELECTRICAL CHARACTERISTICS ( $T_{case} = 25^{\circ}C$ unless otherwise stated)

Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$BV_{DSS}$ Drain–Source Breakdown Voltage	$V_{GS} = 0$ $I_D = 100mA$	70			V
$I_{DSS}$ Zero Gate Voltage Drain Current	$V_{DS} = 28V$ $V_{GS} = 0$			2	mA
$I_{GSS}$ Gate Leakage Current	$V_{GS} = 20V$ $V_{DS} = 0$			1	$\mu A$
$V_{GS(th)}$ Gate Threshold Voltage*	$I_D = 10mA$ $V_{DS} = V_{GS}$	1		7	V
$g_{fs}$ Forward Transconductance*	$V_{DS} = 10V$ $I_D = 2A$	1.6			S
$G_{PS}$ Common Source Power Gain	$P_O = 40W$	16			dB
$\eta$ Drain Efficiency	$V_{DS} = 28V$ $I_{DQ} = 0.2A$	50			%
VSWR Load Mismatch Tolerance	$f = 175MHz$	20:1			—
$C_{iss}$ Input Capacitance	$V_{DS} = 28V$ $V_{GS} = -5V$ $f = 1MHz$			120	pF
$C_{oss}$ Output Capacitance	$V_{DS} = 28V$ $V_{GS} = 0$ $f = 1MHz$			60	pF
$C_{rss}$ Reverse Transfer Capacitance	$V_{DS} = 28V$ $V_{GS} = 0$ $f = 1MHz$			5	pF

\* Pulse Test: Pulse Duration = 300  $\mu s$  , Duty Cycle  $\leq 2\%$

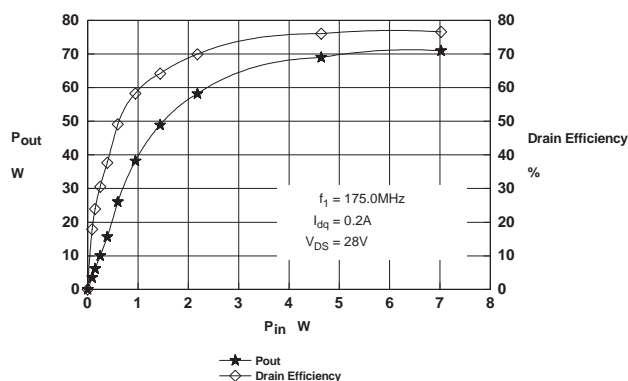
## HAZARDOUS MATERIAL WARNING

The ceramic portion of the device between leads and metal flange is beryllium oxide. Beryllium oxide dust is highly toxic and care must be taken during handling and mounting to avoid damage to this area.

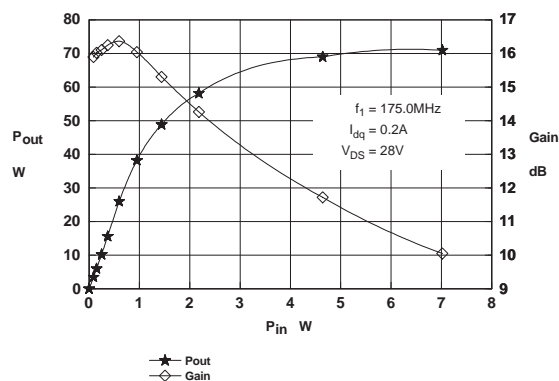
**THESE DEVICES MUST NEVER BE THROWN AWAY WITH GENERAL INDUSTRIAL OR DOMESTIC WASTE.**

## THERMAL DATA

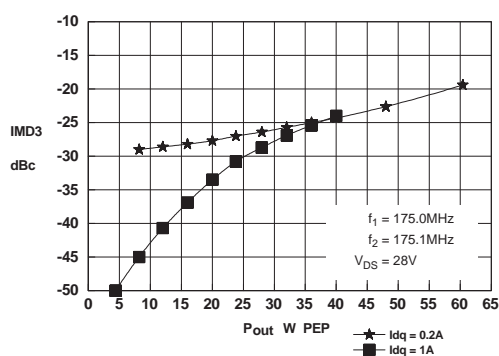
$R_{THj-case}$	Thermal Resistance Junction – Case	Max. 2.0°C / W
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**Figure 1 – Power Output and Efficiency vs. Power Input.**



**Figure 2 – Power Output & Gain vs. Power Input.**



**Figure 3 – IMD vs. Output Power.**

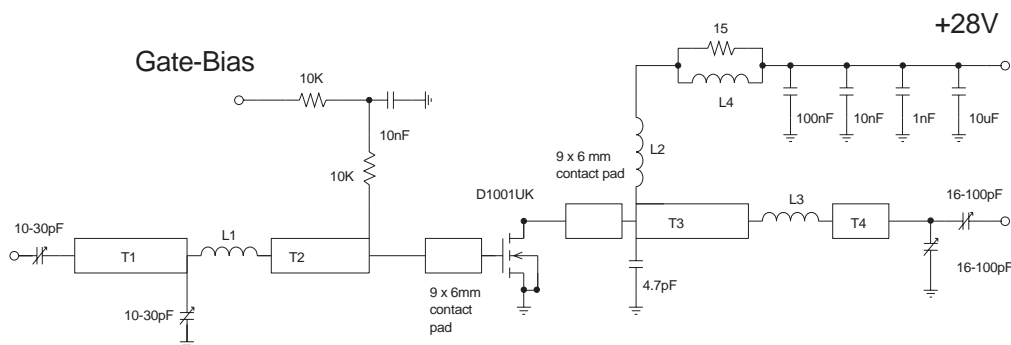
## D1002UK OPTIMUM SOURCE AND LOAD IMPEDANCE

Frequency MHz	$Z_S$ $\Omega$	$Z_L$ $\Omega$
175MHz	$3.8 + j6.5$	$4.6 + j0.4$

## Typical S Parameters

! Vds=28V Idq=0.2A  
# MHz S MA R 50

!Freq MHz	S11 mag ang	S21 mag ang	S12 mag ang	S22 mag ang
50	0.76 -144	15.6 86	0.026 1	0.58 -119
100	0.79 -155	7.1 61	0.021 -9	0.66 -132
150	0.84 -163	4.2 43	0.012 -3	0.74 -144
200	0.87 -169	2.7 33	0.009 47	0.81 -154
250	0.90 -176	1.9 23	0.016 76	0.85 -163
300	0.92 177	1.5 20	0.025 87	0.88 -172
350	0.94 170	1.1 11	0.033 85	0.91 -180
400	0.96 163	0.9 6	0.046 82	0.94 172
450	0.97 156	0.7 -2	0.051 78	0.96 165
500	0.98 150	0.6 -8	0.062 76	0.98 157
550	0.98 144	0.4 -12	0.068 74	0.98 152
600	0.98 141	0.4 -14	0.078 67	0.98 148



## D1002UK 175MHz TEST FIXTURE

Substrate 1.6mm PTFE/glass, Er=2.5

All microstrip lines W=4.4mm

T1 10mm  
T2 13mm  
T3 12mm  
T4 4mm

L1 1.5 turns 22swg enamelled copper wire, 6mm i.d.  
L2 10 turns 19swg enamelled copper wire, 6mm i.d.  
L3 1.5 turns 22swg enamelled copper wire, 6mm i.d.  
L4 13.5 turns 19swg enamelled copper wire on Siemens B64920A618X830 ferrite core