OBSOLETE

ANALOG DEVICES

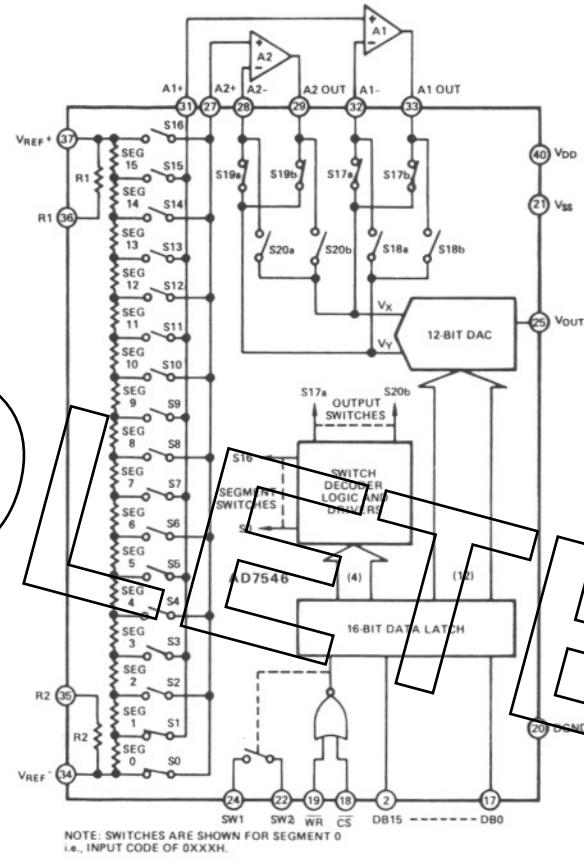
CMOS 16-Bit Voltage Out DAC*

AD7546

FEATURES

- Monotonic to 16 Bits Over Temperature
- On-Chip Deglitch Switch
- Unipolar and Bipolar Operation
- Microprocessor Compatible
- TTL/CMOS Compatible Latched Inputs
- Voltage Output (Constant Output Impedance)
- Low Cost
- Low Power Consumption: 50mW typ

AD7546 FUNCTIONAL BLOCK DIAGRAM



NOTE: SWITCHES ARE SHOWN FOR SEGMENT 0 i.e., INPUT CODE OF 0XXXH.

GENERAL DESCRIPTION

The AD7546 is a 16-bit voltage-output DAC with input data latches for interfacing to 16-bit microprocessors. It uses a novel design consisting of a 12-bit R-2R DAC, operated in the voltage switching mode, which is supplied with a reference voltage from a 4-bit segment DAC under the control of the four most significant bits. A monolithic CMOS device, the AD7546 offers outstanding differential nonlinearity specifications and monotonicity from 14 to 16 bits.

An on-chip deglitch switch which is synchronized with the latch loading signal is provided for use with track/hold circuits.

ORDERING INFORMATION

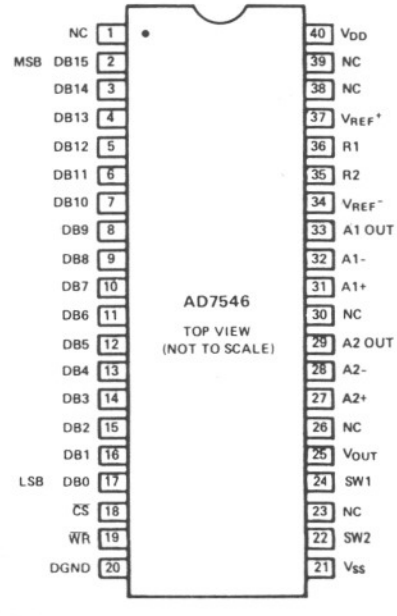
Relative Accuracy	Differential Nonlinearity	Temperature Range - Package: Plastic 0 to +70°C	Temperature Range - Package: Ceramic -25°C to +85°C	Monotonic Range
±0.05%	±0.006%	AD7546JN	AD7546AQ	14 Bits
±0.012%	±0.0015%	AD7546KN	AD7546BQ	16 Bits

PACKAGE IDENTIFICATION[1]

Suffix "D": – Ceramic DIP (D40A)
Suffix "N": – Plastic DIP – (N40A)

[1] See Section 19 for package outline information.

PIN CONFIGURATION



*Patent Pending.

SPECIFICATIONS (VDD = +15V, V_{SS} = -5V, (V_{REF}+ = +4V, V_{REF}- = -4V, A1, A2 = AD544K, unless otherwise noted)

Parameter	Limit at T_A = +25°C	Limit at T_A = T_{min}, T_{max} [1]	Units	Conditions/Comments
ACCURACY				
Resolution				
All Grades	16	16	Bits	
Relative Accuracy				
AD7546JN, AD	±0.05	±0.05	% FSR max[2]	This is an end-point linearity specification
AD7546KN, BD	±0.012	±0.012	% FSR max	assuming zero offset voltage for A1, A2.
Differential Nonlinearity				
AD7546JN, AD	±0.006	±0.006	% FSR max	Guaranteed monotonic to 14 bits (DB0 and DB1 = 0).
AD7546KN, BD	±0.0015	±0.0015	% FSR max	Guaranteed monotonic to 16 bits over temperature.
Gain Error[3]				
Positive Full Scale	-0.02	-0.02	% FSR max	DAC latches loaded with $FFFF_H$
Negative Full Scale	-0.02	-0.02	% FSR max	DAC latches loaded with 0000_H
Gain T.C.[4,5]	±2	±2	ppm of FS/°C max	
dc Supply Rejection[5]				
$\Delta Gain/\Delta V_{DD}$	100	100	µV per V typ	V_{DD} = +14.5V to +15.5V
DYNAMIC PERFORMANCE				
Voltage Settling Time[5,6]	4	4	µs typ	To 0.01% of final value.
	5	5	µs typ	To 0.003% of final value.
	10	10	µs typ	To 0.00076% of final value. Measured using the circuit of Figure 6.
SWITCHING CHARACTERISTICS[5,7]				With +5V input logic levels.
t_{CWS}	0	0	ns min	Chip select to WRITE setup time
t_{CWH}	0	0	ns min	Chip select to WRITE hold time
t_{WR}	400	600	ns min	WRITE pulse width
t_{DS}	200	300	ns min	Data setup time
t_{DH}	100	150	ns min	Data hold time
REFERENCE INPUTS				
Resistance				
V_{REF}^+ to V_{REF}^-	20/32/50	20/32/50	kΩ, min/typ/max	Typical Resistance TC is -300ppm/°C
R1, R2	20/30/50	20/30/50	kΩ, min/typ/max	
R1, R2 Match				
AD7546JN, AD	0.5	0.5	% max	Typical TC of R1, R2 match is ±1ppm/°C
AD7546 KN, BD	0.1	0.1	% max	
Voltage Range				
V_{REF}^+	+5	+5	V max	The AD7546 is tested with V_{REF}^+ =
V_{REF}^-	-5	-5	V max	+4V, V_{REF}^- = -4V
ANALOG OUTPUT				
R_{OUT} (Output Resistance)	10/15/25	10/15/25	kΩ, min/typ/max	
C_{OUT} (Output Capacitance)[5]	8	8	pF max	
DEGLITCH SWITCH				
R_{ON}	300/600	450/900	Ω typ/max	V_{SW} = ±4V, I_{SW} = 100µA
$I_{LEAKAGE}$, SW2 (pin 22)	1	10	nA max	Off switch leakage. V_{SW1} = ±4V, V_{SW2} = ∓4V.
LOGIC INPUTS				
V_{IH}	2.4	2.4	V min	
V_{IL}	0.8	0.8	V max	
I_{IN} (Input Leakage Current)	1	1	µA max	V_{IN} = 0V or V_{DD}
C_{IN} (Input Capacitance)[5]	8	8	pF max	
Input Coding	16-Bit Unipolar Binary			See Figure 7
	16-Bit Offset Binary			See Figure 8
POWER SUPPLY				
V_{DD}	+15	+15	V	±5% for specified performance
V_{SS}	-5	-5	V	±5% for specified performance
I_{DD}	4	4	mA max	V_{IN} = V_{IL} or V_{IH}
I_{DD}	200	200	µA max	V_{IN} = 0V or V_{DD}, $\overline{CS}$ = $\overline{WR}$ = 0V
I_{SS}	100	100	µA max	

NOTES

[1] Temperature ranges as follows: AD7546JN, KN; 0 to +70°C
AD7546AD, BD; -25°C to +85°C

[2] FSR is Full Scale Range.

[3] These gain error specifications have assumed an input offset voltage for A2 of 0V. Actual gain error figures should include amplifier A2 input offset voltage.

[4] Gain TC specifications have assumed a zero input offset voltage drift with temperature for A2. Actual gain TC figures should include amplifier A2 drift with temperature.

[5] Guaranteed but not tested.

[6] Voltage settling time will be a function of the time constant RC seen at the buffer amplifier inputs. The resistance component of this time constant is the equivalent output impedance of the resistor string and will vary depending on which segment is decoded. Maximum equivalent resistance occurs at mid-scale. Worst case settling thus occurs from zero to mid-scale or from full-scale to mid-scale.

[7] +15V logic can be used to reduce power dissipation but no improvement is achieved in the timing specifications. All control signals are measured with $t_r = t_f$ = 20ns for +5V logic and timed from $\frac{(V_{IH} + V_{IL})}{2}$. Data is timed from V_{IH} or V_{IL}. Sample tested at +25°C to ensure conformance.

Specifications subject to change without notice.

CAUTION:
ESD (Electro-Static-Discharge) sensitive device. The digital control inputs are zener protected; however, permanent damage may occur on unconnected devices subject to high energy electrostatic fields. Unused devices must be stored in conductive foam or shunts. The protective foam should be discharged to the destination socket before devices are removed.

ABSOLUTE MAXIMUM RATINGS

(T_A = +25°C unless otherwise noted)

(Note that cavity lid on Ceramic Package is Electrically Connected to V_{DD})

V_{DD} (Pin 40) to DGND . . . . . 0V, +17V
V_{SS} (Pin 21) to DGND . . . . . 0V, –7V
V_{REF}^+ (Pin 37) to DGND . . . . . V_{DD}, V_{REF}^-
V_{REF}^- (Pin 34) to DGND . . . . . V_{SS}, V_{REF}^+
R1 (Pin 36) to DGND . . . . . ±25V
R2 (Pin 35) to DGND . . . . . ±25V
*DB12 LOW (S17, S19 Closed)
A1 – (Pin 32) or A1 Out (Pin 33)
to A2 – (Pin 28) or A2 Out (Pin 29) . . . . . –0.3V, +5V
*DB12 HIGH (S18, S20 Closed)
A2 – (Pin 28) or A2 Out (Pin 29)
to A1 – (Pin 32) or A1 Out (Pin 33) . . . . . –0.3V, +5V
A1 + (Pin 31), A2 + (Pin 27) to DGND . . . . . V_{SS}, V_{DD}
V_{OUT} (Pin 25) to DGND . . . . . ±25V
SW1 (Pin 24), SW2 (Pin 22) to DGND . . . . . V_{SS}, V_{DD}
Digital Inputs (Pins 2 –19) to DGND . . . . . –0.3V, +17V
Power Dissipation (Package)
Plastic (AD7546JN, KN)
Up to +50°C 1200mW
Derates above +50°C by . . . . . 12mW/°C
Ceramic (AD7546AD, BD)
Up to +50°C 1000mW
Derates above +50°C by . . . . . 10mW/°C

***The absolute maximum rating refers to the voltage V_X–V_Y across the inputs of the 12-bit DAC. See Functional Diagram of Figure 2.**

STRESS

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other condition above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ACCURACY SPECIFICATIONS

Two types of nonlinearity errors exist in D/A converters, relative accuracy and differential nonlinearity. Relative accuracy is the error resulting from departure of the DAC transfer characteristic from the ideal straight line drawn between measured zero and measured full scale.

Differential Nonlinearity (DNL) is the difference between the measured output voltage change between two adjacent input codes and the ideal change of 1LSB. A specified DNL of ±1 LSB guarantees monotonicity (i.e. the output voltage will never decrease for any increase in input code). To ensure that the output voltage will always increase when the input code is increased requires a DNL specification of less than ±1LSB. This point is illustrated in Figure 1.

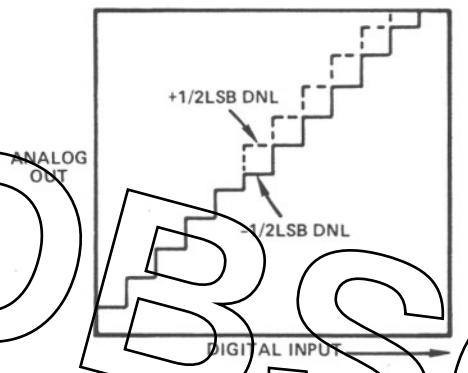


Figure 1a. ±1/2LSB Differential Nonlinearity

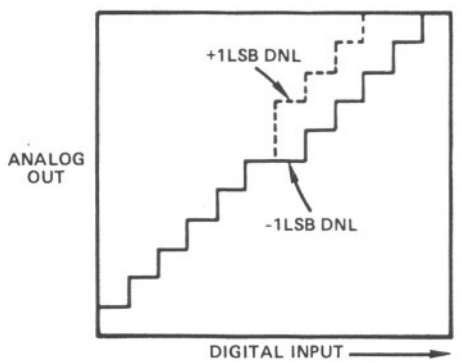


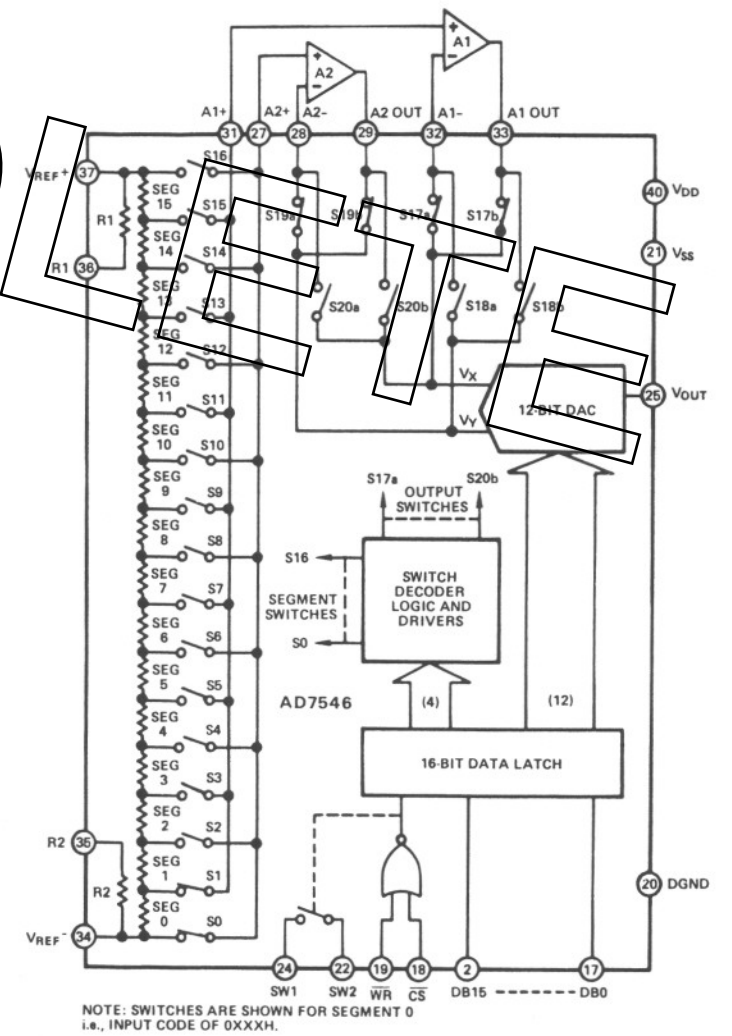
Figure 1b. ±1LSB Differential Nonlinearity

Many applications require high resolution DACs with guaranteed monotonicity (but not necessarily with an equivalent relative accuracy) for fine control of temperature, position and other physical parameters. Good differential nonlinearity is essential in such systems to maintain an even degree of control over the full range. Monotonicity is particularly important in feedback systems where nonmonotonic behavior constitutes positive feedback which may lead to catastrophic results. To ensure monotonic behavior of a particular device, only those bits which are guaranteed monotonic for that grade should be exercised e.g., for the AD7546JN (14-bit monotonic), DB0 and DB1 should be tied LOW and DB2 – DB15 exercised.

THEORY OF OPERATION OF THE AD7546

The traditional solution to achieving high resolution DACs with guaranteed monotonicity is the R-2R ladder approach. This technique usually constrains the converter to have ±1/2LSB nonlinearity in order to guarantee monotonicity, which in turn requires very tight resistor matching and tracking. The resistor ladder tolerance is most critical for the major carry where, in a 16-bit DAC, the 15LSBs turn off and the most significant bit turns on. If the MSB is more than 0.0015% low, the converter will be nonmonotonic. Table I shows the maximum tracking error which can be allowed over a 60°C range to maintain monotonicity, which is ±1LSB DNL. A standard R-2R approach therefore imposes severe constraints on resistor matching.

The design technique used in the AD7546 sidesteps the penalty inherent in the R-2R design (i.e. that tight differential nonlinearity figures require tight nonlinearity figures). The block diagram of the AD7546 is shown in Figure 2. The top four bits of the 16-bit input data are decoded to select, via the segment switches, one of the 16 voltage segments available along the resistor chain. This voltage segment, $\frac{V_{REF}^{+} - V_{REF}^{-}}{16}$,



NOTE: SWITCHES ARE SHOWN FOR SEGMENT 0 i.e., INPUT CODE OF 0XXXH.

Figure 2. AD7546 Functional Diagram

Converter Type	Initial Matching Required for:		Tracking Required for:	
	±1LSB DNL	±1/2LSB DNL	±1LSB DNL (1/2LSB INITIAL DNL)	±1/2LSB DNL (1/4LSB INITIAL DNL)
Straight R-2R	±0.0015%	±0.00076%	±0.127ppm/°C	±0.063ppm/°C
Segmented 4 Bits + 12 Bits	±0.024%	±0.012%	±2ppm/°C	±1ppm/°C

Table I. Resistor Matching Requirements for 16-Bit DAC

is used as a voltage reference to feed a 12-bit R-2R type D/A converter operating in the voltage switching mode (Reference 1). From Figure 2 the reference voltage is the voltage between V_X and V_Y and is always equal to one voltage segment. The output of the D/A converter may be expressed as follows:

$$V_{OUT} = V_Y + D(V_X - V_Y)$$

where D is the lower 12-bit digital code, V_X is the higher segment voltage and V_Y is the lower segment voltage. The 12-bit D/A converter reference inputs, V_X and V_Y, are connected to the two resistor chain nodes which define the segment of interest and the 12-bit D/A converter interpolates between these two points.

Thus the 65,536 output levels available from the 16-bit DAC are composed of 16 groups of 4,096 steps each. Since the major carry of the 12-bit DAC is repeated in each of the 16 segments it requires sixteen times lower initial resistor accuracy and tracking to maintain a given differential nonlinearity over temperature. The resistors that determine monotonicity are in the 12-bit DAC. The truth table for the switch decoder is shown in Table II.

DB15	DB14	DB13	DB12	Segment Switches	Output Switches
1	1	1	1	S15, S16	S18, S20
1	1	1	0	S14, S15	S17, S19
1	1	0	1	S13, S14	S18, S20
1	1	0	0	S12, S13	S17, S19
1	0	1	1	S11, S12	S18, S20
1	0	1	0	S10, S11	S17, S19
1	0	0	1	S9, S10	S18, S20
1	0	0	0	S8, S9	S17, S19
0	1	1	1	S7, S8	S18, S20
0	1	1	0	S6, S7	S17, S19
0	1	0	1	S5, S6	S18, S20
0	1	0	0	S4, S5	S17, S19
0	0	1	1	S3, S4	S18, S20
0	0	1	0	S2, S3	S17, S19
0	0	0	1	S1, S2	S18, S20
0	0	0	0	S0, S1	S17, S19

Table II. Truth Table for Switch Decoder

Since the input impedance of the D/A converter is low and varies with code, two external amplifiers are used to buffer the selected reference segment from the D/A converter. The buffer amplifiers, A1, A2, could give rise to differential nonlinearity if connected directly to V_X and V_Y and stepped up the ladder.

For example consider A1 and A2 to have input offset voltages V_{OS1} and V_{OS2} respectively, then the first major carry from segment 0 to segment 1 occurs as follows:

Segment 0: $V_X = V_1 + V_{OS1}$, $V_Y = V_O + V_{OS2}$

$$V_{OUT} = V_0 + V_{OS2} + (1 - 1/2^{12})[(V_1 + V_{OS1}) - (V_O + V_{OS2})]$$

$$V_{OUT} = V_1 + V_{OS1} - \frac{(V_1 - V_0)}{2^{12}} - \frac{(V_{OS1} - V_{OS2})}{2^{12}}$$

Segment 1: $V_X = V_2 + V_{OS1}$, $V_Y = V_1 + V_{OS2}$

$$V_{OUT} = V_1 + V_{OS2}$$

The error term generated by this segment change is:

$$V_{OS2} - V_{OS1} + \frac{(V_{OS1} - V_{OS2})}{2^{12}}$$

It can be seen that V_{OS1} and V_{OS2} must match to within one LSB to guarantee monotonic behavior at this transition.

To overcome this problem the AD7546 circuit interchanges the amplifiers at each segment transition and, as a result, differential nonlinearity can be guaranteed for a very large range of V_{OS}. Switching inside the feedback loop of the op amp is used to remove the effect of switch R_{ON}. With this technique the first major carry from segment 0 to segment 1 now occurs as follows:

Segment 0: $V_X = V_1 + V_{OS1}$, $V_Y = V_0 + V_{OS2}$

$$V_{OUT} = V_1 + V_{OS1} - \frac{(V_1 - V_0)}{2^{12}} - \frac{(V_{OS1} - V_{OS2})}{2^{12}}$$

Segment 1: Interchange amplifiers

$V_X = V_2 + V_{OS2}$, $V_Y = V_1 + V_{OS1}$

$V_{OUT} = V_1 + V_{OS1}$

The error term at the transition from one segment to another is now $(V_{OS1} - V_{OS2})/4096$ which gives very good differential nonlinearity for reasonable offsets. At the next segment transition, $V_X = V_3 + V_{OS1}$, $V_Y = V_2 + V_{OS2}$ and so on through each segment. The amplifiers are interchanged via output switches S17 – S20, see Table II.

In the segmented DAC the precision of the resistor chain determines integral nonlinearity only. If the resistor chain is trimmed for perfect matching such that Vn + 1 = Vn = Vn – 1 = Vsegment, then the resulting nonlinearity due to amplifier offset voltage corresponds to a gain error in adjacent segments of $V_{OS1} - V_{OS2}$, see Figure 3. This term may be nulled to zero with offset adjustment of one op amp.

This adjustment is facilitated by tying $V_{REF}+$ and $V_{REF}-$ to ground, tying DB0 through DB11 and DB13 through DB15 to digital ground and toggling DB12. The AD7546 output (V_{OUT}, pin 25) will have a square wave at the toggling frequency with an amplitude of $V_{OS1} - V_{OS2}$. This can be adjusted to zero as mentioned.

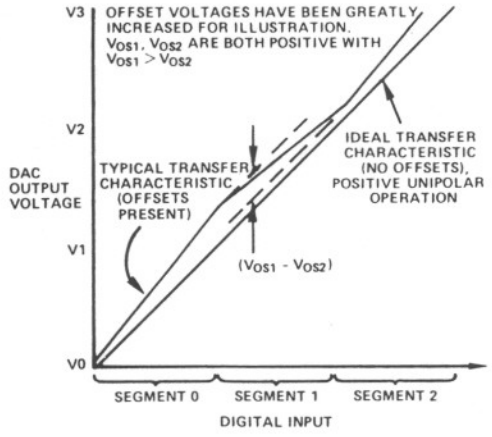


Figure 3. Positive Unipolar Transfer Characteristic (V_{REF}^- = 0V, V_{REF}^+ = +4V) Exaggerated to Show the Effect of Amplifier Offset Voltages

If offsets are equal in magnitude and sign, the result is a constant offset shift in the D/A transfer function and the device will have true 16-bit linearity.

(Reference 1: Analog Dialogue, Volume 14, Number 1 P16-17.)

OP-AMP SELECTION

Amplifiers A1 and A2 determine the overall performance of the AD7546. Since these are external to the converter, the user can choose amplifiers which will tailor the system performance to the required accuracy. Input bias current, open-loop gain and offset voltage of the amplifiers affect relative accuracy. Differential nonlinearity is affected by input bias current. (The offset voltage contribution to linearity has already been dealt with on previous pages.) The following two expressions deal with the relationship between device linearity and input bias current.

For Differential Nonlinearity:

$$\text{MAX DNL (in LSBs)} = \frac{14}{16} \cdot \frac{(I_{BIAS})(R)}{1LSB}$$

For Relative Accuracy:

$$\text{MAX NL (in LSBs)} = \frac{15}{2} \cdot \frac{(I_{BIAS})(R)}{1LSB}$$

Where I_{BIAS} = Input bias current for the noninverting input terminal of A1 or A2 in amps

$$1LSB = \frac{V_{REF}+ - V_{REF}-}{2^N} \text{ volts}$$

N is determined by the required system resolution up to N = 16.

R = R segment, typically 2kΩ

Low bias current op amps, BIFET or Super-Beta types, should be used such as the AD542K, AD544K, AD517K, TL071, TL081. Table III lists some important parameters against various op amps. Note that the AD7546 output settling time is dependent upon the op amps used. The figures in column two give the additional offset voltage contribution to nonlinearity of A1 and A2.

A1, A2	Maximum Additional Nonlinearity	Settling Time (μs) to ±1/2LSB 14 Bits	16 Bits
2 X AD544KH	±0.01%	15	35
1 X TL072BCP (Dual)	±0.05%	5	10
2 X AD517JH	±0.003%	90	100
1 X AD644JH (Dual AD544)	±0.01%	15	35
2 X LF256	±0.05%	5	10

Settling time measurements were made with a similar op amp to buffer V_{OUT} (A4 in Figure 8)

Table III. AD7546 Performance vs. A1, A2

DATA LOADING AND DEGLITCH SWITCH

The AD7546 timing specifications are included on Specifications page and illustrated here in Figure 4. Signals $\overline{CS}$ and $\overline{WR}$ have the same interpretation as in normal microprocessor systems. When both $\overline{CS}$ and $\overline{WR}$ are low the input latches are transparent and the DAC output voltage follows the input data. With $\overline{CS}$ low, the input data is latched on the rising edge of $\overline{WR}$.

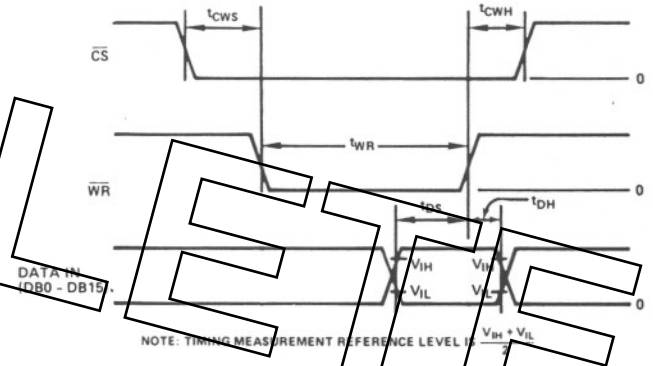


Figure 4. AD7546 Timing Waveforms

Included on the chip is an SPST switch intended for use in a Track/Hold circuit to remove glitches from the DAC output and simplify low-pass filtering of the reconstructed output voltage. The switch is synchronized with the latch loading signals, being open when both $\overline{CS}$ and $\overline{WR}$ inputs are low. The internal logic of the AD7546 ensures that the switch opens before data to the latches can change. To function as a Track/Hold the switch is placed in series with the DAC output as shown in Figure 5. Pin 23 is a no-connect pin which should be grounded to minimize any feedthrough resulting from stray capacitances at the two switch terminals. The switch should be used with pin 24 as the input and pin 22 as the output. When the switch is open the Hold capacitor stores the previous output voltage of the DAC. The $\overline{WR}$ pulse should be of sufficient duration to allow the DAC to settle to its new analog output and for all glitches to have settled out. Driving the $\overline{WR}$ input from a one-shot will ensure sufficient settling time.

When $\overline{WR}$ returns high the switch is closed, updating the output voltage on the capacitor. Typical output waveforms using the circuit of Figure 5 are shown below.

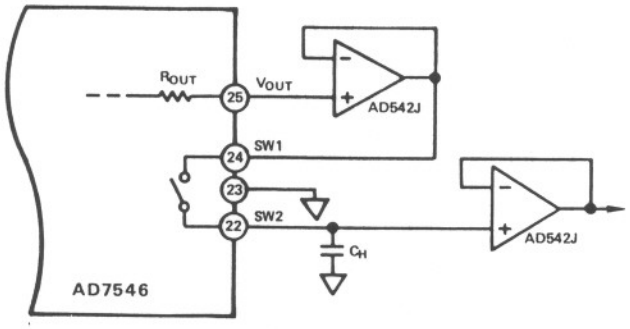
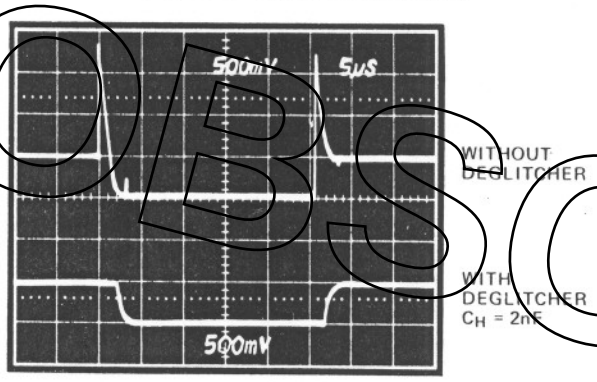


Figure 5. Track/Hold Circuit



UNIPOLAR OPERATION

Unipolar (single quadrant) operation is obtained when one end of the resistor chain is tied to ground i.e., when $V_{REF}+ = +V_{REF}$ and $V_{REF}- = 0V$ or when $V_{REF}+ = 0V$ and $V_{REF}- = -V_{REF}$. A typical unipolar circuit configuration for the AD7546 is shown in Figure 6a. In this positive unipolar application V_{SS} has been set to 0V and the AD7546 operates as a single supply device. If a full scale output is required which is different from the ideal V_{REF} – 1LSB then output amplifier A3 of Figure 6a can be configured to provide the necessary scaling. Figure 6b shows the additional components required to boost the full scale output voltage to +10V with V_{REF} = +4V. Any full scale gain error (introduced by R1, R2 tolerances) can be trimmed out by adjusting V_{REF}. Note that R1, R2 should be the same type of resistor (preferably metal film) so that their temperature coefficients match. The transfer characteristic for the circuit of Figure 6a is shown in Figure 7.

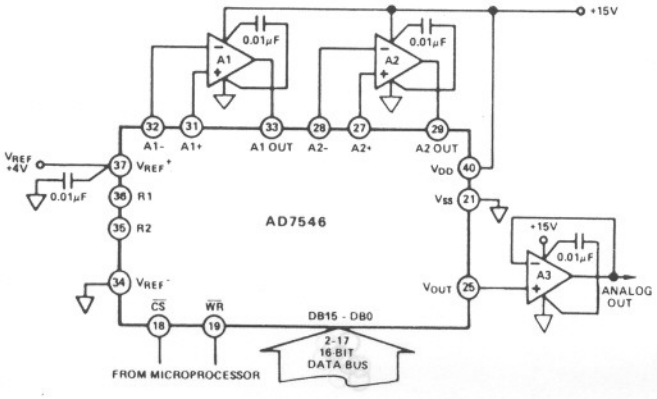


Figure 6a. Typical Unipolar Circuit Configuration for the AD7546 (Positive Reference, $V_{REF}+ = V_{REF}$, $V_{REF}- = 0V$)

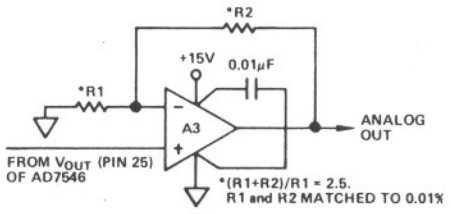


Figure 6b. Adding Gain Around A3 to Change Full Scale Output Voltage of Figure 6a.

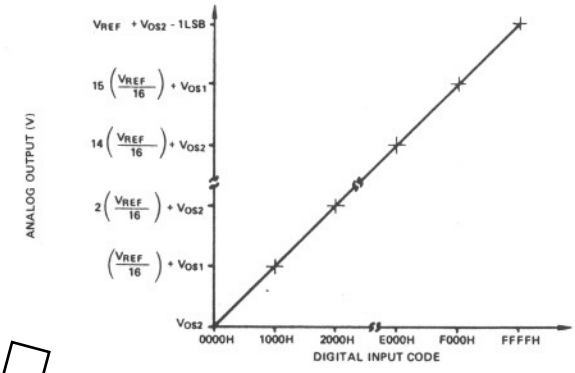


Figure 7. Unipolar Transfer Characteristic of Figure 6a.

BIPOLAR OPERATION

Bipolar (two quadrant) operation is obtained when both ends of the resistor chain are driven with voltage references of opposite polarity. A symmetrical transfer function around 0V is achieved with $|V_{REF}^+| = |V_{REF}^-|$. For this case the zero crossing occurs with DB15=1 and DB14 to DB0 all 0s. Figure 8 shows a typical bipolar circuit configuration for the AD7546 to obtain a symmetrical transfer function around 0V. Figure 9 shows the transfer characteristic of Figure 8.

Two equal trimmed resistors, R1 and R2, are included on the AD7546 to allow one reference to be generated from the other with the addition of an external amplifier (A3 in Figure 8). Note that V_{REF}^+ must always be more positive than V_{REF}^-; operation is confined to two quadrants (1st and 3rd). It is possible to use an ac reference signal with the AD7546 as long as $V_{REF}+$ always remains more positive than $V_{REF}-$.

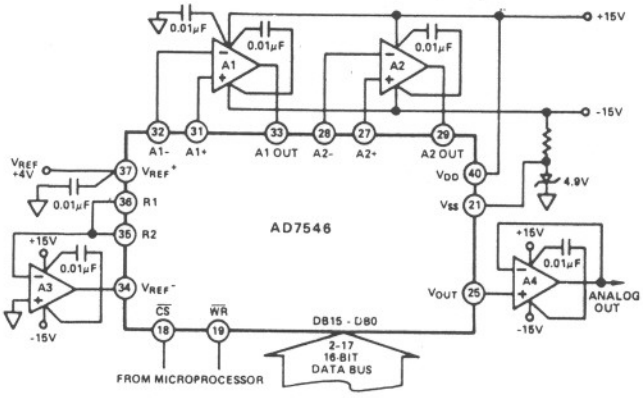


Figure 8. Typical Bipolar Circuit Configuration for the AD7546

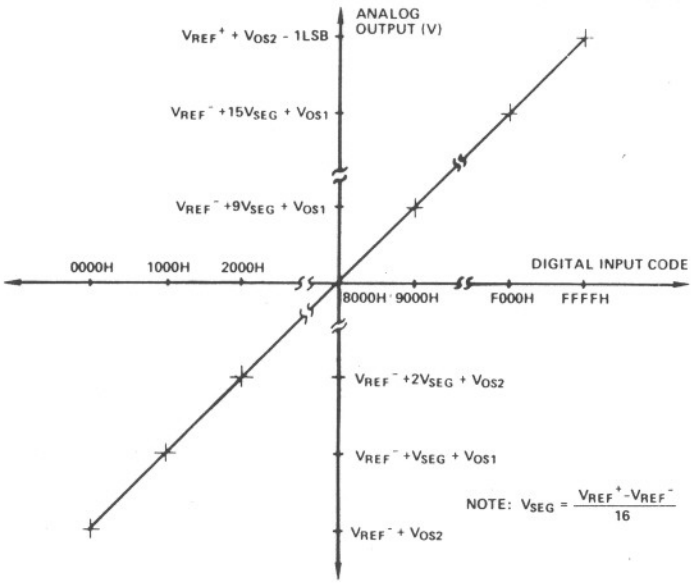


Figure 9. Bipolar Transfer Characteristic of Figure 8.

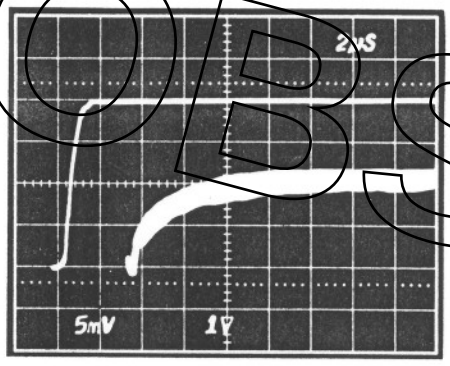


Figure 10. Typical Settling Characteristics of Figure 8 Using TL071 for Full Scale Code Change

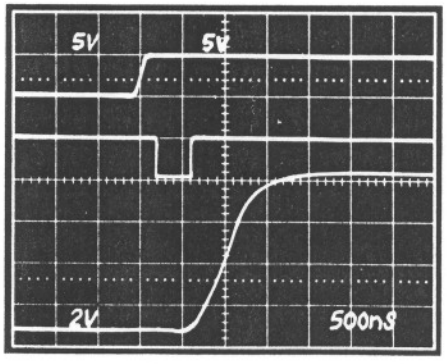


Figure 11. Typical Loading Waveforms with $\overline{CS}$ = 0V

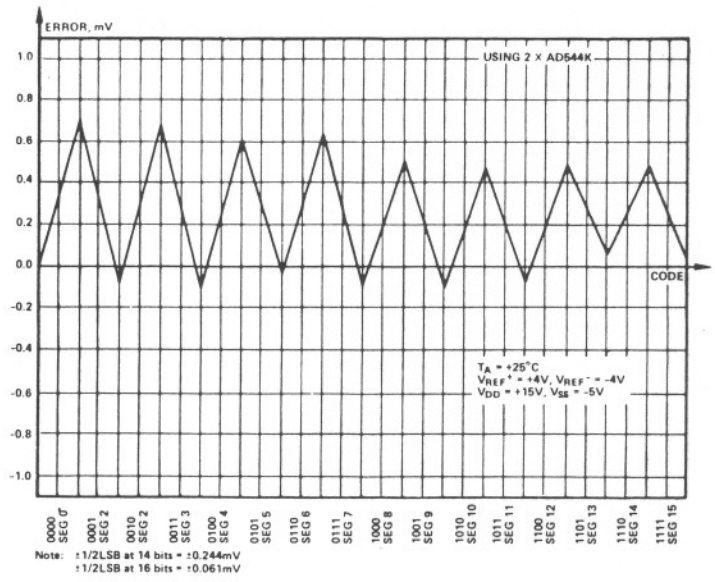


Figure 12a. Typical Error vs Input Code with A1 = A2 = AD544K

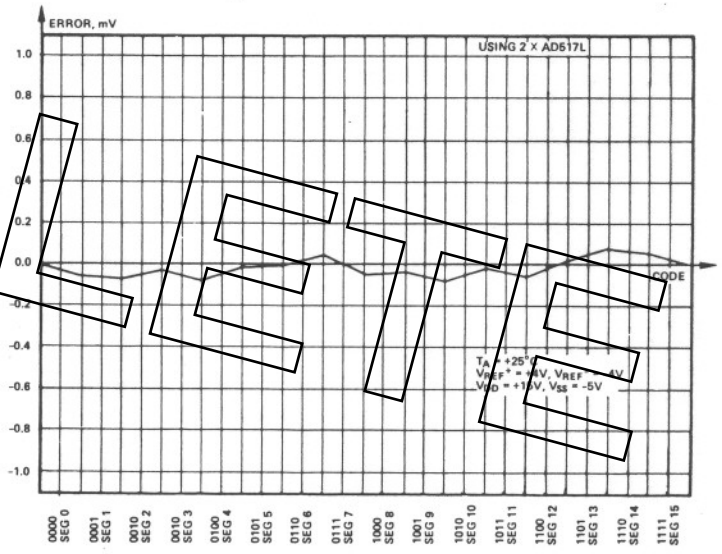
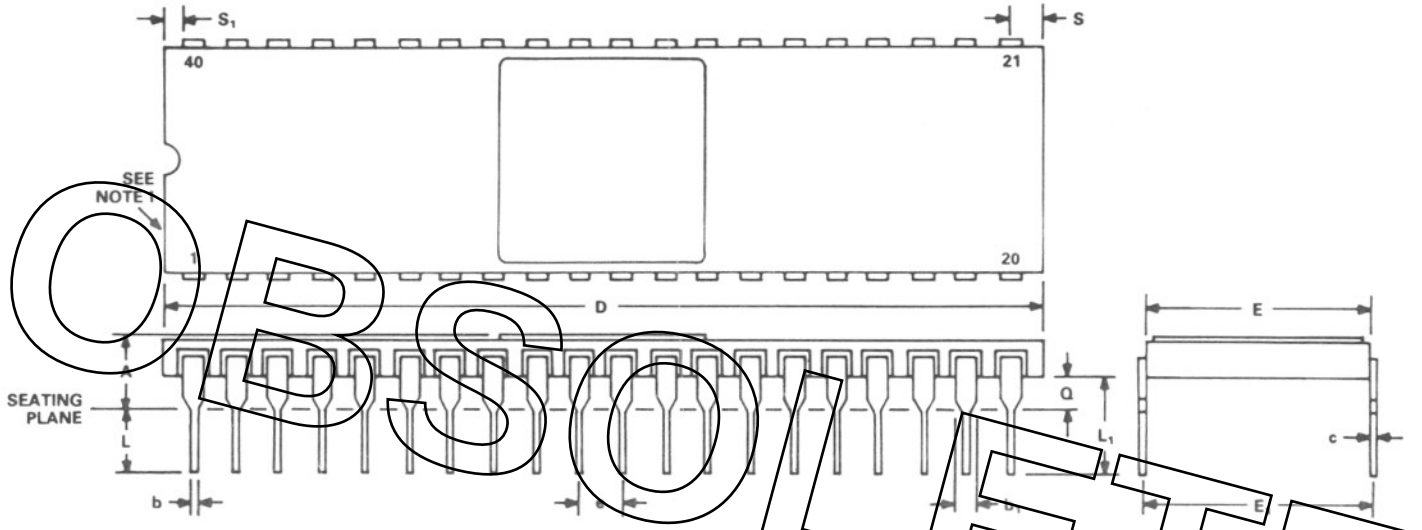


Figure 12b. Typical Error vs Input Code with A1 = A2 = AD517L

D-40

40-Lead Side Brazed Ceramic DIP



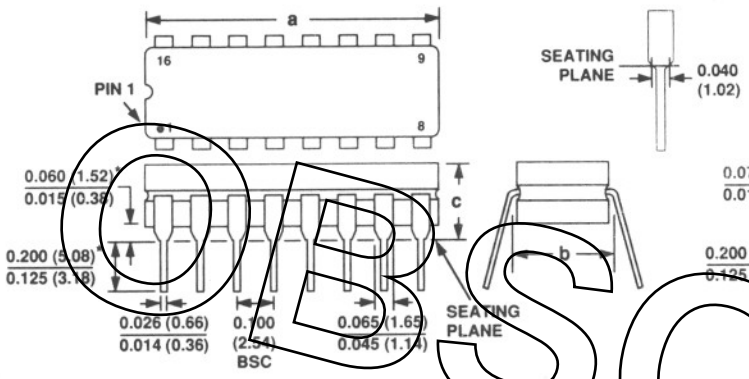
SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A		0.225		5.72	
b	0.014	0.023	0.36	0.58	6
b_1	0.030	0.070	0.76	1.78	2, 6
c	0.008	0.015	0.20	0.38	6
D		2.096		53.24	4
E	0.590	0.620	12.95	15.75	4
E_1	0.520	0.630	13.21	16.00	
e	0.090	0.110	2.29	2.79	7
L	0.125	0.200	3.18	5.08	
L_1	0.150		3.81		
Q	0.015	0.060	0.38	1.52	3
S		0.098		2.49	5
S_1	0.005		0.13		5

NOTES

1. Index area; a notch or a lead one identification mark is located adjacent to lead one.
2. The minimum limit for dimension b_1 may be 0.023" (0.58mm) for all four corner leads only.
3. Dimension Q shall be measured from the seating plane to the base plane.
4. This dimension allows for off-center lid, meniscus and glass overrun.
5. Applies to all four corners.
6. All leads – increase maximum limit by 0.003" (0.08mm) measured at the center of the flat, when hot solder dip lead finish is applied.
7. Thirty-eight spaces.

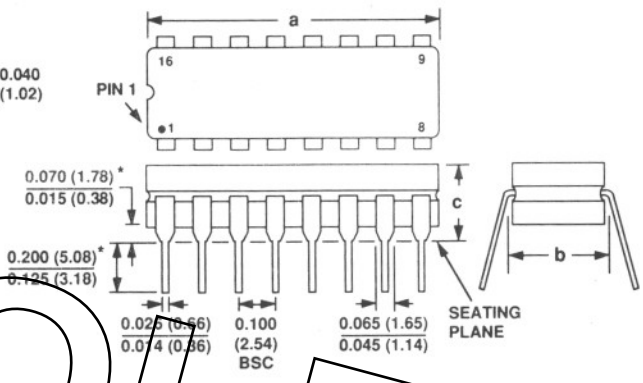
Cerdip

Q-8, Q-14, Q-16, Q-24, Q-28



* THE SEATING PLANE IS LOCATED AT THE LOWEST POINT ON THE LEAD AT WHICH THE LEAD WIDTH EXCEEDS 0.040 (1.02) INCHES

Q-18, Q-20, Q-40



* THE SEATING PLANE IS LOCATED AT THE LOWEST POINT ON THE LEAD AT WHICH THE LEAD WIDTH EXCEEDS 0.040 (1.02) INCHES

Letter Designators		Product	a*		b*		c*	
ADI	PMI	Description	Min	Max	Min	Max	Min	Max
Q-8	Z	8-Lead		0.405 (10.29)	0.290 (7.37)	0.320 (8.13)		0.200 (5.08)
Q14	Y	14-Lead		0.785 (19.94)	0.290 (7.37)	0.320 (8.13)		0.200 (5.08)
Q-16	Q	16-Lead		0.840 (21.34)	0.290 (7.37)	0.320 (8.13)		0.200 (5.08)
Q-18	X	18-Lead		0.960 (24.38)	0.290 (7.37)	0.320 (8.13)		0.200 (5.08)
Q-20	R	20-Lead		1.060 (26.92)	0.290 (7.37)	0.320 (8.13)		0.200 (5.08)
Q-24	W	24-Lead		1.280 (32.51)	0.290 (7.37)	0.320 (8.13)		0.200 (5.08)
Q-28	T	28-Lead		1.490 (37.85)	0.590 (14.99)	0.620 (15.75)		0.225 (5.72)
Q-40		40-Lead		2.096 (52.23)	0.59 (14.93)	0.63 (16.00)		0.21 (5.33)

*For complete package dimensions see reference manual or data sheet.