

AP603

High Dynamic Range 7W 28V HBT Amplifier



Applications

- Mobile Infrastructure
- High Power Amplifier (HPA)

Product Features

- 800 – 2200 MHz
- +38 dBm P1dB
- -50 dBc ACLR @ 1W P_{AVG}
- -51 dBc IMD3 @ 1W PEP
- 15% Efficiency @ 1W P_{AVG}
- Internal Active Bias
- Internal Temp Compensation
- Capable of handling 7:1 VSWR @ 28 Vcc, 2.14 GHz, 5.5W CW Pout
- Lead-free/RoHS-compliant

General Description

The AP603 is a high dynamic range power amplifier in a lead-free/RoHS-compliant 5x6mm power DFN SMT package. The single stage amplifier has excellent backoff linearity, while being able to achieve high performance for 800-2200 MHz applications with up to +38 dBm of compressed 1dB power.

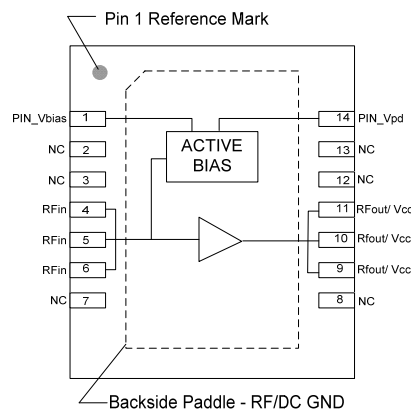
The AP603 uses a high reliability, high voltage InGaP/GaAs HBT process technology. The device incorporates proprietary bias circuitry to compensate for variations in linearity and current draw over temperature. The module does not require any negative bias voltage; an internal active bias allows the AP603 to operate directly off a commonly used high voltage supply (typically +24 to +32V). An added feature allows the quiescent bias to be adjusted externally to meet specific system requirements.

The AP603 is targeted for use as a pre-driver and driver stage amplifier in wireless infrastructure where high linearity and high efficiency is required. This combination makes the device an excellent candidate for next generation multi-carrier 3G / 4G mobile infrastructure.



5x6 mm power DFN package

Functional Block Diagram



Pin Configuration

Pin #	Symbol
1	PIN_Vbias
2, 3, 7, 8, 12, 13	N/C
4, 5, 6	RF IN
9, 10, 11	RF Output / Vcc
14	PIN_Vpd
Backside paddle	RF/DC GND

Ordering Information

Part No.	Description
AP603-F	28V HBT Amp
AP603-PCB900	869-960 MHz Evaluation board
AP603-PCB1960	1930-1990 MHz Evaluation board
AP603-PCB2140	2110-2170 MHz Evaluation board

Standard T/R size = 1000 pieces on a 7" reel.

Specifications

Absolute Maximum Ratings

Parameter	Rating
Storage Temperature	-55 to 150°C
RF Input Power (CW tone), P_{in}	Input P6dB
Breakdown Voltage C-B, BV_{CBO}	80 V @ 0.1 mA
Breakdown Voltage C-E, BV_{CEO}	51 V @ 0.1 mA
Quiescent Bias Current, I_{CQ}	320 mA
Power Dissipation, P_{DISS}	9.5 W

Operation of this device outside the parameter ranges given above may cause permanent damage.

Recommended Operating Conditions

Parameter	Min	Typ	Max	Units
V_{cc}		+28		V
I_{cq}		165		mA
T_J (for $>10^6$ hours MTTF)			192	°C
Operational Temperature	-40	+25	+85	°C

Electrical specifications are measured at specified test conditions. Specifications are not guaranteed over all recommended operating conditions.

Electrical Specifications

Test Conditions: $V_{CC} = +28$ V, $V_{PD} = 5$ V, $I_{CQ} = 165$ mA, $T = 25^\circ\text{C}$ using a tuned application circuit.

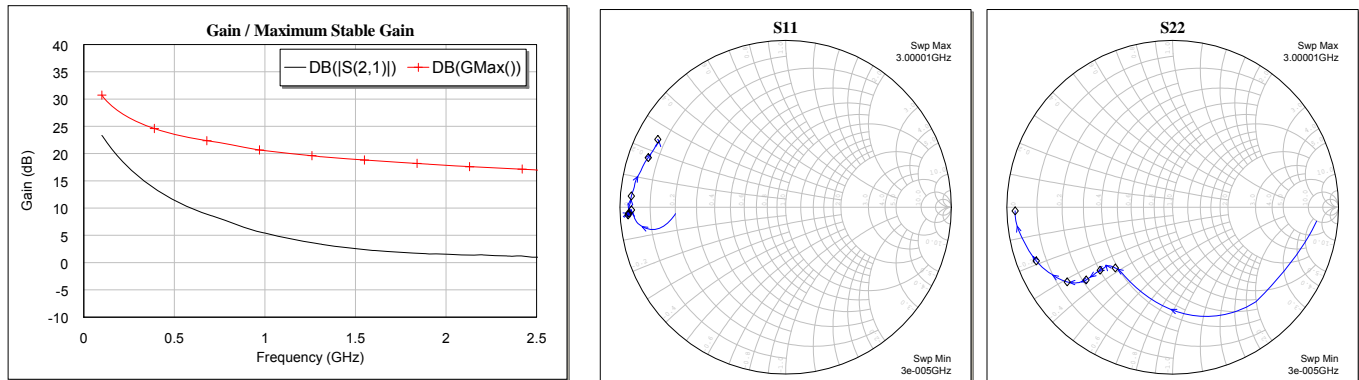
Parameter	Conditions	Min	Typical	Max	Units
Operational Bandwidth		800		2200	MHz
Test Frequency			2140		MHz
Power Gain			11.9		dB
Input Return Loss			15		dB
Output Return Loss			9.5		dB
ACLR @ 28 dBm Output Power	See Note 1.		-50.6		dBc
IMD3 @ +30 dBm PEP	See Note 2.		-50		dBc
PIN_ V_{pd} Current, I_{pd}			4		mA
Operating Current, I_{cc} @ 30 dBm Output Power	See Note 1.		232		mA
Collector Efficiency @ 30 dBm Output Power	See Note 1.		14.5		%
Output P1dB			+37.6		dBm
Quiescent Current, I_{cq}			165		mA
V_{pd}			+5		V
V_{cc}			+28		V
Thermal Resistance (jnc to case) θ_{jc}				8.7	°C/W

Notes:

- Using W-CDMA 3GPP Test Model 1+64 DPCH, PAR = 8.6 dB @ 0.01% Probability, 3.84 MHz BW
- IMD3 is measured with 1 MHz tone spacing.
- The reference designs shown in this datasheet have the device optimized for WCDMA ACLR performance at +25° C. Biasing for the amplifier is suggested at $V_{cc} = +28$ V, $V_{pd} = +5$ V and $I_{cq} = 165$ mA to achieve the best tradeoff in terms of efficiency and linearity. Increasing I_{cq} will improve upon the device linearity (IMD3 and ACLR), but will decrease the efficiency performance slightly.

Device Characterization Data

S-Parameters ($V_{CC} = +28$ V, $V_{pd} = 5$ V, $I_{CQ} = 165$ mA, $T = 25$ °C, unmatched 50 ohm system, calibrated to device leads)



Note:

The gain for the unmatched device in 50 ohm system is shown as the trace in black color. For a tuned circuit for a particular frequency, it is expected that actual gain will be higher, up to the maximum stable gain. The maximum stable gain is shown in the marked red line. The impedance plots are shown from 50 – 3000 MHz, with markers placed at 0.5 – 3.0 GHz in 0.5 GHz increments.

S-Parameter Data

$V_{CC} = +28$ V, $V_{pd} = 5$ V, $I_{CQ} = 165$ mA, $T = 25$ °C, unmatched 50 Ohm system, calibrated to device leads

Freq (MHz)	S11 (dB)	S11 (ang)	S21 (dB)	S21 (ang)	S12 (dB)	S12 (angle)	S22 (dB)	S22 (ang)
50	-2.63	-169.40	25.54	146.01	-40.50	55.97	-1.32	-45.78
100	-1.78	-170.62	23.33	132.51	-38.11	39.21	-3.07	-67.75
200	-0.92	-173.99	19.08	109.79	-36.04	21.60	-5.00	-104.04
400	-0.64	-177.96	13.40	93.01	-35.59	9.15	-6.06	-129.02
600	-0.53	-178.87	9.88	85.15	-35.72	3.39	-5.82	-136.33
800	-0.52	-178.84	7.52	79.52	-35.90	6.93	-5.38	-138.25
1000	-0.46	-177.79	5.42	74.40	-35.68	5.88	-4.77	-139.20
1200	-0.44	-177.25	4.01	69.71	-35.62	3.23	-4.16	-139.65
1400	-0.38	-176.83	2.93	64.99	-35.48	1.79	-3.62	-139.95
1600	-0.39	-177.55	2.22	59.81	-35.13	-0.56	-3.12	-140.63
1800	-0.48	-179.87	1.77	52.82	-34.75	-4.12	-2.63	-142.14
2000	-0.59	175.92	1.54	44.04	-34.21	-10.23	-2.19	-144.85
2200	-0.73	170.02	1.41	33.03	-33.63	-18.12	-1.74	-149.24
2400	-0.97	163.30	1.23	19.79	-33.13	-29.67	-1.28	-155.12
2600	-1.21	157.14	0.75	3.56	-32.89	-43.94	-0.90	-162.55
2800	-1.28	153.30	0.03	-14.33	-33.04	-61.10	-0.57	-170.87
3000	-1.18	152.21	-0.89	-34.56	-33.44	-81.90	-0.45	-178.70

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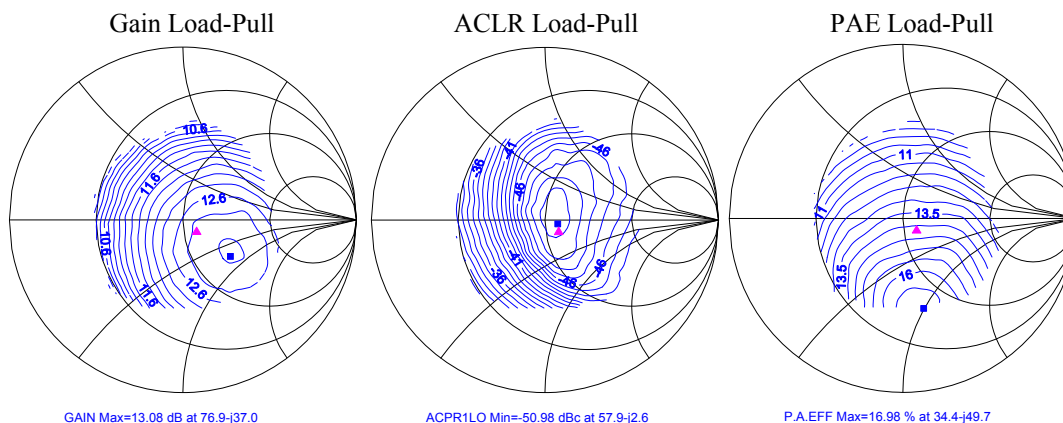
Load-Pull Data

Test condition: Output Power = 29.5 dBm, $V_{CC} = +28$ V, $I_{CQ} = 160$ mA, $Z_S = 50 \Omega$

Test signal = W-CDMA (PAR=8.6dB @ 0.01% Probability), 2140 MHz

The reference plane is at the AP603-PCB2140 eval board's SMA connectors.

The plots are shown to detail the optimization of the ACLR performance.



Evaluation Board Bias Procedure

The following bias procedure is recommended to ensure proper functionality of AP603 in a laboratory environment. The sequencing is not required in the final system application.

Bias.	Voltage (V)
V _{CC}	+28
V _{bias}	+5

Turn-on Sequence:

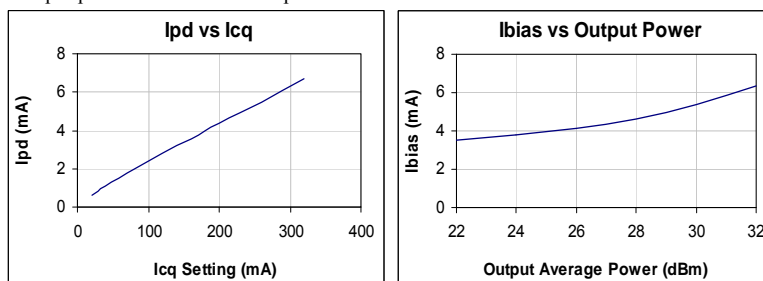
1. Attach input and output loads onto the evaluation board.
2. Turn on power supply $V_{CC} = +28$ V. Pin_Vbias is connected to 28V supply through dropping resistor. At this point, the only current drawn by the device is leakage current ($< 25 \mu$ A).
3. Turn on power supply $V_{PD} = +5$ V. Power supply V_{CC} should now be drawing typical $I_{CQ} = 165$ mA.
4. Turn on RF power.

Turn-off Sequence:

1. Turn off RF power.
2. Turn off power supply $V_{PD} = +5$ V.
3. Turn off power supply $V_{CC} = +28$ V.

Notes:

1. I_{CQ} can be adjusted with the resistor R2 from the V_{PD} (+5V) supply and the PIN_VPD (pin14) of the amplifier. Increasing R2 results in a lower I_{CQ} . I_{CQ} should not be increased above 320 mA.
2. V_{PD} is used as a reference for the internal active bias circuitry. It can be used to turn on/off the amplifier. I_{PD} depends on the I_{CQ} quiescent current setting. I_{PD} can be up to 8mA at a quiescent current setting of 320mA.
3. I_{bias} will change based on RF input power level. It can be up to 8mA on the AP603.

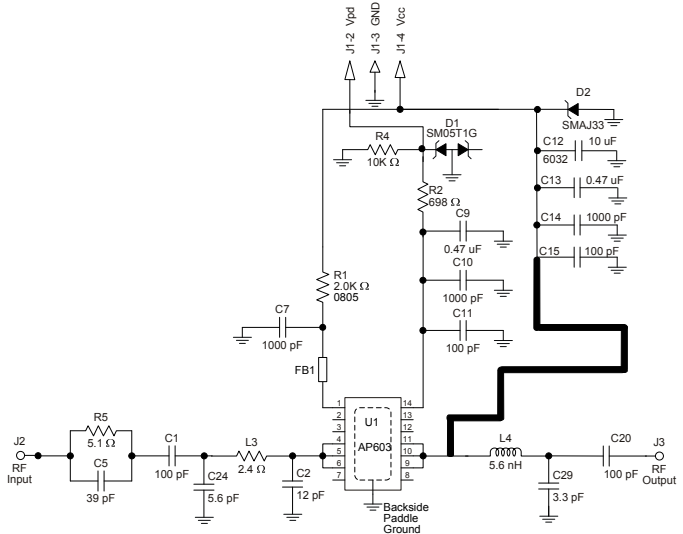
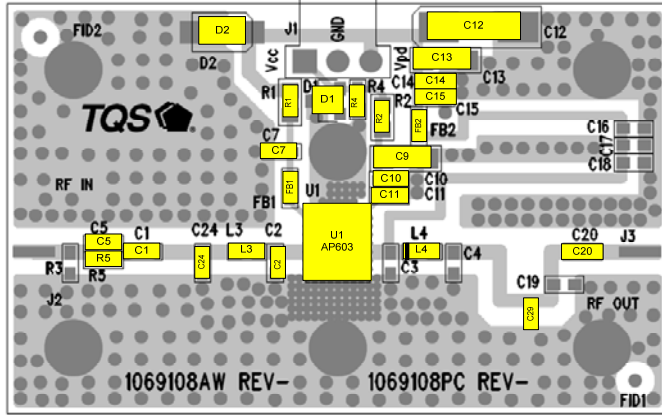


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High Dynamic Range 7W 28V HBT Amplifier



Application Circuit 920-960 MHz (AP603-PCB900)



Notes:

1. PC Board Material: 0.0147" Rogers Ultralam 2000, 1 oz Cu, $\epsilon_r = 2.45$, Microstrip line details: width = .042", spacing = .050"
2. The primary RF microstrip line is 50 Ω .
3. Do not exceed 5.5V on Vpd or damage to D1 will occur.
4. Do not exceed 33V on Vcc or damage to D2 will occur.
5. The center of L3 is placed at 210 mil from the AP603 (U1) device package.
6. The distance between edge of C2 and AP603 (U1) device package is 45 mil.
7. The distance between edge of C24 and AP603 (U1) device package is 294 mil.
8. The center of L4 is placed at 155 mil from AP603 (U1) device package.
9. The bold-faced RF trace is for the DC bias feed. The stub's length is approximately a $\frac{1}{4} \lambda$.
10. The main RF trace is cut at component L3 and L4 for this particular reference design.

Bill of Material

Ref Des	Value	Description	Manufacturer	Part Number
U1		28V Power Amplifier	TriQuint	AP603-F
C5	39 pF	Cap, Chip, 0603, 50V, 5%, NPO	various	
C1, C20, C11, C15	100 pF	Cap, Chip, 0603, 50V, 5%, NPO	various	
C7, C10, C14	1000 pF	Cap, Chip, 0603, 50V, 5%, NPO	various	
C9, C13	0.47 uF	Cap, Chip, 1206, 50V, 10%, X7R	various	
C12	10 uF	Cap, Tantalum, 6032, 35V, 10%	various	
R4	10 K Ω	Resistor, Chip, 0603, 5%, 1/16W	various	
R2	698 Ω	Resistor, Chip, 0603, 1%, 1/16W	various	
R1	2.0 K Ω	Resistor, Chip, 0805, 1%, 1/16W	various	
R5	5.1 Ω	Resistor, Chip, 0603, 5%, 50V	various	
FB2	0 Ω	Resistor, Chip, 0603, 5%, 50V	various	
L3	2.4 Ω	Resistor, Chip, 0603, 1%, 50V	various	
C2	12 pF	Cap, Chip, 0603, 50V, ± 0.1 pF	AVX	
C24	5.6 pF	Cap, Chip, 0603, 50V, ± 0.1 pF	AVX	06035J5R6BSTR
C29	3.3 pF	Cap, Chip, 0603, 50V, ± 0.1 pF	AVX	06035J3R3BSTR
L4	5.6 nH	Ind, Chip, 0603, ± 0.5 nH	Toko	LL1608-FSL5N6S
FB1		Filter EMI Ferrite Bead	various	
D1		TVS Diode Array, 5V, SOT23, 2Ch	On-Semiconductor	SM05T1G
D2		Diode TVS, 33V, 400W, 5% SMA	On-Semiconductor	1SMA33AT3G

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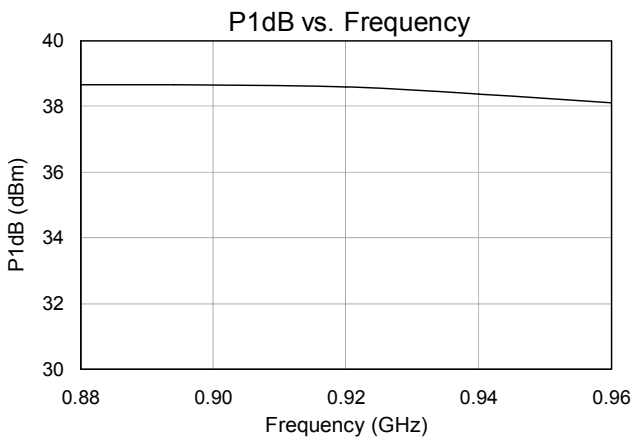
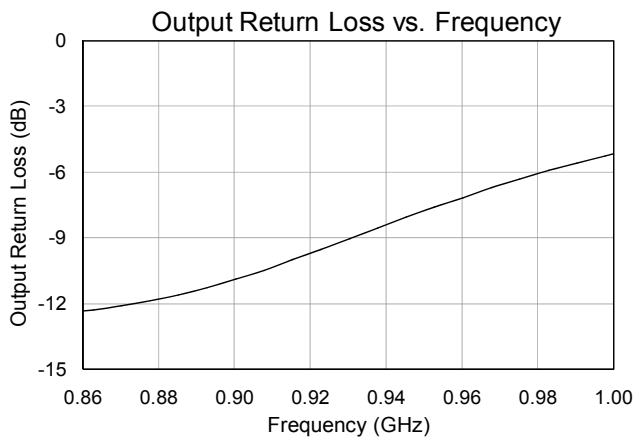
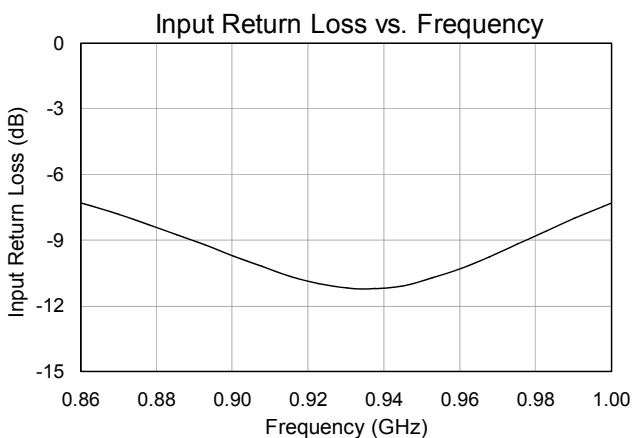
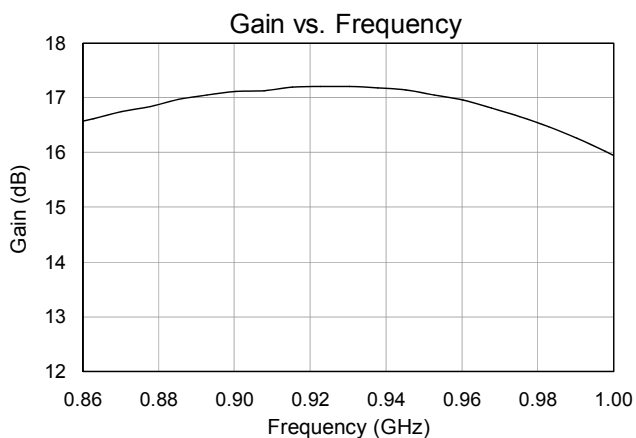


Typical Performance 920-960 MHz (AP603-PCB900)

Frequency	MHz	869	880	894	920	940	960
Gain [1]	dB	16.7	16.8	17	17	17	16.8
Input Return Loss	dB	8	8	9	11	11	10
Output Return Loss	dB	12	11	11	10	8.5	7
ACLR @ 28 dBm Output Power [3]	dBc	-52.5	-52.5	-53	-55.4	-55.5	-57.5
IMD3 @ 30 dBm PEP [2]	dBc					-52	
Collector Efficiency @ 30 dBm Output Power [3]	%	14.7	14.9	15.0	16.0	16.0	16.5
Output P1dB	dBm	+38.6	+38.6	+38.6	+38.6	+38.4	+38.1
Operating Current, Icc @ 30 dBm Output Power [3]	mA	240	238	228	225	223	217
Quiescent Current, Icq	mA	165					
Vpd	V	+5					
Vcc	V	+28					

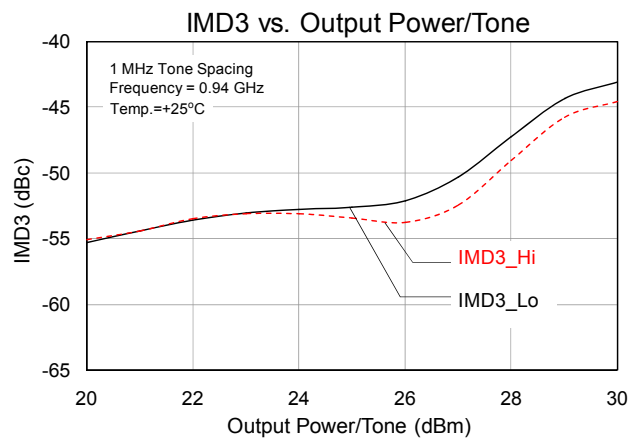
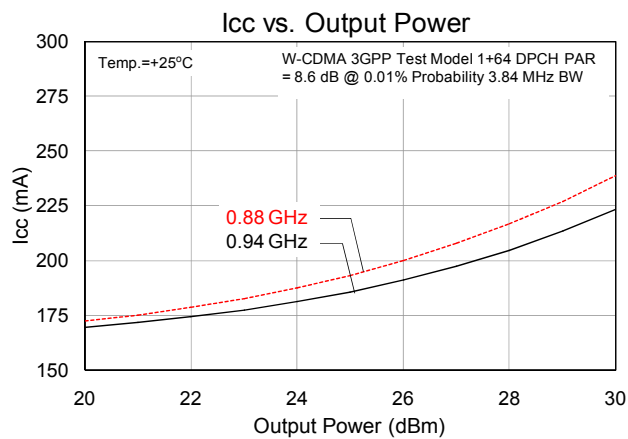
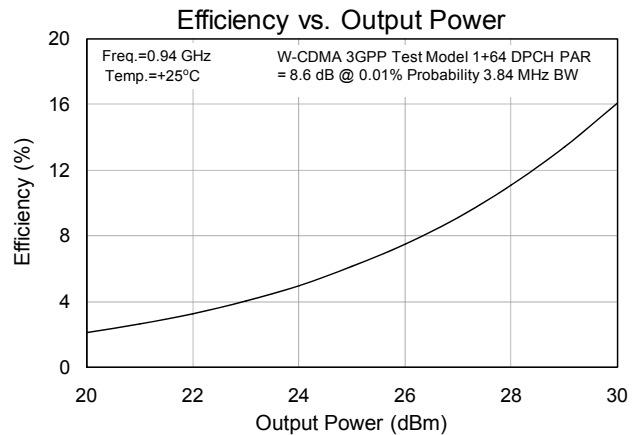
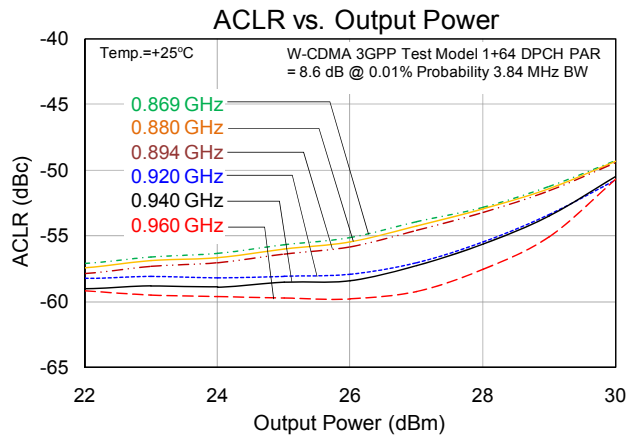
Notes

1. Test conditions unless otherwise noted: 25 °C, +5V, in tuned application circuit.
2. IMD3 is measured with 1 MHz tone spacing.
3. ACLR test set-up: 3GPP WCDMA, TM1+64DPCH, +5MHz Offset, PAR = 8.6 dB @ 0.01% Probability.



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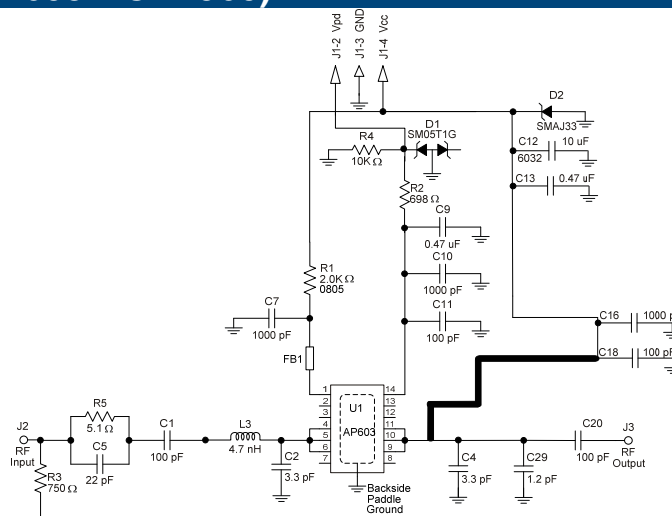
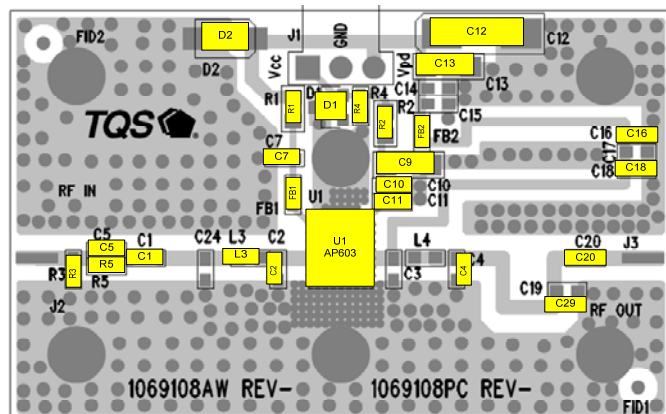
High Dynamic Range 7W 28V HBT Amplifier



High Dynamic Range 7W 28V HBT Amplifier



Application Circuit 1930-1990 MHz (AP603-PCB1960)



Notes:

1. PC Board Material: 0.0147" Rogers Ultralam 2000, 1 oz Cu, $\epsilon_r = 2.45$, Microstrip line details: width = .042", spacing = .050"
2. The primary RF microstrip line is 50 Ω .
3. Do not exceed 5.5V on Vpd or damage to D1 will occur.
4. Do not exceed 33V on Vcc or damage to D2 will occur.
5. The center of L3 is placed at 175 mil from the AP603 (U1) device package.
6. The distance between edge of C2 and AP603 (U1) device package is 110 mil.
7. The distance between edge of C4 and AP603 (U1) device package is 240 mil.
8. The bold-faced RF trace is for the DC bias feed. The stub's length is approximately a $\frac{1}{4} \lambda$.
9. The main RF trace is cut at component L3 for this particular reference design.

Bill of Material

Ref Des	Value	Description	Manufacturer	Part Number
U1		28V Power Amplifier	TriQuint	AP603-F
C5	22 pF	Cap, Chip, 0603, 50 V, 5%, NPO	various	
C1, C20, C11, C18	100 pF	Cap, Chip, 0603, 50 V, 5%, NPO	various	
C7, C10, C16	1000 pF	Cap, Chip, 0603, 50 V, 5%, NPO	various	
C9, C13	0.47 uF	Cap, Chip, 1206, 50 V, 10%, X7R	various	
C12	10 uF	Cap, Tantalum, 6032, 35 V, 10%	various	
R4	10 KΩ	Resistor, Chip, 0603, 5%, 1/16 W	various	
R2	698 Ω	Resistor, Chip, 0603, 1%, 1/16 W	various	
R1	2.0 KΩ	Resistor, Chip, 0805, 1%, 1/16 W	various	
R5	5.1 Ω	Resistor, Chip, 0603, 5%, 50 V	various	
R3	750 Ω	Resistor, Chip, 0603, 5%, 50 V	various	
FB2	0 Ω	Resistor, Chip, 0603, 5%, 50V	various	
C2, C4	3.3 pF	Cap, Chip, 0603, 50 V,± 0.1 pF	AVX	06035J3R3BSTR
C29	1.2 pF	Cap, Chip, 0603, 50 V, +/-0.05 pF	AVX	06035J1R2BSTR
L3	4.7 nH	Ind, Chip, 0603, +/-0.5 nH	Toko	LL1608-FSL4N7S
FB1		Filter EMI Ferrite Bead	various	
D1		TVS Diode Array, 5V, SOT23, 2Ch	On-Semiconductor	SM05T1G
D2		Diode TVS, 33V, 400W, 5% SMA	On-Semiconductor	1SMA33AT3G

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High Dynamic Range 7W 28V HBT Amplifier

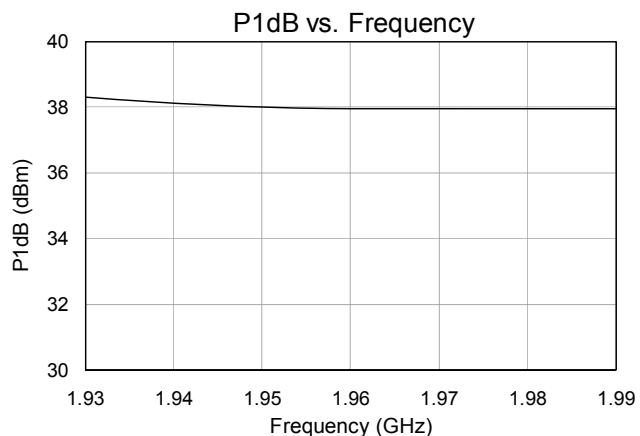
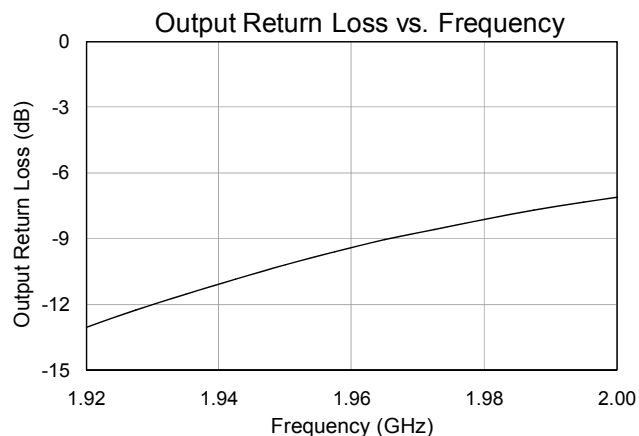
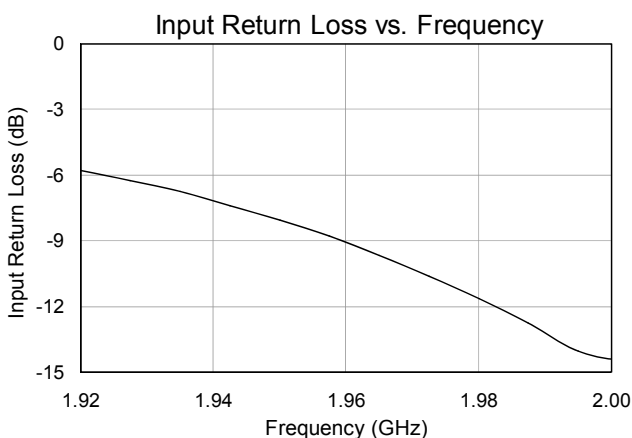
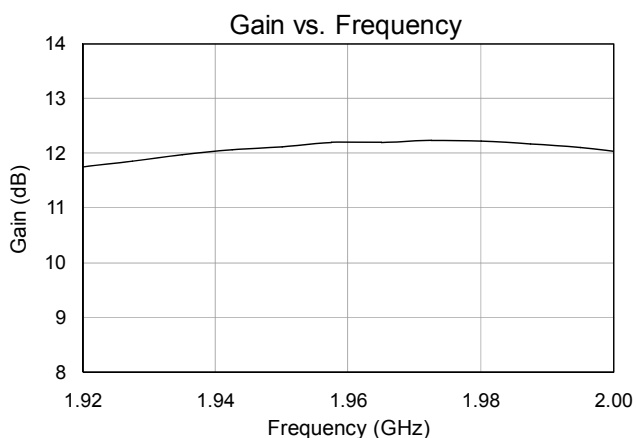


Typical Performance 1930-1990 MHz (AP603-PCB1960)

Frequency	MHz	1930	1960	1990
Gain [1]	dB	11.9	12	12
Input Return Loss	dB	6.5	9	12
Output Return Loss	dB	12	9.5	7.5
ACLR @ 28 dBm Output Power [3]	dBc	-50	-51	-51
IMD3 @ 30 dBm PEP [2]	dBc		-49.5	
Collector Efficiency @ 30 dBm Output Power [3]	%	15.4	14.7	14.2
Output P1dB	dBm	+38.3	+38.0	+37.3
Operating Current, Icc @ 30 dBm Output Power [3]	mA	228	240	251
Quiescent Current, Icq	mA	165		
Vpd	V	+5		
Vcc	V	+28		

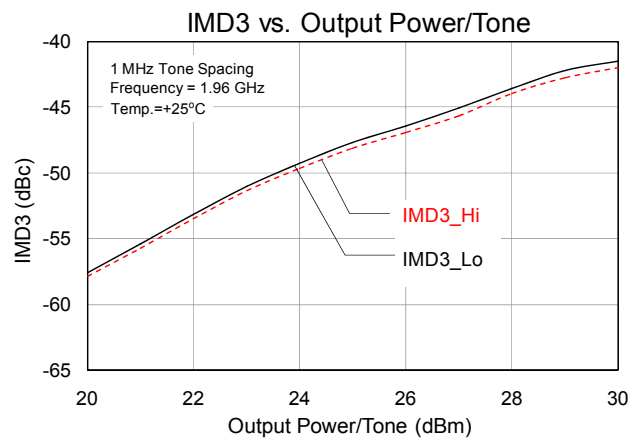
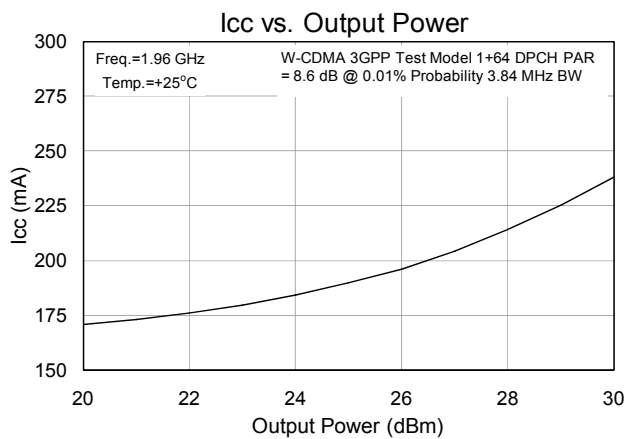
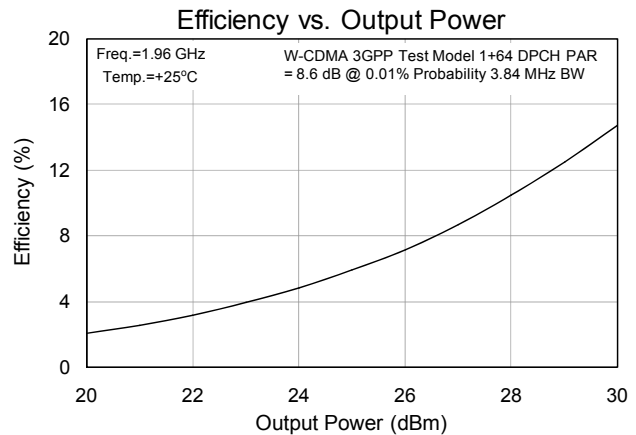
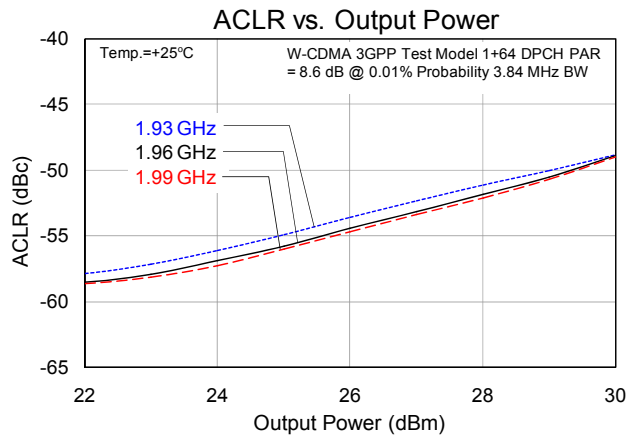
Notes

1. Test conditions unless otherwise noted: 25 °C, +5V, in tuned application circuit.
2. IMD3 is measured with 1 MHz tone spacing.
3. ACLR test set-up: 3GPP WCDMA, TM1+64DPCH, +5MHz Offset, PAR = 8.6 dB @ 0.01% Probability.



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High Dynamic Range 7W 28V HBT Amplifier

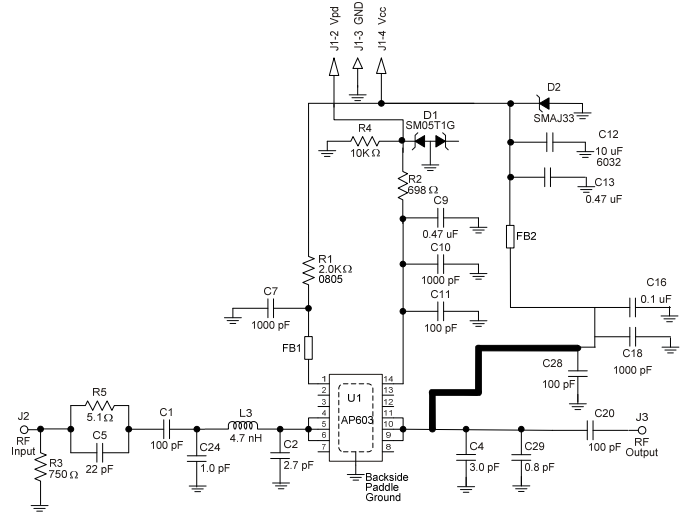
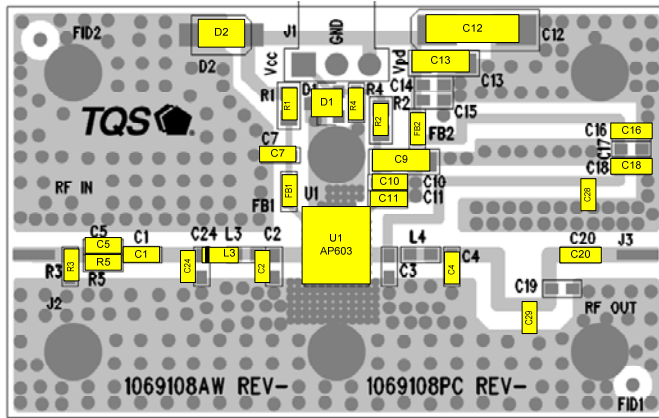


AP603

High Dynamic Range 7W 28V HBT Amplifier



Application Circuit 2110-2170 MHz (AP603-PCB2140)



Notes:

1. PCB Board Material: 0.0147" Rogers Ultralam 2000, 1 oz Cu, $\epsilon_r = 2.45$, Microstrip line details: width = .042", spacing = .050"
2. The primary RF microstrip line is 50 Ω .
3. Do not exceed +5.5V on Vpd or TVS diode D1 will be damaged.
4. Do not exceed +33V on Vcc or TVS diode D2 will be damaged.
5. Components shown on the silkscreen but not on the schematic are not used.
6. The center of L3 is placed at 247 mil from the AP603 (U1) device package.
7. The distance between edge of C2 and AP603 (U1) device package is 141 mil.
8. The distance between edge of C24 and AP603 (U1) device package is 276 mil.
9. The distance between the edge of C4 and AP603 (U1) device package is 210 mil.
10. The bold-faced RF trace is for the DC bias feed. The stub's length is approximately a $\frac{1}{4}\lambda$.
11. The main RF trace is cut at component L3 and L4 for this particular reference design.

Bill of Material

Ref Des	Value	Description	Manufacturer	Part Number
U1		28V Power Amplifier	TriQuint	AP603-F
L3	4.7 nH	Ind, Chip, 0603, +/-0.3 nH	various	
R1	2.0 K Ω	Resistor, Chip, 0805, 1%, 1/10W	various	
R2	698 Ω	Resistor, Chip, 0603, 1%, 1/10W	various	
R5	5.1 Ω	Resistor, Chip, 0603, 5%, 1/16W	various	
R3	750 Ω	Resistor, Chip, 0603, 5%, 1/16W	various	
R4	10 K Ω	Resistor, Chip, 0603, 5%, 1/16W	various	
FB2	0 Ω	Resistor, Chip, 0603, 5%, 1/16W	various	
C2	2.7 pF	CAP, 0603, +/- 0.05 pF, 50V. ACCU-P	AVX	06035J2R7ABSTR
C4	3.0 pF	CAP, 0603, +/- 0.05 pF, 50V. ACCU-P	AVX	06035J3R0ABSTR
C29	0.8 pF	CAP, 0603, +/- 0.05pF, 50V. ACCU-P	AVX	06035J0R8ABSTR
C7, C10, C18	1000 pF	CAP, 0603, 5%, 50V, NPO/COG	various	
C16	0.1 uF	CAP, 0603, 10%, 50V, X7R	various	
C9, C13	0.47 uF	CAP, 1206, 10%, 50V, X7R	various	
C20, C28, C11	100 pF	CAP, 0603, 5%, 50V, NPO/COG	various	
C12	10.0 uF	CAP, 6032, 10%, 35V, TANT	various	
C24	1.0 pF	CAP, 0603, +/- 0.05 pF, 50V. ACCU-P	AVX	06035J1R0ABSTR
C1, C5	22 pF	CAP, 0603, 5%, NPO/COG	various	
D1		TVS Diode Array, 5V, SOT23, 2Ch	On-Semiconductor	SM05T1G
D2		Diode TVS, 33V, 400W, 5% SMA	On-Semiconductor	1SMA33AT3G
FB1		Filter EMI Ferrite Bead	various	

AP603

High Dynamic Range 7W 28V HBT Amplifier

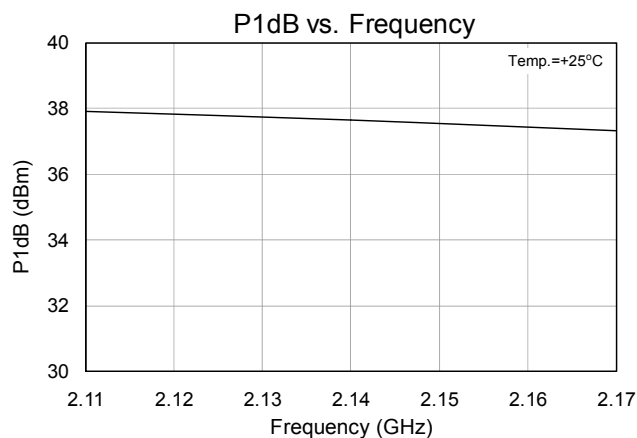
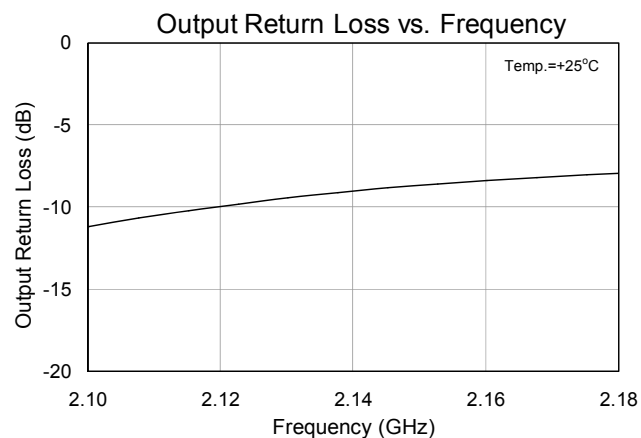
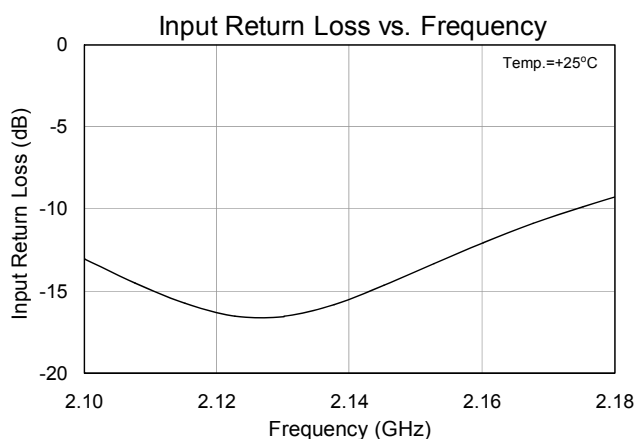
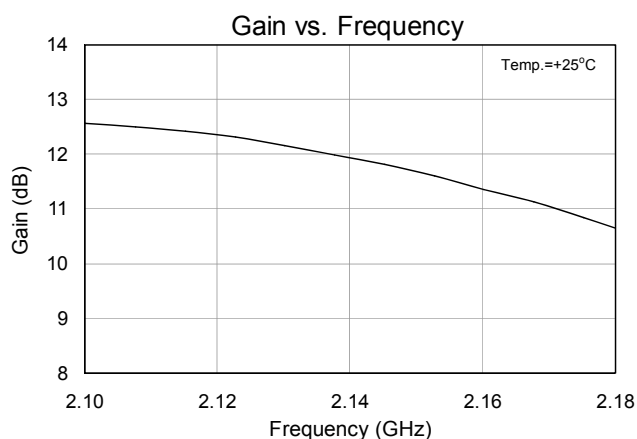


Typical Performance 2110-2170 MHz (AP603-PCB2140)

Frequency	MHz	2110	2140	2170
Gain [1]	dB	12	11.9	11
Input Return Loss	dB	14	15	10
Output Return Loss	dB	10	9.5	8.5
ACLR @ 28 dBm Output Power [3]	dBc	-49	-50	-51
IMD3 @ 30 dBm PEP [2]	dBc	-47	-50	-51
Collector Efficiency @ 30 dBm Output Power [3]	%	15.7	14.6	14.6
Output P1dB	dBm	+37.9	+37.6	+37.3
Operating Current, Icc @ 30 dBm Output Power [3]	mA	225	232	245
Quiescent Current, Icq	mA	165		
Vpd	V	+5		
Vcc	V	+28		

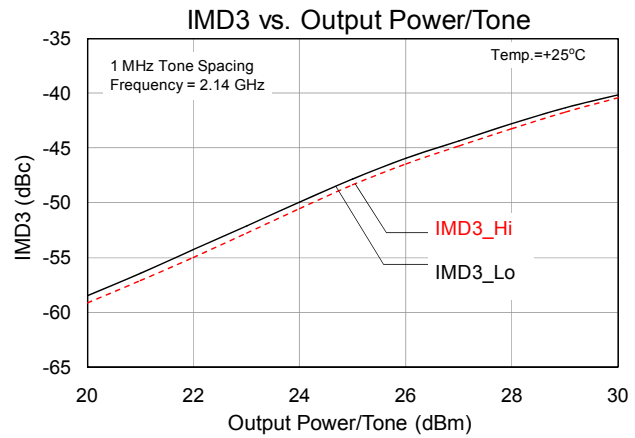
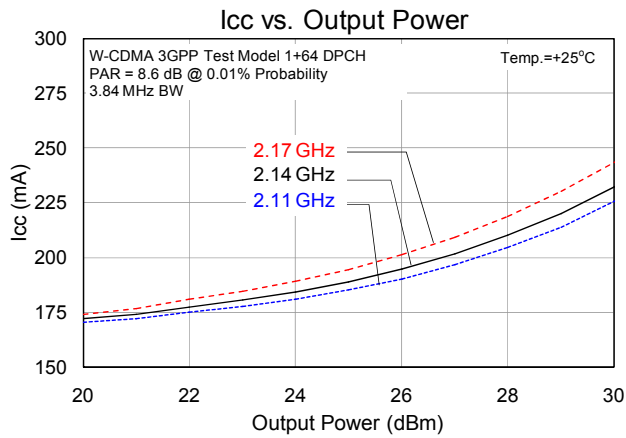
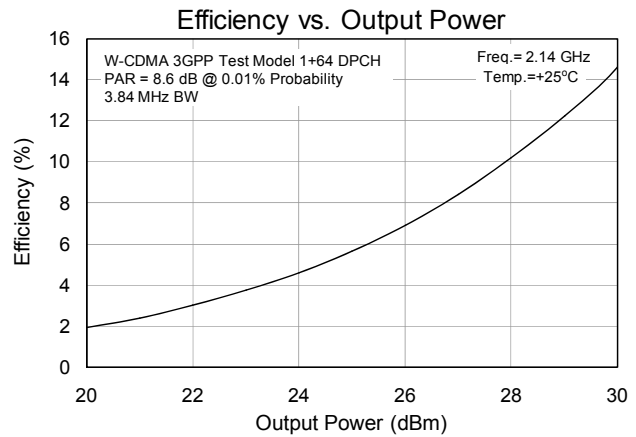
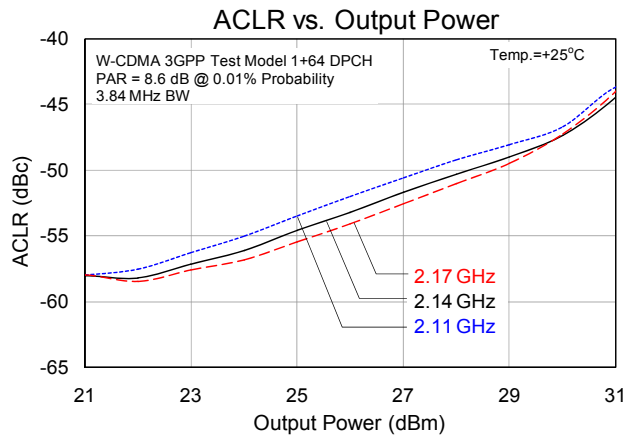
Notes

1. Test conditions unless otherwise noted: 25 °C, +5V, in tuned application circuit.
2. IMD3 is measured with 1 MHz tone spacing.
3. ACLR test set-up: 3GPP WCDMA, TM1+64DPCH, +5MHz Offset, PAR = 8.6 dB @ 0.01% Probability.



AP603

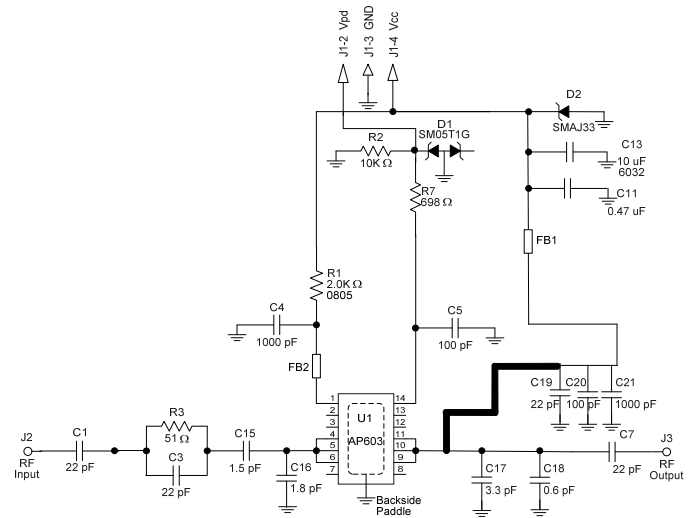
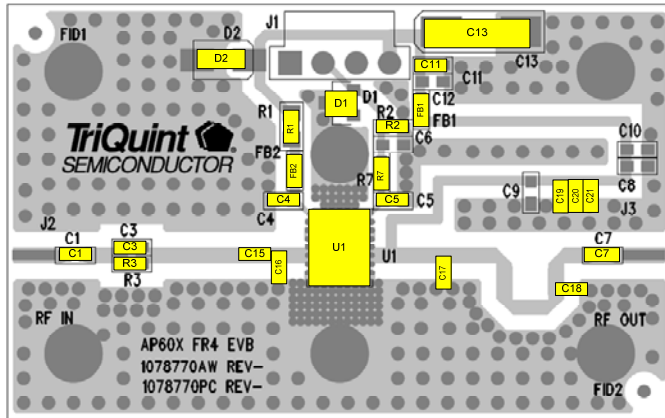
High Dynamic Range 7W 28V HBT Amplifier



High Dynamic Range 7W 28V HBT Amplifier



Reference Design 2110-2170 MHz (using FR4 PCB)



Notes:

1. PC Board Material: 0.021" Nelco N4000-13, single layer, 1 oz Cu, $\epsilon_r = 3.7$, Microstrip line details: width = .042", spacing = .050".
2. The primary RF microstrip line is 50 Ω .
3. Do not exceed +5.5V on Vpd or TVS diode D1 will be damaged.
4. Do not exceed +33V on Vcc or TVS diode D2 will be damaged.
5. Components shown on the silkscreen but not on the schematic are not used.
6. The center of C15 is placed at 150 mil from the AP603 (U1) device package.
7. The distance between edge of C16 and AP603 (U1) device package is 84 mil.
8. The distance between edge of C17 and AP603 (U1) device package is 190 mil.
9. The bold-faced RF trace is for the DC bias feed. The stub's length is approximately a $\frac{1}{4} \lambda$.
10. The main RF trace is cut at component C15 for this particular reference design.

Bill of Material

Ref Des	Value	Description	Manufacturer	Part Number
U1		28V Power Amplifier	TriQuint	AP603-F
C1, C3, C7, C19	22 pF	Cap, Chip, 0603, 50V, 5%, NPO	various	
C5, C20	100 pF	Cap, Chip, 0603, 50V, 5%, NPO	various	
C4, C21	1000 pF	Cap, Chip, 0603, 50V, 5%, NPO	various	
C11	0.47 uF	Cap, Chip, 1206, 50V, 10%, X7R	various	
C13	10 uF	Cap, Tantalum, 6032, 35V, 10%	various	
R2	10 KΩ	Resistor, Chip, 0603, 5%, 1/16W	various	
R7	698 Ω	Resistor, Chip, 0603, 1%, 1/10W	various	
R1	2.0 KΩ	Resistor, Chip, 0805, 1%, 1/10W	various	
R3	51 Ω	Resistor, Chip, 0603, 5%, 50V	various	
C15	1.5 pF	Cap, Chip, 0603, 50V, ± 0.05pF	AVX	06035J1R5BSTR
C16	1.8 pF	Cap, Chip, 0603, 50V, ± 0.05pF	AVX	06035J1R8BSTR
C17	3.3 pF	Cap, Chip, 0603, 50V, ± 0.05pF	AVX	06035J3R3BSTR
C18	0.6 pF	Cap, Chip, 0603, 50V, ± 0.05pF	AVX	06035J0R6BSTR
FB1, FB2	0 Ω	Resistor, Chip, 0603, 5%, 50V, 1/16W	various	
D1		TVS Diode Array, 5V, SOT23, 2Ch	various	SM05T1G
D2		Diode TVS, 33V, 400W, 5% SMA	various	1SMA33AT3G

AP603

High Dynamic Range 7W 28V HBT Amplifier

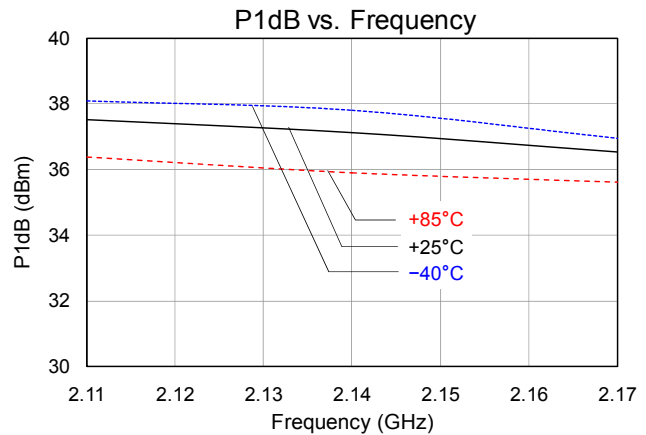
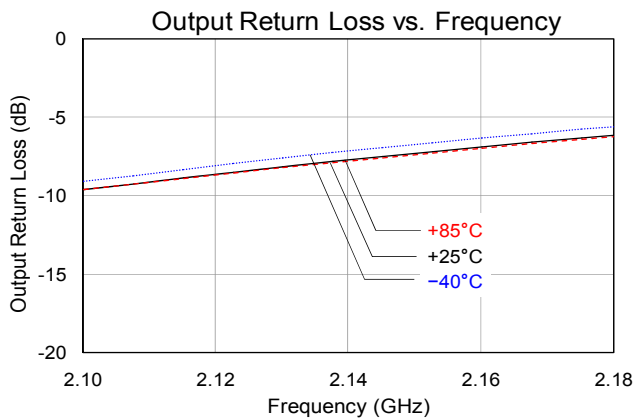
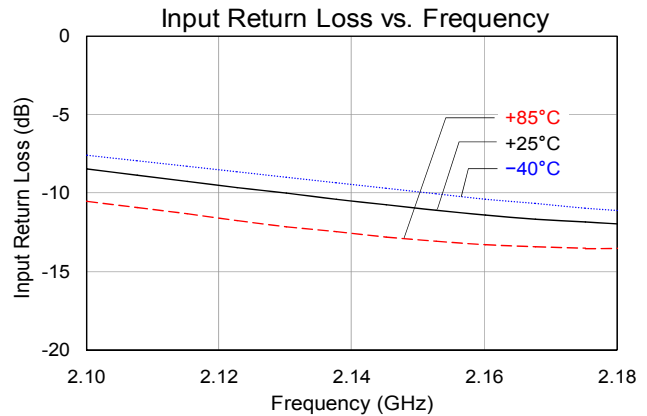
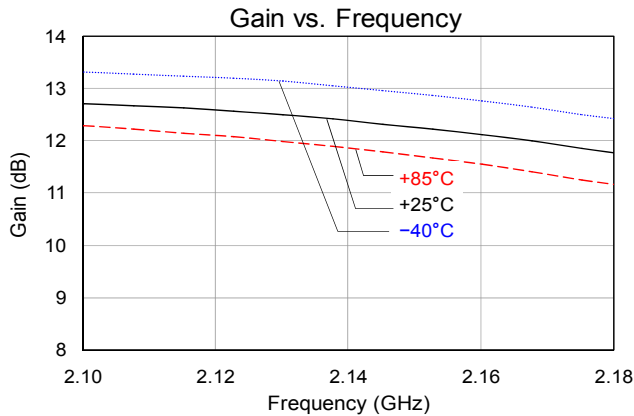


Typical Performance 2110-2170 MHz (using FR4 PCB)

Frequency	MHz	2110	2140	2170
Gain [1]	dB	12.4	12.2	11.8
Input Return Loss	dB	9	10	11
Output Return Loss	dB	9	8	7
ACLR @ 28dBm Output Power [3]	dBc	-50	-51	-50
IMD3 @ 30 dBm PEP [2]	dBc	-50.5	-52.5	-51.5
Collector Efficiency @ 30 dBm Output Power [3]	%	14.8	14.2	13.3
Output P1dB	dBm	+37.5	+37.1	+36.5
Operating Current, Icc @ 30 dBm Output Power	mA	240	250	267
Quiescent Current, Icq	mA	165		
Vpd	V	+5		
Vcc	V	+28		

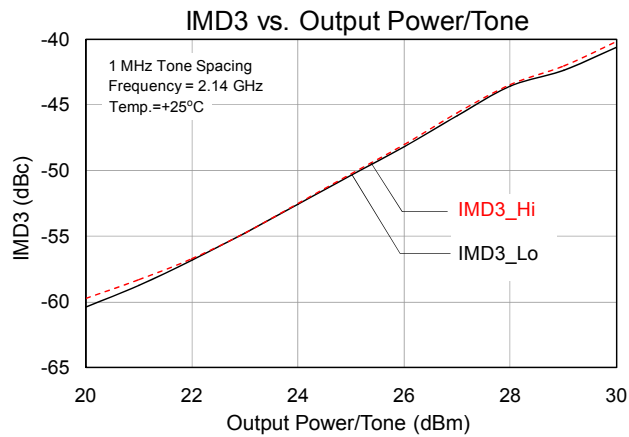
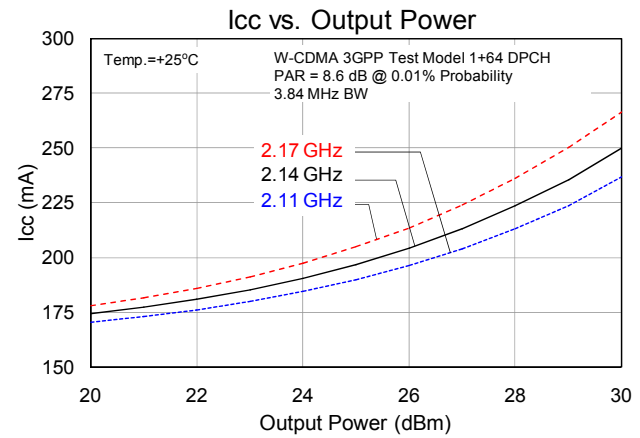
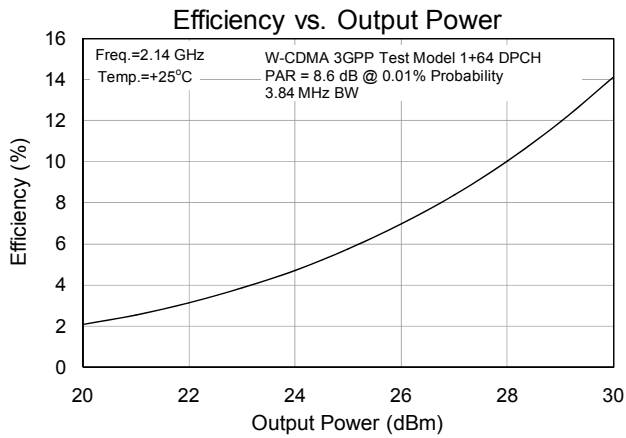
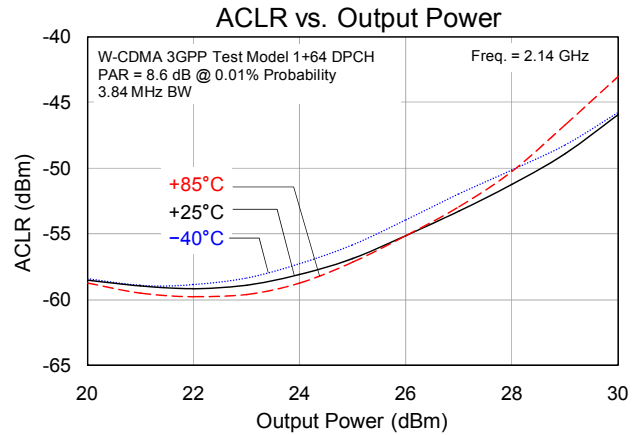
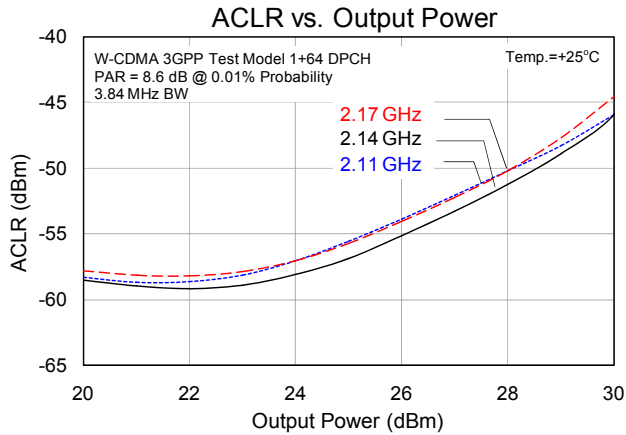
Notes

1. Test conditions unless otherwise noted: 25 °C, Vcc = +28V, Vpd = +5V, in tuned application circuit.
2. IMD3 is measured with 1 MHz spacing.
3. ACLR test set-up: 3GPP WCDMA, TM1+64DPCH, +5MHz Offset, PAR = 8.6 dB @ 0.01% Probability.

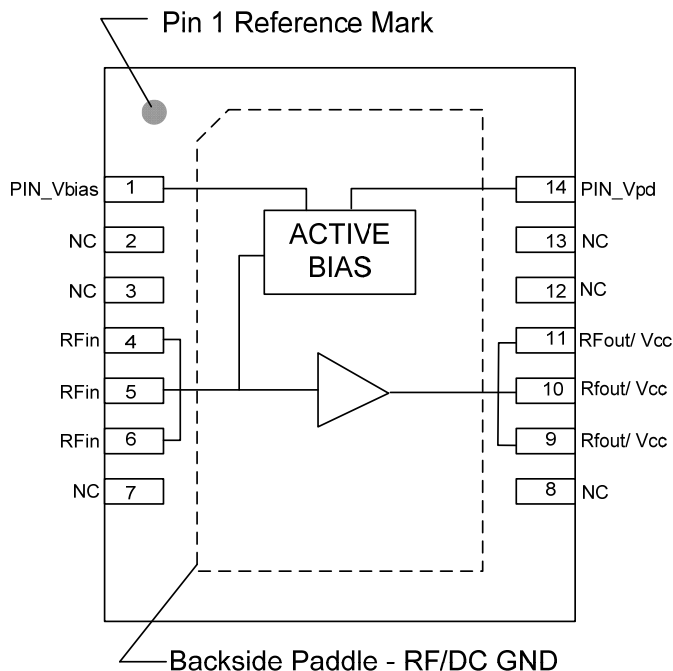


AP603

High Dynamic Range 7W 28V HBT Amplifier



Pin Description



Pin	Symbol	Description
1	PIN_Vbias	Voltage supply for active bias for the amp. Connect to same supply voltage as Vcc.
2, 3, 7, 8, 12, 13	N/C	No internal connection. This pin can be grounded or N/C on PCB. Land pads should be provided for PCB mounting integrity.
4, 5, 6	RF IN	RF Input. DC Voltage present, blocking cap required. Requires matching for operation.
9, 10, 11	RF Output / Vcc	RF Output. DC Voltage present, blocking cap required
14	PIN_VPD	Reference current into internal active bias current mirror. Current into PIN_VPD sets device quiescent current. Also, can be used as on/off control.
Backside paddle	RF/DC GND	Multiple Vias should be employed to minimize inductance and thermal resistance. Use recommended via pattern shown under mounting configuration and ensure good solder attach for optimum thermal and electrical performance

AP603

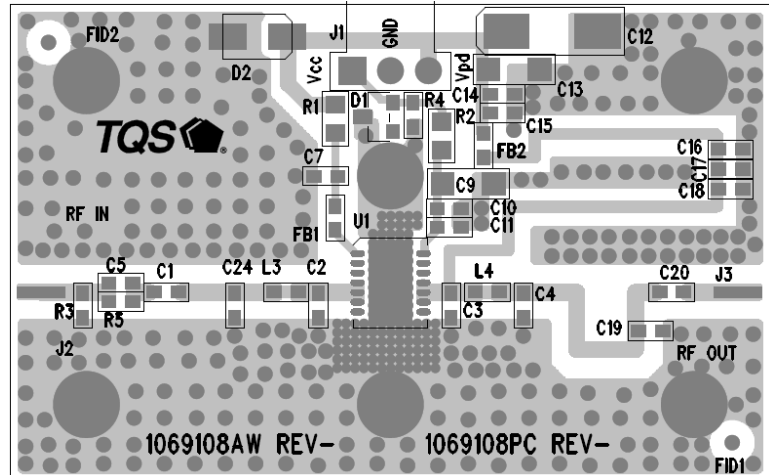
High Dynamic Range 7W 28V HBT Amplifier



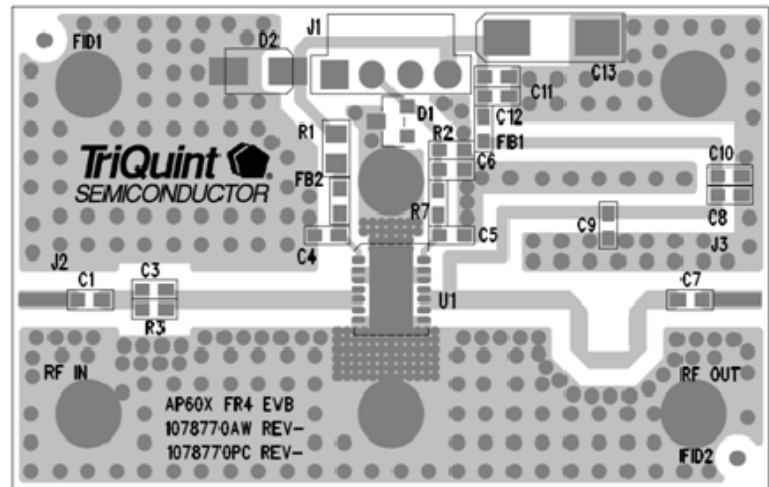
Applications Information

PC Board Layout

PCB Material: 0.0147" Rogers Ultralam 2000, single layer, 1 oz Cu, $\epsilon_r = 2.45$, Microstrip line details: width = .042", spacing = .050"



PCB Material: 0.021" Nelco N4000-13, single layer, 1 oz Cu, $\epsilon_r = 3.7$, Microstrip line details: width = .042", spacing = .050"

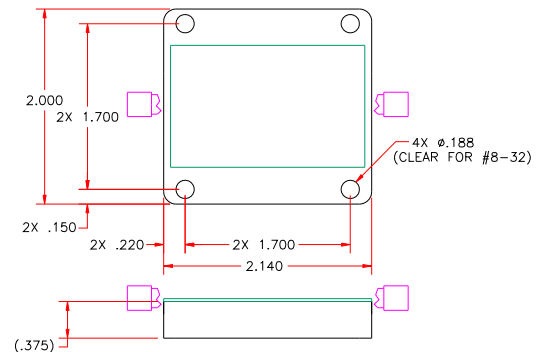


The pad pattern shown has been developed and tested for optimized assembly at TriQuint Semiconductor. The PCB land pattern has been developed to accommodate lead and package tolerances. Since surface mount processes vary from company to company, careful process development is recommended.

Baseplate Configuration

Notes:

1. Please note that for reliable operation, the evaluation board will have to be mounted to a much larger heat sink during operation and in laboratory environments to dissipate the power consumed by the device. The use of a convection fan is also recommended in laboratory environments.
2. The area around the module underneath the PCB should not contain any soldermask in order to maintain good RF grounding.
3. For proper and safe operation in the laboratory, the power-on sequencing is recommended.

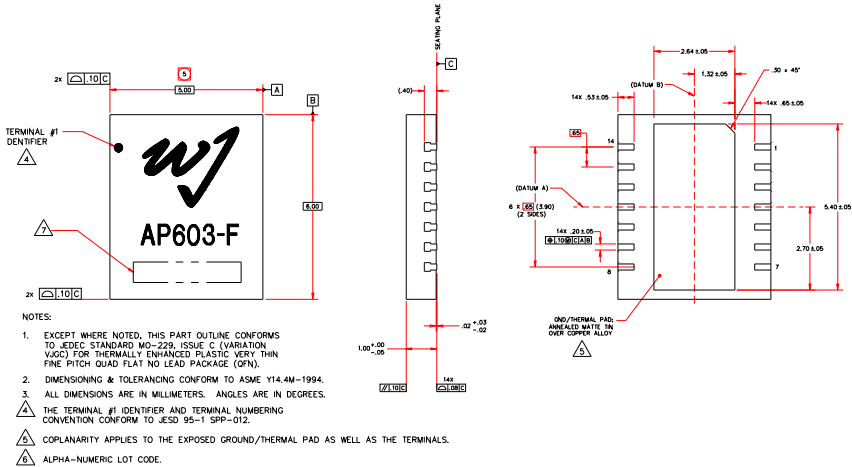


Mechanical Information

Package Information and Dimensions

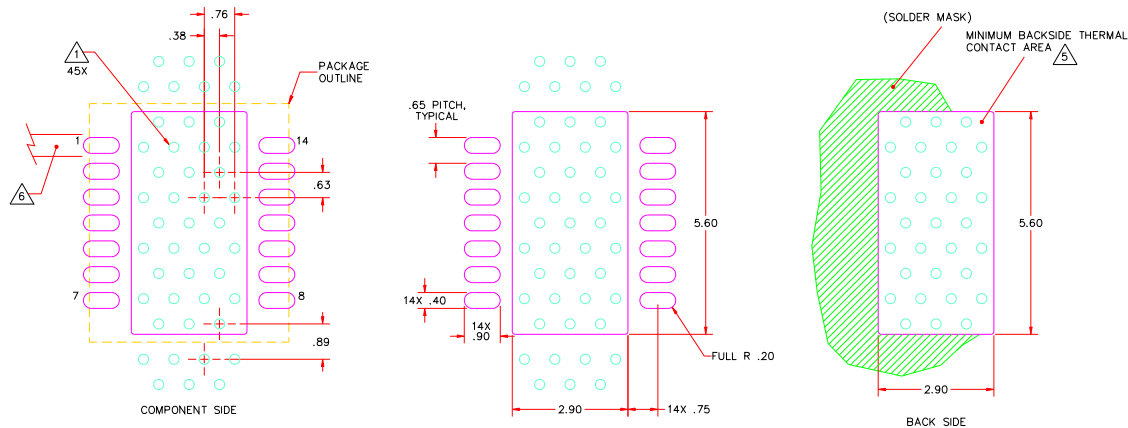
This package is lead-free and RoHS-compliant. It is compatible with both lead-free (maximum 260 °C reflow temperature) and leaded (maximum 245 °C reflow temperature) soldering processes. The plating material on the pins is annealed matte tin over copper.

The component will be laser marked with an “AP603-F” product identifier with an alphanumeric lot code on the top surface of the package.



Mounting Configuration

All dimensions are in millimeters (inches). Angles are in degrees.



Notes:

- Ground/Thermal vias are critical for the proper performance of this device. Vias should use a .35mm (#80/.0135") diameter and have a final, plated thru diameter of .25mm (.010").
- Add as much copper as possible to inner and outer layers near the part to ensure optimal performance.
- To ensure reliable operation, device ground paddle-to-ground pad solder joint is critical.
- Add mounting screws near the part to fasten the board to a heatsink. Ensure that the ground/thermal via region contacts the heatsink.
- Do not put solder mask on the back side of the PC Board in the region where the board contacts the heatsink.
- RF trace width depends upon the width of the PC board material and construction.
- Use 1 oz. copper minimum
- A heatsink underneath the area of the PCB for the mounted device is strictly required for proper thermal operation. Damage to the device can occur without one

Product Compliance Information

ESD Information



Caution! ESD-Sensitive Device

ESD Rating: Class 1A
Value: Passes > 250 V to < 500 V.
Test: Human Body Model (HBM)
Standard: JEDEC Standard JESD22-A114

ESD Rating: Class IV
Value: Passes ≥ 1000 V to <2000 V.
Test: Charged Device Model (CDM)
Standard: JEDEC Standard JESD22-C101

MSL Rating

Level 3 at +260 °C convection reflow

The part is rated Moisture Sensitivity Level 3 at 260°C per JEDEC standard IPC/JEDEC J-STD-020.

Solderability

Compatible with the latest version of J-STD-020,
Lead free solder, 260°

This part is compliant with EU 2002/95/EC RoHS directive (Restrictions on the Use of Certain Hazardous Substances in Electrical and Electronic Equipment).

This product also has the following attributes:

- Lead Free
- Halogen Free (Chlorine, Bromine)
- Antimony Free
- TBBP-A ($C_{15}H_{12}Br_4O_2$) Free
- PFOS Free
- SVHC Free

Contact Information

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Fax: +1.503.615.8902

For technical questions and application information:

Email: sjcpplcations.engineering@tqs.com

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