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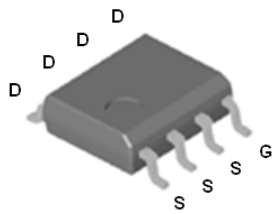
RoHS Compliant

# P06P03LVG

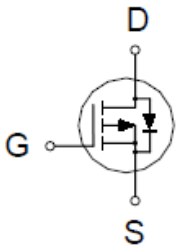
## P-Channel Logic Level Enhancement Mode MOSFET

### PRODUCT SUMMARY

| $V_{(BR)DSS}$ | $R_{DS(ON)}$ | $I_D$ |
|---|---|---|
| -30V | 45mΩ @$V_{GS}$ = -10V | -6A |




**SOP- 08**




### ABSOLUTE MAXIMUM RATINGS ($T_A$ = 25 °C Unless Otherwise Noted)

| PARAMETERS/TEST CONDITIONS | | SYMBOL | LIMITS | UNITS |
|---|---|---|---|---|
| Drain-Source Voltage | | $V_{DS}$ | -30 | V |
| Gate-Source Voltage | | $V_{GS}$ | ±20 | |
| Continuous Drain Current | $T_A$ = 25 °C | $I_D$ | -6 | A |
| | $T_A$ = 70 °C | | -5 | |
| Pulsed Drain Current[1] | | $I_{DM}$ | -30 | |
| Power Dissipation | $T_A$ = 25 °C | $P_D$ | 2.5 | W |
| | $T_A$ = 70 °C | | 1.6 | |
| Operating Junction & Storage Temperature Range | | $T_J$, $T_{STG}$ | -55 to 150 | °C |

### THERMAL RESISTANCE RATINGS

| THERMAL RESISTANCE | SYMBOL | TYPICAL | MAXIMUM | UNITS |
|---|---|---|---|---|
| Junction-to-Case | $R_{\theta JC}$ | | 25 | °C / W |
| Junction-to-Ambient | $R_{\theta JA}$ | | 50 | |

[1]Pulse width limited by maximum junction temperature.

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### ELECTRICAL CHARACTERISTICS ($T_A$ = 25 °C, Unless Otherwise Noted)

| PARAMETER | SYMBOL | TEST CONDITIONS | LIMITS | | | UNIT |
|---|---|---|---|---|---|---|
| | | | MIN | TYP | MAX | |
| **STATIC** | | | | | | |
| Drain-Source Breakdown Voltage | $V_{(BR)DSS}$ | $V_{GS}$ = 0V, $I_D$ = -250μA | -30 | | | V |
| Gate Threshold Voltage | $V_{GS(th)}$ | $V_{DS}$ = $V_{GS}$, $I_D$ = -250μA | -0.9 | -1.5 | -3.0 | |
| Gate-Body Leakage | $I_{GSS}$ | $V_{DS}$ = 0V, $V_{GS}$ = ±20V | | | ±100 | nA |
| Zero Gate Voltage Drain Current | $I_{DSS}$ | $V_{DS}$ = -24V, $V_{GS}$ = 0V | | | 1 | μA |
| | | $V_{DS}$ = -20V, $V_{GS}$ = 0V , $T_J$ = 125 °C | | | 10 | |
| On-State Drain Current[1] | $I_{D(ON)}$ | $V_{DS}$ = -5V, $V_{GS}$ = -10V | -30 | | | A |
| Drain-Source On-State Resistance[1] | $R_{DS(ON)}$ | $V_{GS}$ = -4.5V, $I_D$ = -5A | | 60 | 75 | mΩ |
| | | $V_{GS}$ = -10V, $I_D$ = -6A | | 37 | 45 | |
| Forward Transconductance[1] | $g_{fs}$ | $V_{DS}$ = -10V, $I_D$ = -6A | | 16 | | S |
| **DYNAMIC** | | | | | | |
| Input Capacitance | $C_{iss}$ | $V_{GS}$ = 0V, $V_{DS}$ = -15V, f = 1MHz | | 530 | | pF |
| Output Capacitance | $C_{oss}$ | | | 135 | | |
| Reverse Transfer Capacitance | $C_{rss}$ | | | 70 | | |
| Total Gate Charge[2] | $Q_g$ | $V_{DS}$ = 0.5$V_{(BR)DSS}$, $V_{GS}$ = -10V, $I_D$ = -6A | | 10 | 14 | nC |
| Gate-Source Charge[2] | $Q_{gs}$ | | | 2.2 | | |
| Gate-Drain Charge[2] | $Q_{gd}$ | | | 2 | | |
| Turn-On Delay Time[2] | $t_{d(on)}$ | $V_{DS}$ = -15V, $R_L$= 1Ω $I_D$≅ -1A, $V_{GS}$ = -10V, $R_{GS}$ = 6Ω | | 5.7 | | nS |
| Rise Time[2] | $t_r$ | | | 10 | | |
| Turn-Off Delay Time[2] | $t_{d(off)}$ | | | 18 | | |
| Fall Time[2] | $t_f$ | | | 5 | | |
| **SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS ($T_A$ = 25 °C)** | | | | | | |
| Continuous Current | $I_S$ | | | | -2.1 | A |
| Forward Voltage[1] | $V_{SD}$ | $I_F$ = -6A, $V_{GS}$ = 0V | | | -1.2 | V |
| Reverse Recovery Time | $t_{rr}$ | $I_F$ = -5A, dIF/dt = 100A / μS | | 15.5 | | nS |
| Reverse Recovery Charge | $Q_{rr}$ | | | 7.9 | | nC |

[1]Pulse test : Pulse Width ≤ 300 μsec, Duty Cycle ≤ 2%.

[2]Independent of operating temperature.

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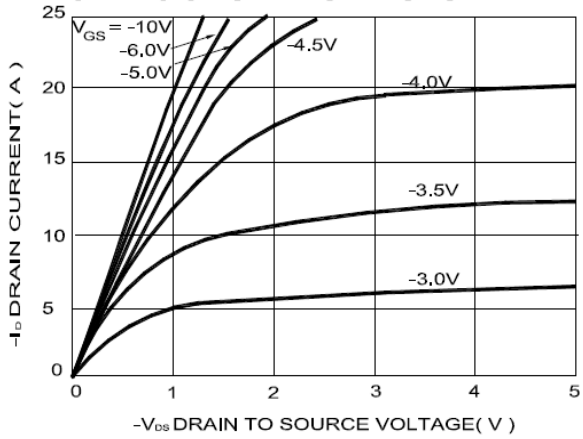
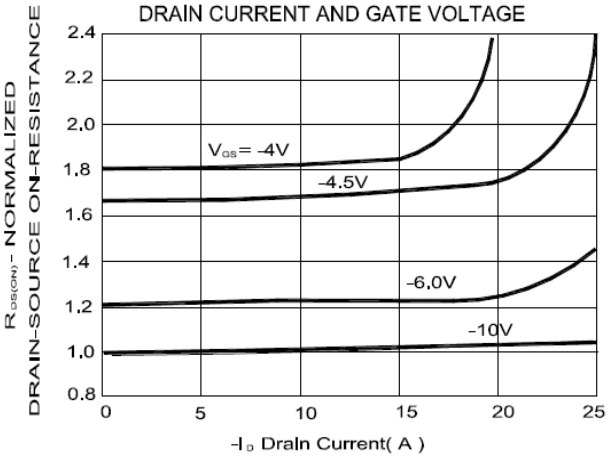
## Typical Characteristics

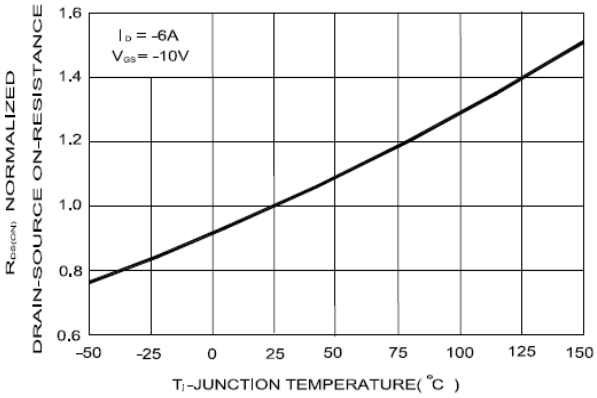
ON-REGION CHARACTERISTICE



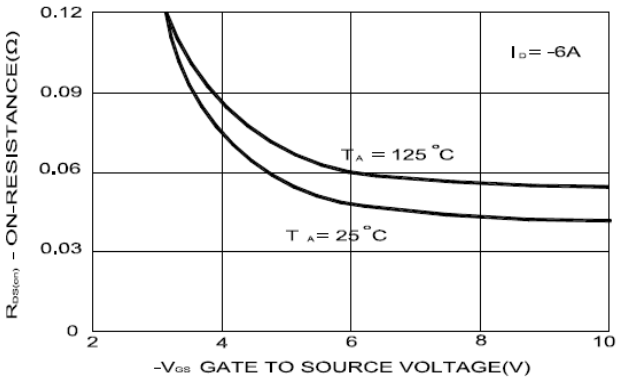

ON-RESISTANCE VARIATION WITH DRAIN CURRENT AND GATE VOLTAGE



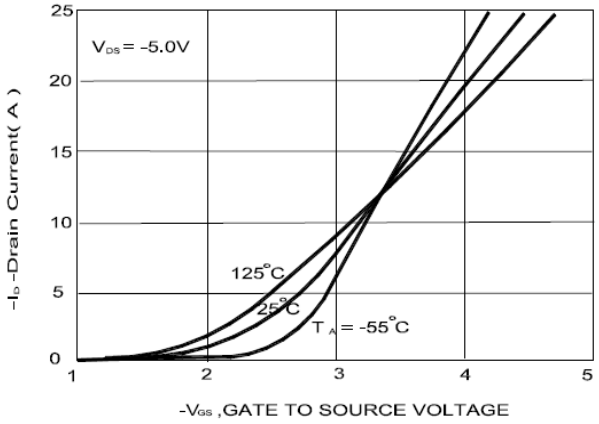

ON-RESISTANCE VARIATION WITH TEMPERATURE



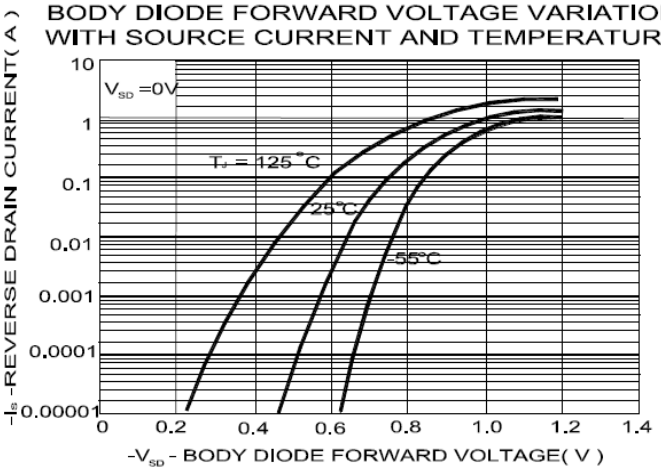

ON-RESISTANCE VARIATION WITH GATE-TO-SOURCE VOLTAGE




Transfer Characteristics




BODY DIODE FORWARD VOLTAGE VARIATION WITH SOURCE CURRENT AND TEMPERATURE



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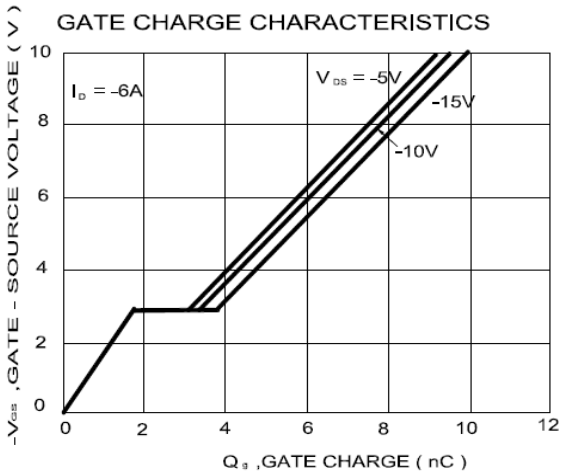


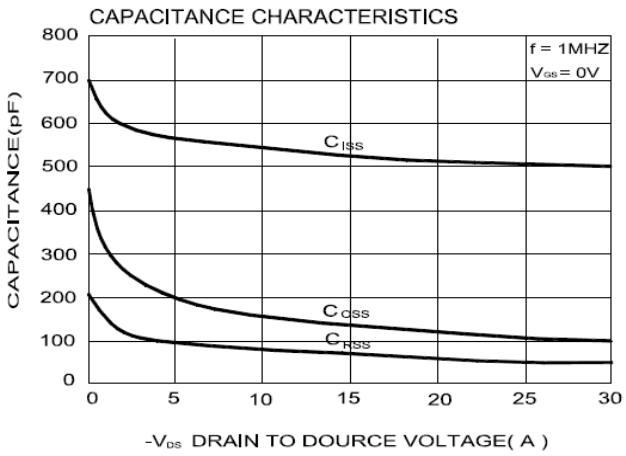


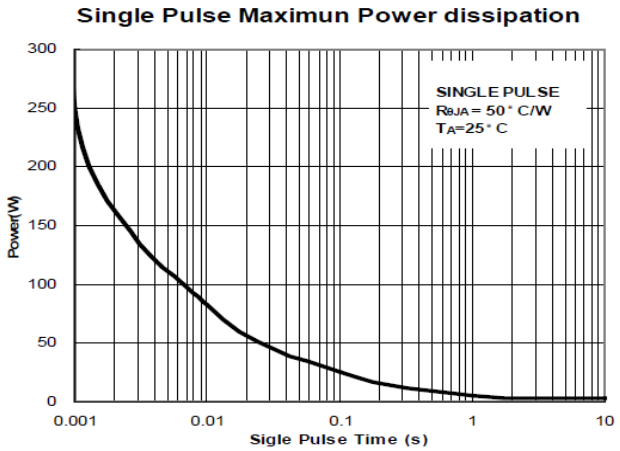


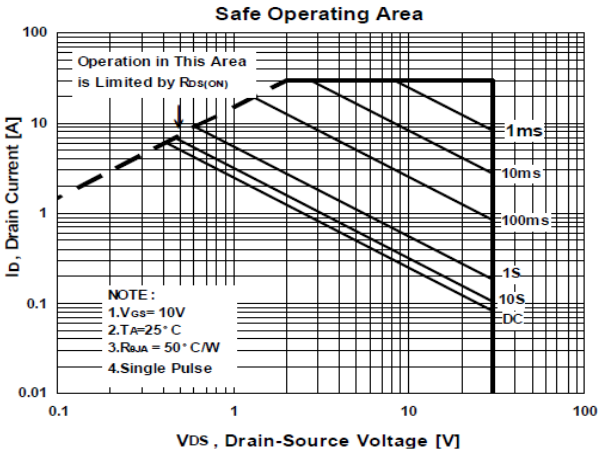


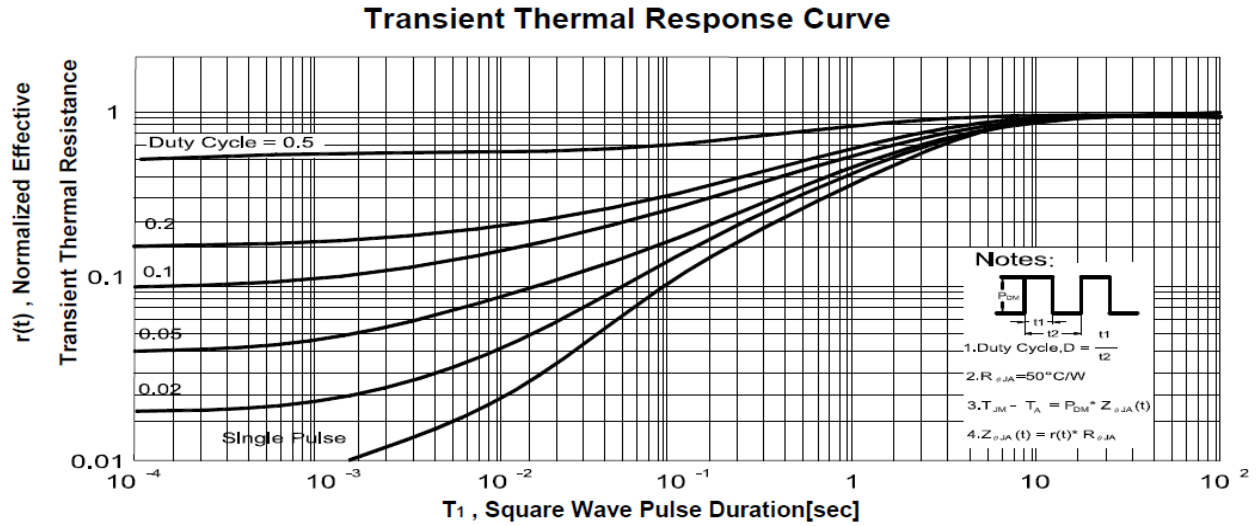

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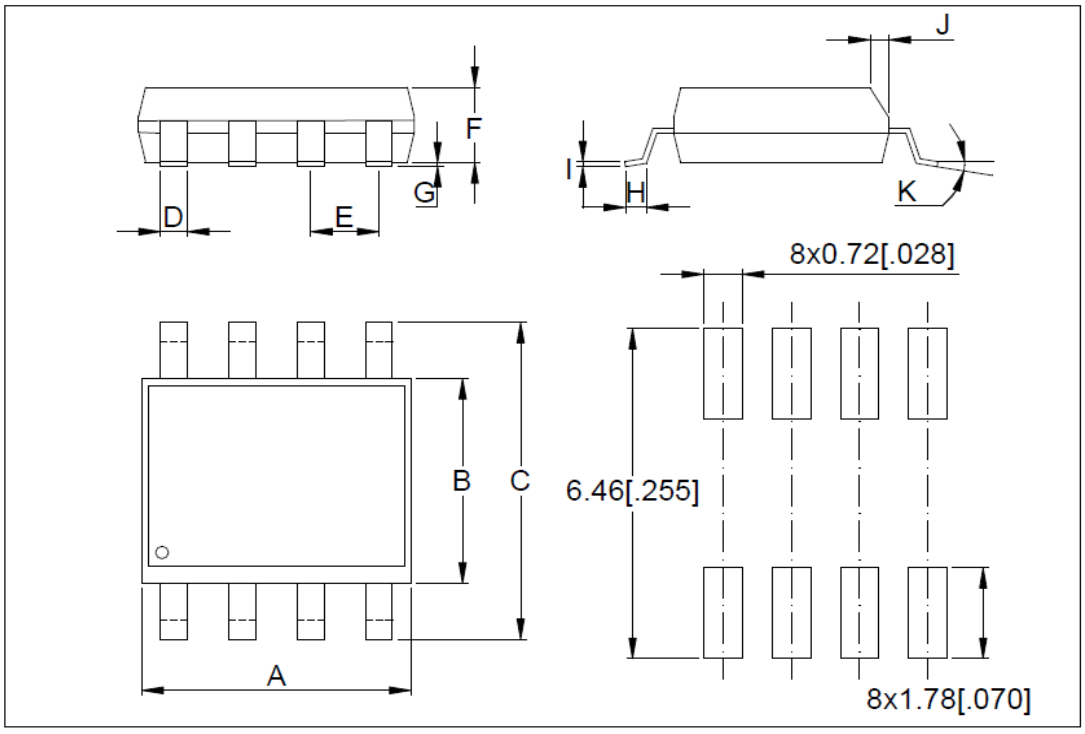
## P-Channel Logic Level Enhancement Mode MOSFET

### Package Dimension

## SOP-8 MECHANICAL DATA

| Dimension | mm | | | Dimension | mm | | |
|---|---|---|---|---|---|---|---|
| | Min. | Typ. | Max. | | Min. | Typ. | Max. |
| A | 4.8 | 4.9 | 5.0 | H | 0.4 | 0.6 | 0.93 |
| B | 3.8 | 3.9 | 4.0 | I | 0.19 | 0.21 | 0.25 |
| C | 5.79 | 6.0 | 6.2 | J | 0.25 | 0.375 | 0.5 |
| D | 0.33 | 0.4 | 0.51 | K | 0° | 3° | 18° |
| E | 1.25 | 1.27 | 1.29 | | | | |
| F | 1.1 | 1.3 | 1.65 | | | | |
| G | 0.05 | 0.15 | 0.25 | | | | |



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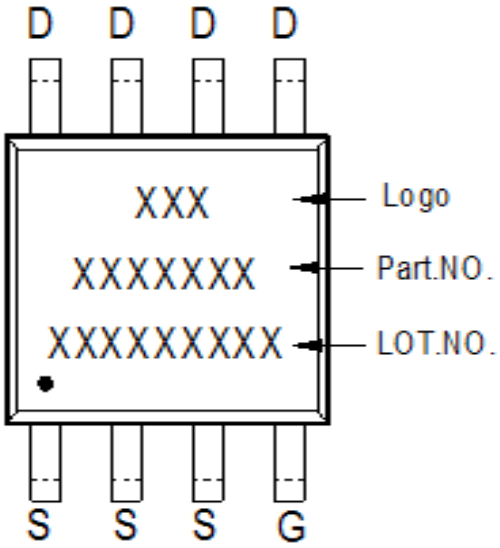
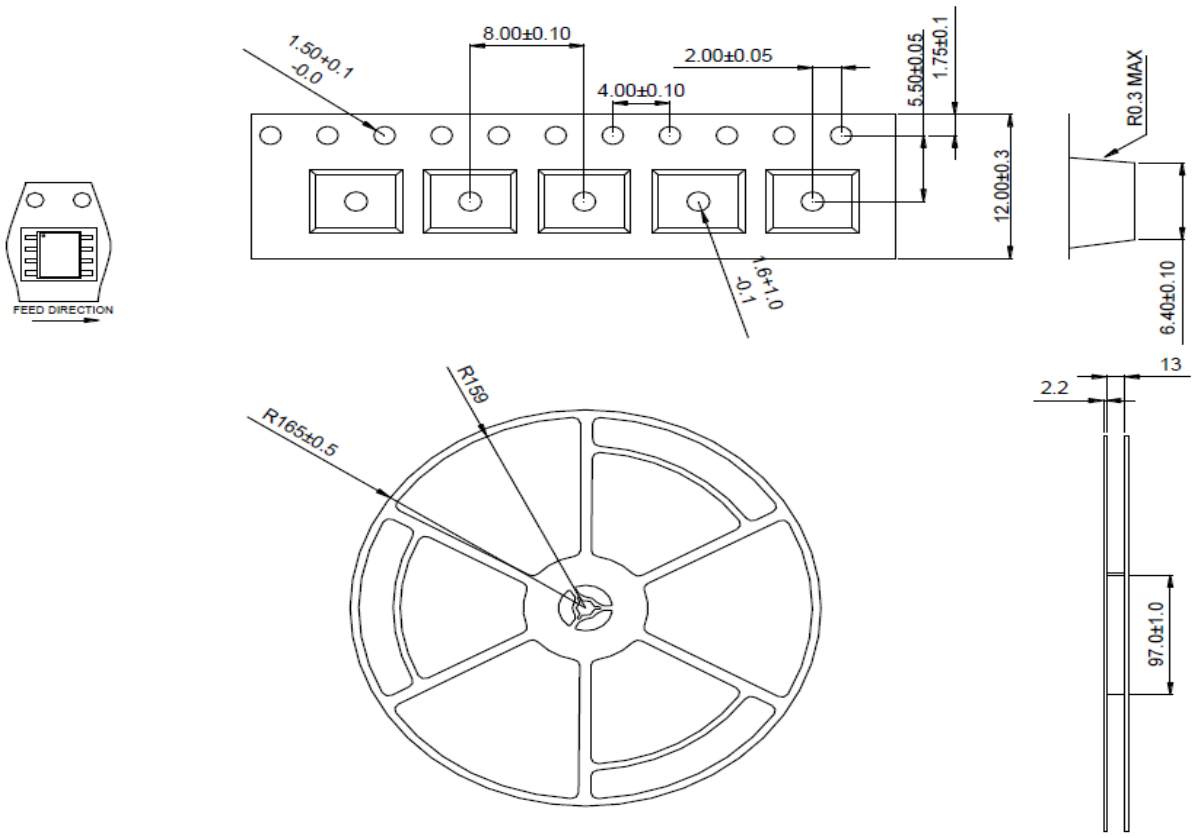
## P-Channel Logic Level Enhancement Mode MOSFET

## A. Marking Information




## B. Tape&Reel Information:2500pcs/Reel



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## P-Channel Logic Level Enhancement Mode MOSFET

## C. Lot.No. & Date Code rule

### 1.LOT.NO.

M N 15M21 03

- 03 → #8~9 Sub-lot No
- 15M21 → Order series no.
- N → Foundry site
- M → Assembly site

### 2.Date Code

D Y M X XXX

- XXX → Order series no. & Sub-lot No
- X → Week
- M → M : Month (A:Jan , B:Feb , C:Mar ,D :Apr ,E:May ,F:Jun,G:Jul,H:Aug,I:Sep,J:Oct,K:Nov,L:Dec.)
- Y → Y : Year (N : 2011, O : 2012 ...)
- D → Assembly site

### 3.Date Code (for Small package)

XX Y WW

- WW → Week
- Y → Y : Year (9: 2009,A : 2010, B : 2011 ...)
- XX → Device Name

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## P-Channel Logic Level Enhancement Mode MOSFET

## D.Label rule

标签内容(Label content)


| | | |
|---|---|---|
| 1 | Label Size | 30 * 90 mm |
| 2 | Font style | Times New Roman or Arial<br>(或可区分英文”0”和数字”0”，”G和”Q”的字型即可) |
| 3 | Great Power | Height: 4 mm |
| 4 | Package | Height: 2 mm |
| 5 | Date | Height: 2 mm Shipping date: YYYY/MM/DD, ex. 2008/09/12 |
| 6 | Device | Height: 3 mm (Max: 16 Digit) |
| 7 | Lot | Height: 3 mm (Max: 9 Digit) Sub lot |
| 8 | D/C | Height: 3 mm (Max: 7 Digit) |
| 9 | QTY | Height: 3 mm (Max: 6 Digit) Thousand mark is no needed |
| 10 | Pb Free label | Pb Diameter: 1 cm bottom color: Green<br>Font color: Black Font style: Arial |
| 11 | Halogen Free label | G Diameter: 1 cm bottom color: Green<br>Font color: Black Font style: Arial |
| 12 | Scan info | Device / Lot / D/C / QTY , Insert “ / “ between every parts.<br>for example: P3055LDG/G12345601/GGG2301/2000<br>DPI (Dots per inch): Over 300 dpi<br>Code : Code 128<br>Height: 6 mm at least |