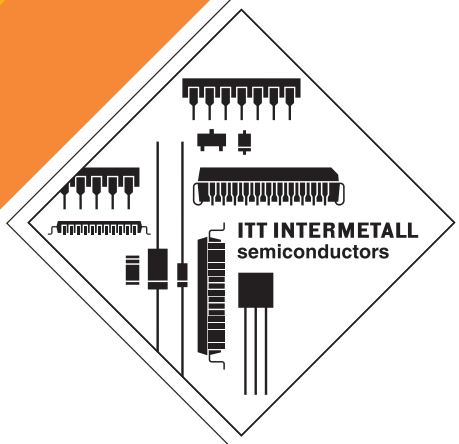


PRELIMINARY DATA SHEET

MSP 3410 B
Multistandard
Sound Processor

Edition Nov. 20, 1995
6251-366-9PD

ITT INTERMETALL

Contents

Contents, continued

Multistandard Sound Processor

Release Notes:

The hardware description in this document is valid for the MSP 3410 B version F7 and following versions. The suffix “B” in the name denotes the requirements of the crystal with modified specifications.

For a brief history survey, please see appendix “MSP 3410 B Technical Code History”.

The present document is version 0.8. Revision bars indicate significant changes to revision 0.7.

1. Introduction

The **MSP 3410 B** is a single-chip Multistandard Sound Processor for applications in analog and digital TV sets, satellite receivers and video recorders.

The MSP-family, which goes back to the MSP 2400, demonstrates in an impressive way the progressive development towards highly integrated ICs, offering more and more features and flexibility. The development of the MSP 2410 included an automatic gain control but reduced the amount of external components. The MSP 2410 reached a high level of performance and is the basis for the new generation.

The **MSP 3410 B** increases function integration in a spectacular way. By including the MSP2410 as a library cell and combining it with AD/DA converters and high performance digital signal processing, the chip offers a wide range of features. The complete TV-sound-processing, starting at the Sound-IF domain, will be performed by one single IC. The inputs of the IC are analog audio signals in baseband and at intercarrier position. The MSP 3410 B covers the sound processing of a wide range of TV-standards. Some examples are listed in Table 3–1.

The MSP 3410 B is produced in 1.0 µm CMOS technology and is available in 68-pin PLCC and in 64-pin PSDIP packages.

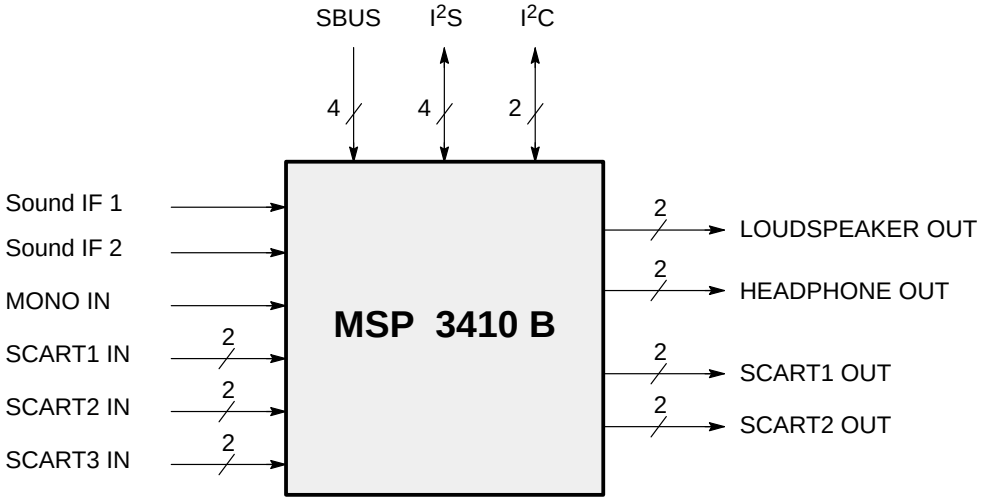


Fig. 1–1: Main I/O Signals MSP 3410 B

2. Features of the MSP 3410 B

2.1. Features of the Demodulator and Decoder Sections

The MSP 3410 B is designed to simultaneously perform digital demodulation and decoding of NICAM-coded TV stereo sound, as well as demodulation of FM-mono TV sound. Alternatively, two carrier FM systems according to the German or Korean terrestrial specs or the satellite specs can be processed with the MSP 3410 B.

Since it is simple and economic to demodulate AM sound carriers with conventional sound-IF-mixing units, the AM demodulation feature of the MSP will seldom be used. However, for FM carrier detection in satellite operation the AM demodulation offers a powerful feature to calculate the carrier field strength, which can be used for automatic search algorithms. So the IC facilitates a first step towards multistandard capability with its very flexible application and may be used in TV-sets, satellite tuners and video recorders.

The MSP 3410 B facilitates profitable multistandard capability, offering the following advantages:

– two selectable analog inputs (TV- and SAT-IF sources)

– Automatic Gain Control (AGC) for analog input: input range: 0.14 – 3 Vpp

– integrated A/D converter for sound-IF inputs

– all demodulation and filtering is performed on chip and is individually programmable

– simple realization of both digital NICAM standards (UK/Scandinavia)

– no external filter hardware is required

– only one crystal clock (18.432 MHz) is necessary

– Pay-TV for NICAM-mode

– FM carrier level calculation for automatic search algorithms and carrier mute function

– high deviation FM-mono mode (max. deviation: approx. ±360 kHz)

2.2. Features of the DSP-Section

– flexible selection of audio sources to be processed

– digital input and output interfaces via S-Bus for DMA-via AMU, and via I^2S-Bus for external DSP-Processors featuring Graphic Equalizer, Surround Sound etc.

– performance of all deemphasis systems including adaptive Wegener Panda 1 without external components or controlling

– performance of D2MAC audio together with an AMU 2481

– digitally performed FM-identification decoding and dematrixing

– digital baseband processing: volume, bass, treble, pseudostereo and basewidth enlargement

– simplified controlling of volume, bass, treble etc.

– increased audio bandwidth for FM-Audio-signals (20 Hz – 15 kHz , ±1 dB)

2.3. Features of the Analog Section

– three selectable analog pairs of audio baseband inputs (=three SCART inputs)
Input level: ≤ 2 V RMS;
input impedance: ≥25 kΩ

– one selectable analog mono input (i.e. AM sound);
Input level: ≤ 2 V RMS;
input impedance: ≥10 kΩ

– two high quality A/D converters; S/N-Ratio: ≥85 dB

– 20 Hz to 20 kHz Bandwidth for SCART-to-SCART-Copy facilities

– MAIN (loudspeaker) and AUX (headphones): two pairs of 4-fold oversampled D/A-converters
Output level per channel: max. 1.4 VRMS
Output resistance: max. 5 kΩ
S/N-Ratio: ≥85 dB at maximum volume
max. noise voltage in mute mode: ≤ 10 µV (BW: 20 Hz ... 16 kHz)

– one pair of four-fold oversampled D/A-converters supplying two selectable pairs of SCART-Outputs. Output level per channel: max. 2 V RMS, output resistance: max. 0.5 kΩ, S/N-Ratio: ≥85 dB
(20 Hz ... 16 kHz)

3. Application Fields of the MSP 3410 B

In the following sections, a brief overview about the two main TV sound standards, NICAM 728 and German FM-Stereo, demonstrates the complex requirements of a multistandard audio IC.

3.1. NICAM plus FM-Mono

According to the British, Scandinavian and Spanish TV-standards, high quality stereo sound is transmitted digitally. The systems allow two high quality digital sound channels to be added to the already existing FM channel. The sound coding follows the format of the so-called Near Instantaneous Companding System (NICAM 728). Transmission is performed using Differential Quadrature Phase Shift Keying (DQPSK). Table 3–2 gives some specifications of the sound coding (NICAM); Table 3–3 offers an overview of the modulation parameters.

In the case of NICAM/FM mode there are three different audio channels available: NICAM A,NICAM B and FM-mono. NICAM A and B may belong either to a stereo or to a dual language transmission. Information about operation mode and about the quality of the NICAM signal can be read by the CCU via the control bus. In the case of low quality (high bit error rate) the CCU may decide to switch to the analog FM-mono sound.

3.2. German 2-Carrier System (DUAL FM System)

Since September 1981, stereo and dual sound programs have been transmitted in Germany using the 2-carrier system. Sound transmission consists of the already existing first sound carrier and a second sound carrier additionally containing an identification signal. Some more details of this standard are given in Table 3–4.

Table 3–1: European TV standards

TV-System	Position of Sound Carrier /MHz	Sound Modulation	Color System	Country
B/G	5.5/5.74	FM-Stereo	PAL	Germany
B/G	5.5/5.85	FM-Mono/NICAM	PAL	Scandinavia,Spain
L	6.5/5.85	AM-Mono/NICAM	SECAM	France
I	6.0/6.552	FM-Mono/NICAM	PAL	UK
D,K	6.5	FM-Mono	SECAM	USSR
M	4.5	FM-Mono	NTSC	USA
Satellite Satellite	6.5 7.02/7.2	FM-Mono FM-Stereo	PAL PAL	Europe (ASTRA) Europe (ASTRA)

Table 3–2: Summary of NICAM 728 sound coding characteristics

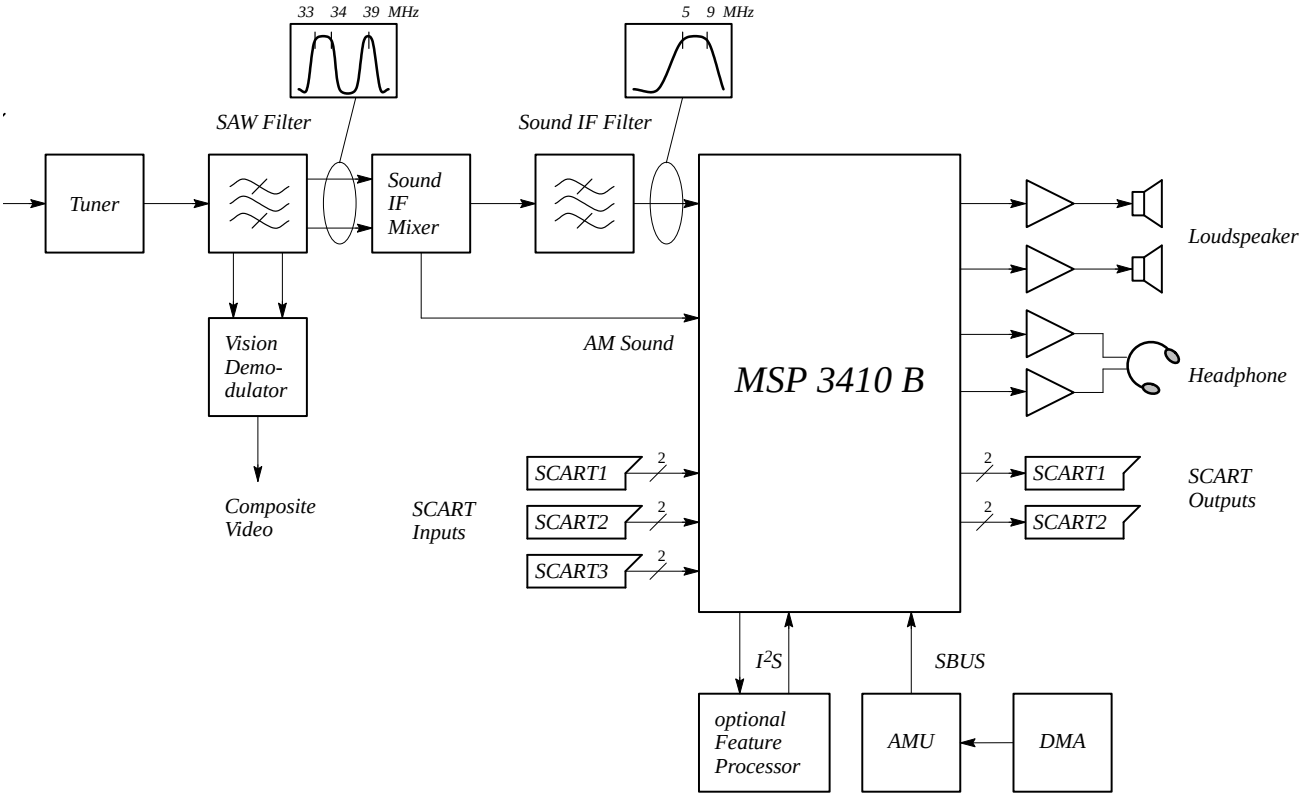
Characteristics	Values
Audio sampling frequency	32 kHz
Number of channels	2
Initial resolution	14 bit/sample
Companding characteristics	near instantaneous, with compression to 10 bits/sample in 32-samples (1 ms) blocks
Coding for compressed samples	2’s complement
Preemphasis	CCITT Recommendation J.17 (6.5 dB attenuation at 800 Hz)
Audio overload level	+12 dBm0 measured at the unity gain frequency of the preemphasis network (2 kHz)

Table 3–3: Summary of NICAM 728 sound modulation parameters

Specification	UK	Scandinavia/Spain	France	
Carrier frequency of digital sound	6.552 MHz	5.85 MHz	5.85 MHz	
Transmission rate	728 kBit/s 1 part/million			
Type of modulation	Differentially encoded quadrature phase shift keying (DQPSK)			
Spectrum shaping Roll-off factor	by means of Roll-off filters 1.0	0.4	0.4	
Carrier frequency of analog sound component	6.0 MHz FM mono	5.5 MHz FM mono	6.5 MHz AM mono terrestric	cable
Power ratio between vision carrier and analog sound carrier	10 dB	13 dB	10 dB	16 dB
Power ratio between analog and modulated digital sound carrier	10 dB	7 dB	17 dB	11 dB

Table 3–4: Key parameters for German 2-carrier sound system

Sound Carriers	Channel FM1	Channel FM2
Intercarrier frequencies	5.5 MHz	5.7421875 MHz
Vision/sound power difference	13 dB	20 dB
Sound bandwidth	40 Hz to 15 kHz	
Pre-emphasis	50 µs	
Frequency deviation	±50 kHz	
Sound Signal Components		
Mono transmission	mono	mono
Stereo transmission	(L+R)/2	R
Dual sound transmission	language A	language B
Identification of Transmission Mode on Channel 2		
Pilot carrier frequency		54.6875 kHz
Type of modulation		AM
Modulation depth		50%
Modulation frequency		mono: unmodulated stereo: 117.5 Hz dual: 274.1 Hz



According to the mixing characteristics of the Sound-IF mixer, the Sound-IF filter may be omitted.

Fig. 3–1: Typical MSP 3410 B application

4. Architecture of the MSP 3410 B

Fig. 4–1 shows a simplified block diagram of the IC. Its architecture is split into three functional blocks:

1. demodulator and decoder section

2. digital signal processing (DSP) section performing audio baseband processing

3. analog section containing two A/D-converters, 6 D/A-converters, and channel selection

4.1. Demodulator Block

4.1.1. Analog Sound IF – Input Section

The input pins ANA_IN1+, ANA_IN2+ and ANA_IN– offer the possibility to connect two different sound IF sources to the MSP 3410 B. By means of bit [8] of AD_CV (see Table 11–2) either terrestrial or satellite sound IF signals can be selected. The analog-to-digital conversion of the preselected sound IF signal is done by a flash-converter, whose output can be used to control an analog automatic gain circuit (AGC), providing optimum level for a wide range of input levels. It is possible to switch between automatic gain control and a fixed (setable) input gain. In the optimum case, the input range of the AD converter is completely covered by the sound if source. Some combinations of SAW filters and sound IF mixer ICs however show large picture components on their outputs. In this case filtering is recommended. It was found, that the high pass filters formed by the coupling capacitors at pins ANA_IN1+ and ANA_IN2+ (as shown in the application diagram) are sufficient in most cases.

4.1.2. Quadrature Mixers

The digital input coming from the integrated A/D converter may contain audio information at a frequency range of theoretically 0 to 9 MHz corresponding to the selected standards. By means of two programmable quadrature mixers two different audio sources, for example NICAM and FM-mono, may be shifted into baseband position. In the following, the two main channels are provided to process either:

– NICAM (channel 1) and FM mono (channel 2) simultaneously or, alternatively,

– FM2 (channel 1) and FM1 (channel 2).

Two independent digital oscillators are provided to generate two pairs of sin/cos-functions. Two programmable increments, to be divided up into Low- and High Part, determine frequency of the oscillator, which corresponds to the frequency of the desired audio carrier. In section 11.1., format and values of the increments are listed.

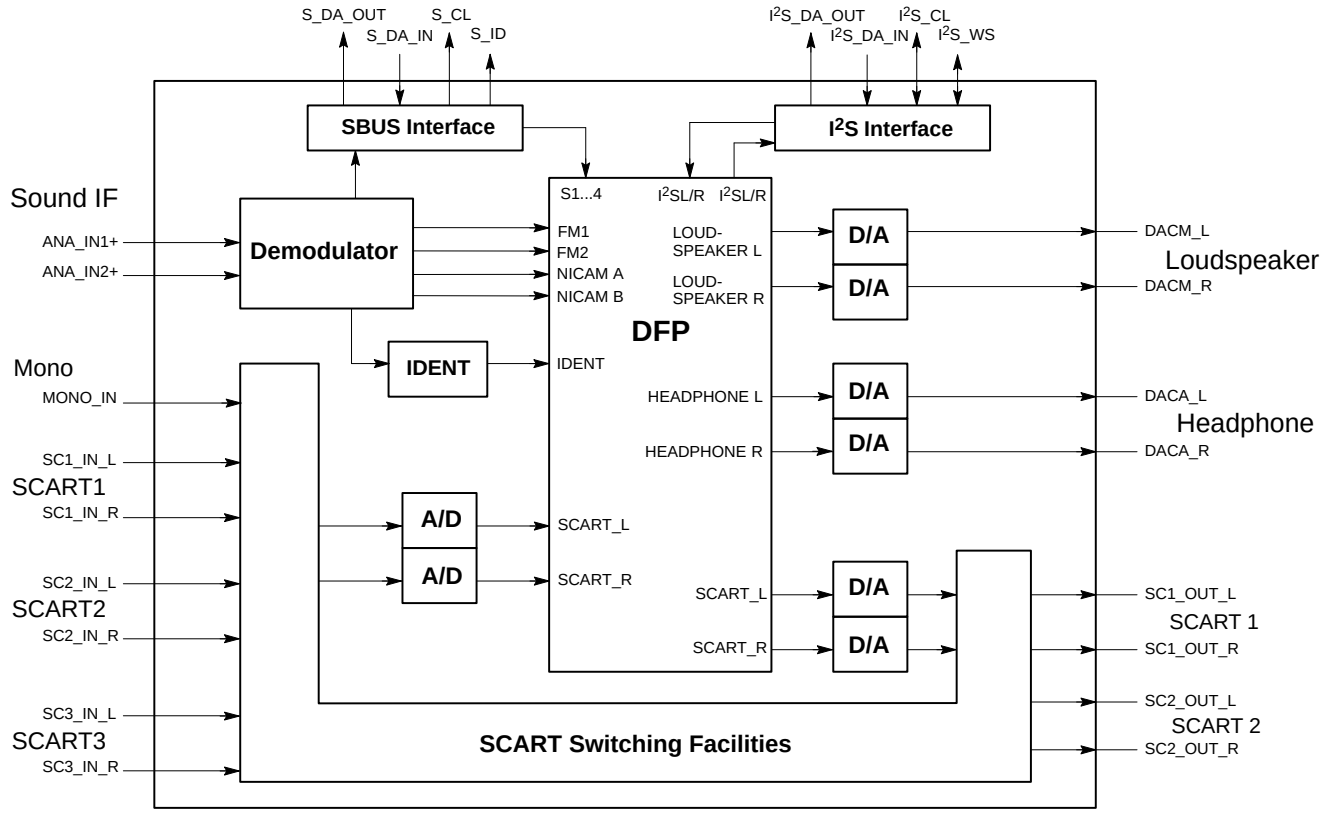


Fig. 4–1: Architecture of the MSP 3410 B

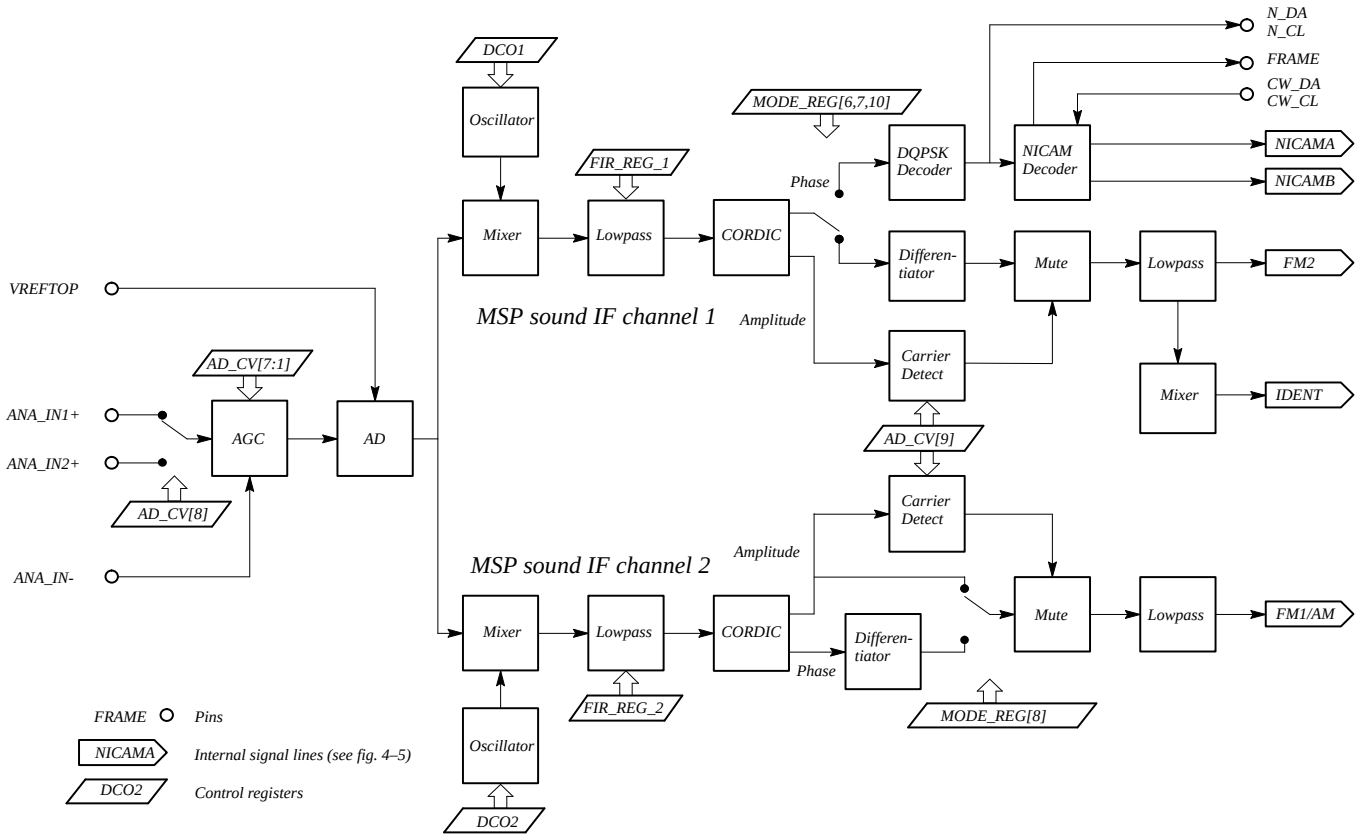


Fig. 4–2: Demodulator architecture

4.1.3. Lowpass Filtering Block for Mixed Sound IF Signals

By means of decimation filters the sampling rate is reduced. Then, data shaping and/or FM bandwidth limitation is performed by a linear phase Finite Impulse Response (FIR-filter). Just like the oscillators' increments the filter coefficients are programmable and are written into the IC by the CCU via the control bus. Thus, for example, different NICAM versions can easily be implemented. Two not necessarily different sets of coefficients are required, one for channel 1 (NICAM or FM2) and one for channel 2 (FM1=FM-mono). In section 11.2.3. several coefficient sets are proposed.

Since both MSP channels are designed to process the German FM Stereo System with the same FIR coefficient set (despite 7 dB power level difference of the two sound carriers), the MSP channel 1 has an internal overall gain of 6 dB. To process two carriers of identical power level these 6 dBs have to be taken into account by decreasing the values of the channel 1 coefficient set, which has already been done in table 11–7.

4.1.4. CORDIC Block

The filtered sound IF signals are demodulated by transforming the incoming signals from Cartesian into polar format by means of a CORDIC processor block. On the output, the phase and amplitude is available for further processing. AM signals are derived from the amplitude information whereas the phase information serves for FM and NICAM (DQPSK) demodulation.

4.1.5. Differentiators

FM demodulation is completed by differentiating the phase information output of the CORDIC block.

4.1.6. Lowpass Filter Block for Demodulated Signals

The demodulated FM and AM signals are further lowpass filtered and decimated to a final sampling frequency of 32 kHz. The usable bandwidth of the final baseband signals is about 15 kHz.

4.1.7. High Deviation FM Mode

By means of MODE_REG [9], the maximum FM-deviation can be extended to approximately ±360 kHz. Since this mode can be applied only for the MSP sound IF channel 2, the corresponding matrices in the baseband processing must be set to sound A. Apart from this, the coefficient sets 380 kHz FIR_REG2 or 500 kHz FIR_REG2 must be chosen for the FIR_REG_2. In relation to the normal FM-mode, the audio level of the high-deviation mode is reduced by 6 dB.

4.1.8. MSP-Mute Function in the Dual Carrier FM Mode

To prevent noise effects or FM identification problems in the absence of one of the two FM carriers the MSP 3410 B offers a carrier detection feature, which must be activated by means of AD_CV[9], see section 11.2.1. If no FM carrier is available at the MSP channel 1, the corresponding channel FM2 (and S-Bus output samples 3 and 4) are muted. If no FM carrier is available at the MSP channel 2, the corresponding channel FM1 (and S-Bus output samples 1 and 2) are muted. In case of the absence of both FM carriers pure noise will be amplified by the input AGC. Therefore a proper mute function depends on the noise quality of the TV set's IF part and cannot be guaranteed. The mute function is not recommended for the satellite mode.

4.1.9. DQPSK-Decoder

In case of NICAM-mode the phase samples are decoded according the DQPSK-Coding scheme. The output of this block contains the original NICAM-bitstream, which is available at the N-Bus interface.

4.1.10. NICAM-Decoder

Before any NICAM decoding can start, the MSP must lock to the NICAM frame structure by searching and synchronizing to the so-called Frame Alignment Words (FAW).

To reconstruct the original digital sound samples the NICAM-bitstream has to be descrambled, deinterleaved and rescaled. Also bit error detection and correction (concealment) is performed in this NICAM specific block.

To facilitate the Central Control Unit CCU to switch the TV-set to the actual sound mode, control information on the NICAM mode and bit error rate are supplied by the the NICAM-Decoder. It can be read out via the I^2C-Bus.

4.2. Analog Section: SCART Switches and Standby Mode

The analog input and output sections offer a wide range of switching facilities, which are shown in Fig. 4–3.To design a TV set with 3 pairs of SCART-inputs and two pairs of SCART-outputs, no external switching hardware is required.

The switches are controlled by the ACB bits defined in the audio processing interface (see section 12. Programming the Audio Processing Part).

If the MSP 3410 B is switched off by first pulling STANDBYQ low and then disconnecting the 5V but keeping the 8V power supply (**'Standby'-mode**), the switches S1, S2 and S3 maintain their position and function. This facilitates the copying from selected SCART-inputs to SCART-outputs in the TV-set's standby mode.

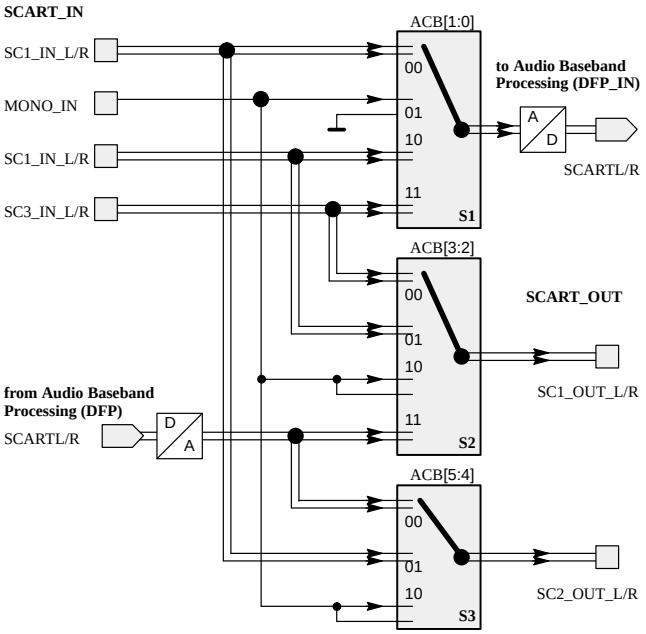


Fig. 4–3: SCART-Switching Facilities
Bold lines determine the default configuration

In case of power-on start or starting from standby, the IC switches automatically to the default configuration, shown in the figure above. This action takes place after the first I^2C transmission into the DFP part. By transmitting the ACB register first, the individual default setting mode of the TV set can be defined.

4.3. MSP 3410 B Audio Baseband Processing

By means of the DFP processor all audio baseband functions are performed by digital signal processing (DSP). The DSP functions are grouped into three processing parts: Input preprocessing, channel selection and channel postprocessing.

The input preprocessing is intended to prepare the various signals of all input sources in order to form a standardized signal at the input to the channel selector. The signals can be adjusted in volume, are processed with the appropriate deemphasis and are dematrixed if necessary.

Having prepared the signals that way, the channel selector makes it possible to distribute all possible source signals to the desired output channels.

The ability to route in an external coprocessor for special effects like graphic equalizer, surround processing, and sound field processing is of special importance. Routing can be done with each input source and output channel via the I^2S inputs and outputs.

All input and output signals can be processed simultaneously with the exception that FM2 cannot be pro-

cessed at the same time as NICAM. Note that the NICAM input signals are only available in the MSP 3410 B version. While processing the adaptive deemphasis, no dual carrier stereo (German or Korean) or NICAM processing is possible. Identification values are not valid either.

4.4. Dual Carrier FM Stereo/Bilingual Detection

In the German and Korean TV standard, audio information can be transmitted in three modes: Mono, stereo or bilingual. To obtain information about the current audio operation mode, the MSP 3410 B detects the so-called identification signal. Information is supplied via the Stereo Detection Register to an external CCU.

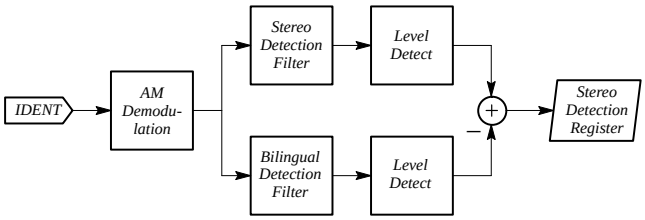


Fig. 4–4: Stereo/bilingual detection

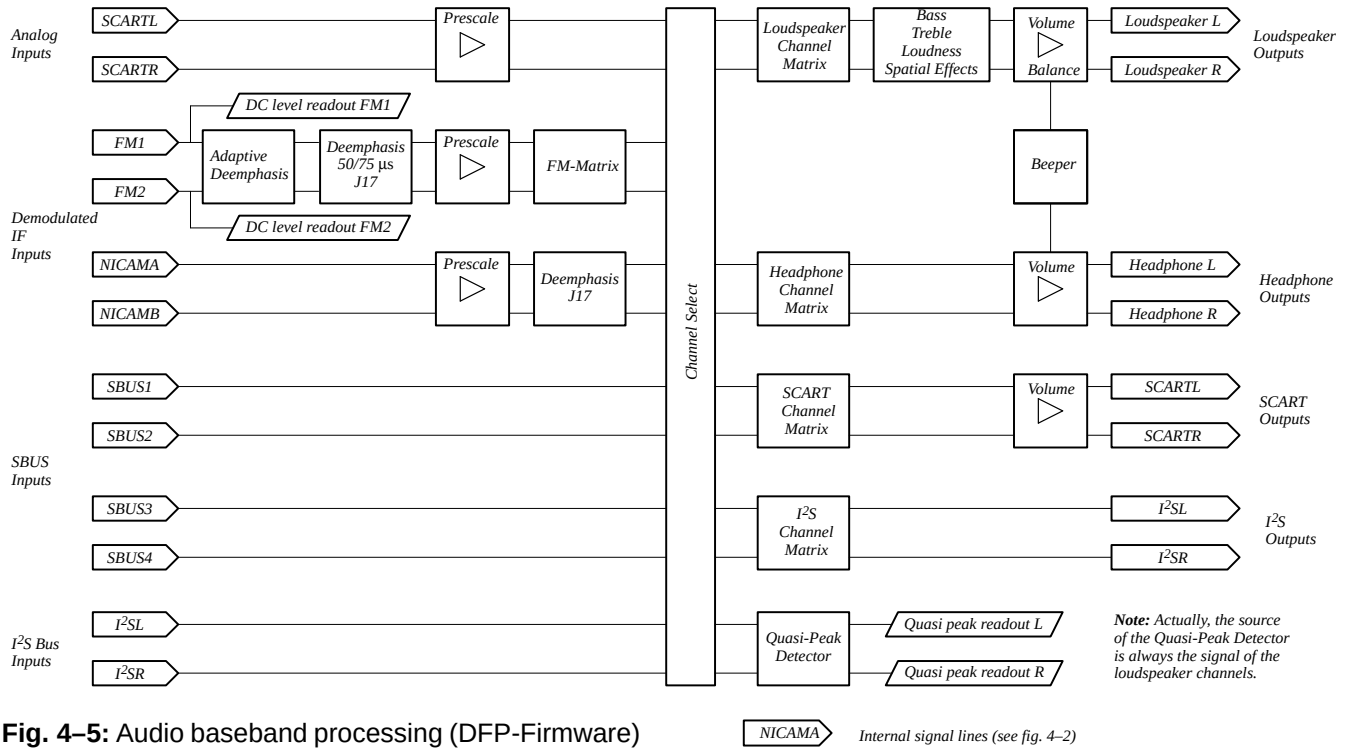


Fig. 4–5: Audio baseband processing (DFP-Firmware)

Table 4–1: Some examples for recommended channel assignments for demodulator and audio processing part

Mode	MSP Sound IF-Channel 1	MSP Sound IF-Channel 2	FM-Matrix	Channel-Select	Channel Matrix
B/G-Stereo	FM2 (5.74 MHz): 2R	FM1 (5.5 MHz): L+R	B/G Stereo	Speakers: FM	Stereo
B/G-Bilingual	FM2 (5.74 MHz): Sound B	FM1 (5.5 MHz): Sound A	No Matrix	Speakers: FM H. Phone: FM	Speakers: Sound A H. Phone: Sound B
NICAM-I-ST/ FM-mono	NICAM (6.552 MHz)	FM (6.0 MHz): mono	No Matrix	Speakers: NICAM H. Phone: FM	Speakers: Stereo H. Phone: Sound A
Sat-Mono	not used	FM (6.5 MHz): mono	No Matrix	Speakers: FM	Sound A
Sat-Stereo	7.2 MHz: R	7.02 MHz: L	No Matrix	Speakers: FM	Stereo
Sat-Bilingual	7.38 MHz: Sound C	7.02 MHz: Sound A	No Matrix	Speakers: FM H. Phone: FM	Speakers: Sound A H. Phone: Sound B=C
Sat-High Dev. Mode	don't care	6.552 MHz	No Matrix	Speakers: FM H. Phone: FM	Speakers: Sound A H. Phone: Sound A

5. Control Bus Interface

As a slave receiver, the MSP 3410 B can be controlled via I²C bus. Access to internal memory locations is achieved by subaddressing. The FP processor and the DFP processor parts have two separate subaddressing register banks.

In order to allow for more MSP 3410 B IC's to be connected to the control bus, an ADR_SEL pin has been implemented. With ADR_SEL pulled to high, the MSP 3410 B responds to changed device addresses, thus two identical devices can be selected. Other devices of the same family will have different subaddresses (e.g. 34X0).

By means of the RESET bit in the CONTROL register all devices with the same device address are reset.

The IC is selected by asserting a special device address in the address part of a I²C transmission. A device address pair is defined as a write address (80 hex or 84 hex) and a read address (81 hex or 85 hex). Writing is done by sending the device write address first, followed by the subaddress byte, two address bytes, and two data bytes. For reading, the read address has to be transmitted first by sending the device write address (80 hex or 84 hex) followed by the subaddress byte and two address bytes. Without sending a stop condition, reading of the addressed data is done by sending the device read address (81 hex or 85 hex) and reading two bytes of data. Refer to Fig. 5–1: I²C Bus Protocol and section 5.2. Proposal for MSP 3410 B I²C Telegrams.

Due to the internal architecture of the MSP 3410 B, the IC cannot react immediately to an I²C request. The typical response time is about 0.3 ms for the DFP processor part and 1 ms for the FP processor part if NICAM processing is active. If the receiver (MSP) can't receive another complete byte of data until it has performed some other functions, for example servicing an internal interrupt, it can hold the clock line I²C_CL LOW to force the transmitter into a wait state. The positions within a transmission where this may happen are indicated by 'Wait' in section 5.1. The maximum Wait-period of the MSP during normal operation mode is less than 7 ms.

I²C-Bus error conditions (valid only from TC17 on):
In case of any internal error, the MSPs wait-period is extended to 7.07 ms. Afterwards the MSP does not acknowledge (NAK) the device address. The data line will be left HIGH by the MSP and the clock line will be released. The master can then generate a STOP condition to abort the transfer.

By means of NAK, the master is able to recognize the error state and to reset the IC via I²C-Bus. While transmitting the reset protocoll (s. 5.2.4.) to 'CONTROL', the master must ignore the not acknowledge bits (NAK) of the MSP.

Table 5–1: I²C Bus Device and Subaddresses

Name	Binary Value	Hex Value	Hex Value	Mode	Function
		ADR_SEL=low	ADR_SEL=high		
MSP	**1000 000x**	**80/81**	**84/85**	**R/W**	**MSP device address**
CONTROL	0000 0000	00		W	software reset
TEST	0000 0001	01		W	only for internal use
WR_FP	0001 0000	10		W	write address FP
RD_FP	0001 0001	11		W	read address FP
WR_DFP	0001 0010	12		W	write address DFP
RD_DFP	0001 0011	13		W	read address DFP

Table 5–2: Control Register

Name	MSB	14	13..1	LSB
CONTROL	RESET	0	0	0

5.1. Protocol Description

Write to DFP or FP

S	hex 80	Wait	ACK	sub-addr	ACK	addr-byte high	ACK	addr-byte low	ACK	data-byte high	ACK	data-byte low	ACK	P

Read from DFP or FP

S	hex 80	Wait	ACK	sub-addr	ACK	addr-byte high	ACK	addr-byte low	ACK	S	hex 81	Wait	ACK	data-byte high	ACK	data-byte low	NAK	P

Write to Control or Test Registers

S	hex 80	Wait	ACK	sub-addr	ACK	data-byte high	ACK	data-byte low	ACK	P

Note: S = I^2C-Bus Start Condition from master
P = I^2C-Bus Stop Condition from master
ACK = Acknowledge-Bit: LOW on I^2C_DA from slave (=MSP, grey) or master (=CCU, hatched)
NAK = Not Acknowledge-Bit: HIGH on I^2C_DA from master (=CCU, hatched) to indicate 'End of Read' or from MSP indicating internal error state (not illustrated, only for version F7 on.)
Wait = I^2C-Clock line held low by the slave (=MSP) while interrupt is serviced (< 7 ms)

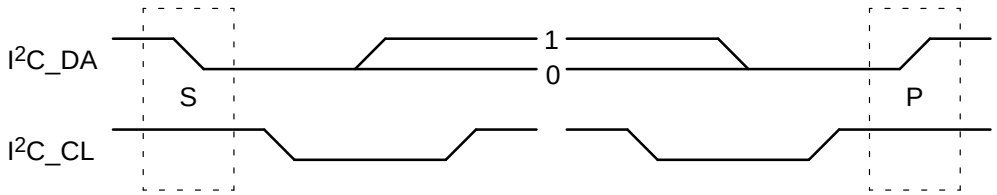


Fig. 5–1: I^2C bus protocol (MSB first; data must be stable while clock is high)

5.2. Proposal for MSP 3410 B I^2C Telegrams

5.2.1. Symbols

< Start Condition
> Stop Condition
aa Address Byte
dd Data Byte

5.2.2. Write Telegrams

```
<80 00 dd dd>          software RESET
<80 10 aa aa dd dd>    write data into FP register
<80 12 aa aa dd dd>    write data into DFP register
```

5.2.3. Read Telegrams

```
<80 11 aa aa <81 dd dd>  read data from FP register
<80 13 aa aa <81 dd dd>  read data from DFP register
```

5.2.4. Examples

```
<80 00 80 00>          RESET all MSP's statically
<80 00 00 00>          clear RESET
<80 12 00 08 01 20>    set loudspeaker channel source
                       to NICAM and Matrix to STEREO
```

5.3. Start Up Sequence

After power on or RESET the IC is in an inactive state. The CCU has to transmit the required coefficient set for a given operation via the I^2C bus. Initialization must start with the demodulator part. If required for any reason, from version F7 on, the audio processing part can be loaded before the demodulator part.

6. N-Bus Interface

The N-Bus interface consists of two lines, N-data and N-clock. The pure NICAM_728 data stream (before descrambling) is available together with a 728 kHz clock signal for the purpose of data transmission. N-Bus signals are based on TTL-levels. Data are latched with the falling clock edge.

7. Pay-TV Interface

The MSP 3410 B facilitates the reception of encrypted NICAM sound, which is provided by Pay-TV systems. By means of bit 1 of the control word 'MODE_REG' the operation mode 'PAY-TV' can be activated. The MSP 3410 B inherent descrambler generally uses a 9-bit start sequence, which initializes a pseudo random sequence generator each ms. In normal operation mode the 9-bit sequence exists of 9 bits having each high level, which are loaded automatically into the descrambler's shift register. In the Pay-TV mode these bits have to be loaded via the two pins CW_DA and CW_CL into the mentioned shift register. The time window to load one complete 9-bit sequence is given by the high time of the frame signal which is available on pin 5. It is not necessary to load a new sequence at each ms, because if no new sequence has been transmitted, the old one is saved. If less than 9 new bits at each ms are loaded, one has to consider that any new incoming bit shifts the old ones by one position inside the shift register. A complete timing diagram is illustrated in Fig. 7–1.

8. Audio PLL and Crystal Specifications

The MSP 3410 B requires a 18.432 MHz (10 pF, parallel) crystal. The clock supply of the whole system depends on the MSP 3410 B operation mode:

1. FM-Stereo:
The system clock runs free on the crystal's 18.432 MHz.

2. D2-MAC operation:
In this case, the system clock is locked to a synchronizing signal (DMA_SYNC) supplied by the D2-MAC chip. The DMA and the AMU chips can be driven by the MSP 3410 B audio clock (AUD_CL_OUT).

3. NICAM and FM_mono:
An integrated clock PLL uses the 364 kHz baud-rate, accomplished in the NICAM demodulator block, to lock the system clock to the bit rate respective 32 kHz sampling rate of the NICAM transmitter. As a result, the whole audio system is supplied with a controlled 18.432 MHz clock.

Remark on using the crystal:
External capacitors at each crystal pin to ground are required. They are necessary for tuning the open-loop frequency of the internal PLL and for stabilizing the frequency in closed-loop operation. The higher the capacitors, the lower the clock frequency results. The nominal free running frequency should match the center of the tolerance range between 18.433 and 18.431 MHz as closely as possible.

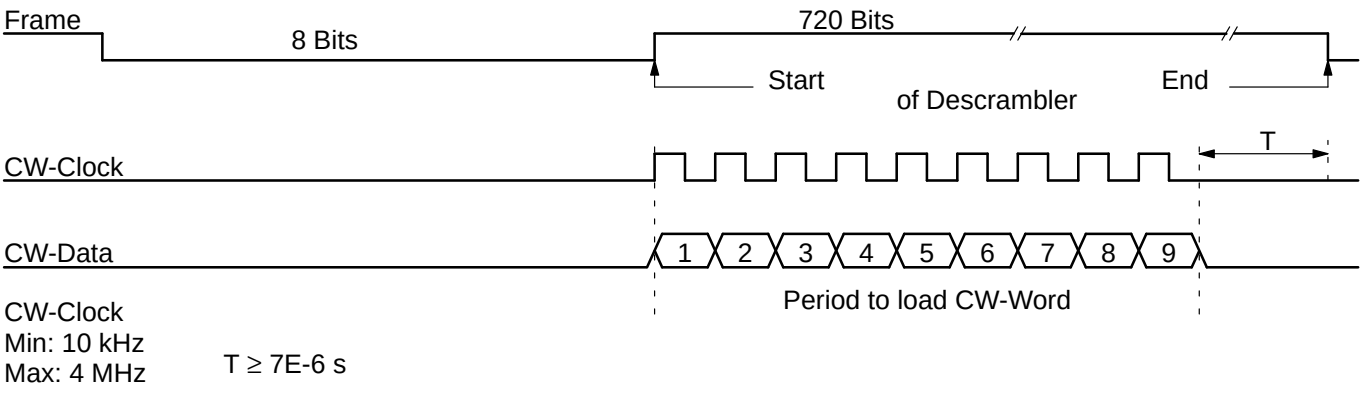


Fig. 7–1: Timing for Pay-TV signals

9. S-Bus Interface

Digital audio information provided by the DMA2381 via the AMU is serially transmitted to the MSP 3410 B via the S-Bus. The MSP 3410 B always has the master function.

The S-Bus interface consists of four pins:

1. S_DA_IN:
Four channels (4*16 bits) per sampling cycle (32 kHz) are transmitted.

2. S_CL:
Gives the timing for the transmission of S-DATA (4.608 MHz).

3. S_ID:
After 64 S-CLOCK cycles the S_ID determines the end of one sampling period.

4. S_DA_OUT:
FM-Demodulator or NICAM decoder output for test purpose.

10. I^2S Bus Interface

By means of this standardized interface, additional feature processors can be connected to the MSP 3410 B. Two possible formats are supported: The standard mode (MODE_REG[4]=0) selects the SONY format, where the I^2S_WS signal changes at the word boundaries. The so-called PHILIPS format, which is characterized by a change of the I^2S_WS signal one I^2S_CL period before the word boundaries, is selected by setting MODE_REG[4]=1.

The MSP 3410 B normally serves as the master on the I^2S interface. Here the clock and word strobe lines are driven by the MSP 3410 B. By setting MODE_REG[3]=1, the MSP 3410 B is switched to a slave mode. Now these lines are input to the MSP 3410 B and the master clock is synchronized to 576 times the I^2S_WS rate (32 kHz). No NICAM or D2MAC operation is possible in this mode.

The I^2S bus interface consists of four pins:

1. I^2S_DA_IN:
For input, two channels (2*16 bits) per sampling cycle (32 kHz) are transmitted.

2. I^2S_DA_OUT:
For output, two channels (2*16 bits) per sampling cycle (32 kHz) are transmitted.

3. I^2S_CL:
Gives the timing for the transmission of I^2S serial data (1.024 MHz).

4. I^2S_WS:
The I^2S_WS word strobe line defines the left and right sample.

11. Programming the Demodulator Part

11.1. Write Registers: Table and Addresses

In Table 11–1 all Write Registers are listed.

All transmissions on the control bus are 16 bits wide. Data for the demodulator part (FP) have 8 or 12 significant bits. These data have to be inserted LSB bound and filled with zero bits into the 16 bit transmission word.

Accessing a process address starts specific actions in the FP processor. For example addressing register 60_{hex} activates the internal transfer of all preloaded data (MODE_REG, DCO1_LO/HI) into their final hardware registers. It's only the access of the address 60_{hex} that counts, the two data bytes in the transmission have no meaning. Table 4–1 explains how to assign FM carriers to the MSP-Sound IF channels and the corresponding matrix modes in the audio processing part.

Table 11–1: MSP 3410 B write registers

Register	**Write Address (hex)**	**Function**
AD_CV	00BB	input selection, configuration of AGC and Mute Function and selection of A/D-converter
MODE_REG	0083	mode register
FIR_REG_1 FIR_REG_2	0001 0005	serial shift register for 6 · 8 bit, filter coefficient channel 1 (48 bit) serial shift register for 6 · 8 bit, + 2 · 12 bit off set (total 72 bit)
DCO1_LO DCO1_HI DCO2_LO DCO2_HI	0093 009B 00A3 00AB	increment channel 1 Low Part increment channel 1 High Part increment channel 2 Low Part increment channel 2 High Part
FAWCT_SOLL FAW_ER_TOL	0107 010F	To synchronize to the frame structure of the NICAM bit stream, the MSP checks the data for Frame Alignment Words (FAWs). After having captured the first one, the MSP continues to check for n frame periods. On having found at least n-m FAWs after this period, the frame synchronism is achieved and the MSP switches to active NICAM-decoding. The value for n has to be loaded into FAWCT_SOLL; the one for m into FAW_ER_TOL. Proposal : n=12; m=2
AUDIO_PLL	02D7	audio PLL in case of NICAM operation mode: 0 always open; 1 to be closed = default
Process	**Address (hex)**	**Function**
LOAD_REG_1/2	0056	After switch on or changing the TV system (B/G to I, I to B/G) all write-parameters have to be transmitted via I^2C-Bus into the MSP 3410 B. Then 'Load_REG_1/2' writes them into the corresponding registers. FM-processing starts. These are MODE_REG, DCO1/2_LO/HI.
LOAD_REG_1	0060	In the case of a TV-Standard change in MSP channel 1, only new channel 1 parameters have to be transmitted into the IC via I^2C-Bus. These are: MODE_REG, DCO1_LO/HI. LOAD_REG_1 sets up the MSP channel 1 without interrupting the MSP channel 2 (FM1 or MONO channel).
SEARCH_NICAM	0078	To start the NICAM-processing, this address has to be transmitted into the FP.
SELF_TEST	0792	Check of the FP ALU (for testing only)

Note: The WRITE-Addresses **cannot** be used to read back the corresponding register values.

11.2. Write Registers: Functions and Values

In the following, the functions of some registers are explained and their (default) values are defined:

11.2.1. Setting of Parameter AD_CV

Table 11–2: AD_CV Register

AD_CV 00BB$_{hex}$		
Bit	**Meaning**	**Settings**
AD_CV [0]	test	0 = on (default) 1 = off (for testing)
AD_CV [6:1]	Reference level in case of Automatic Gain Control = on (see Table 11–3). Constant gain factor when Automatic Gain Control = off (see Table 11–4).	
AD_CV [7]	Determination of Automatic Gain or Constant Gain	0 = constant gain 1 = automatic gain
AD_CV [8]	Selection of analog input	0 = ANALOG IN1 1 = ANALOG IN2
AD_CV [9]	MSP-Carrier-Mute Function	0 = off (no mute) 1 = on (mute as described in section 4.1.)
AD_CV[10]	NICAM-FIFO-Watchdog (only for test mode)	0 = on (default) 1 = off (for testing)
AD_CV[15:11]	reserved	0

Table 11–3: Reference values for active AGC (AD_CV[7] = 1)

Application	**Input Signal Contains**	**AD_CV [6:1] Ref. Value**	**AD_CV [6:1] in integer**	**Range of Input Signal at pin 41 or 43**
Terrestrial TV	2 FM Carriers or 1 FM and 1 NICAM Carrier	101000	40	0.14 – 3 V_{pp}[1)]
SAT	1 or more FM Carriers	100011	35	0.14 – 3 V_{pp}[1)]
NICAM only	1 NICAM Carrier only	010100	20	0.07 – 1.0 V_{pp}

[1)] For signals above 1.4 Vpp, the minimum gain of 3 dB is switched and overflow of the AD converter may result. Due to the robustness of the internal processing, the IC works up to and even more than 3 Vpp, if norm conditions of FM/NICAM or FM1/FM2 ratio are supposed. In this overflow case, a loss of FM-S/N-ratio of about 10 dB may appear.

Table 11–4: AD_CV parameters for constant input gain (AD_CV[7]=0)

Step	AD_CV [6:1] Constant Gain	Gain	Input Level at pin ANA_IN1+ and ANA_IN2+
0	000000	3.00 dB	maximum input level: 3 V_{pp} (FM) or 1 V_{pp} (NICAM)[1)]
1	000001	3.85 dB	
2	000010	4.70 dB	
3	000011	5.55 dB	
4	000100	6.40 dB	
5	000101	7.25 dB	
6	000110	8.10 dB	
7	000111	8.95 dB	
8	001000	9.80 dB	
9	001001	10.65 dB	
10	001010	11.50 dB	
11	001011	12.35 dB	
12	001100	13.20 dB	
13	001101	14.05 dB	
14	001110	14.90 dB	
15	001111	15.75 dB	
16	010000	16.60 dB	
17	010001	17.45 dB	
18	010010	18.30 dB	
19	010011	19.15 dB	
20	010100	20.00 dB	maximum input level: 0.14 V_{pp}

[1)] For signals above 1.4 Vpp, the minimum gain of 3 dB is switched and overflow of the AD converter may result. Due to the robustness of the internal processing, the IC works up to and even more than 3 Vpp, if norm conditions of FM/NICAM or FM1/FM2 ratio are supposed. In this overflow case, a loss of FM-S/N-ratio of about 10 dB may appear.

11.2.2. Control Register ‘MODE_REG’

The register ‘MODE_REG’ contains the control bits determining the operation mode of the MSP 3410 B; Table 11–5 explains all bit positions.

Table 11–5: Control word ‘MODE_REG’: all bits are “0” after power-on-reset

MODE_REG 0083_{hex}				
Bit	**Function**	**Comment**	**Definition**	**Recom-mendation**
[0]	DMA_SYNC[1)]	Synchronization to DMA	0 = NICAM (intern. Sync) 1 = D2MAC (ext. Sync)	X
[1]	PAYTV_EN	Pay-TV	0 = off 1 = on	0
[2]	DESCR_DIS	NICAM-Descrambler	0 = on 1 = off	0
[3]	I^2S Mode[1)]	Master/Slave mode of the I^2S bus	0 = Master 1 = Slave	X
[4]	I^2S_WS Mode	WS due to the Sony or Philips-Format	0 = Sony 1 = Philips	X
[5]	Audio_CL_OUT	Switch Audio_Clock_Output to tristate	0 = on 1 = tristate	X
[6]	NICAM[1)]	MSP-channel 1 mode	0 = FM 1 = Nicam	X

MODE_REG 0083$_{hex}$				
Bit	**Function**	**Comment**	**Definition**	**Recom-mendation**
[7]	FM1 FM2	MSP-channel 1 mode	0 = Nicam 1 = FM	X
[8]	FM AM	MSP-channel 1/2 mode	0 = FM 1 = AM	0
[9]	HDEV	High Deviation Mode (channel matrix must be sound A)	0 = normal 1 = high deviation mode	0
[10]	S-Bus Setting	configuration of internal sound bus	0 = Nicam/FM-Mono 1 = Two Carrier FM	X
[11]	S-Bus Mode[2)]	mode of sound bus[3)]	0 = Tristate 1 = Active	0
[15:12]	reserved	reserved	must be 0	0
[1)] In case of NICAM operation, I^{2}S-slave mode or synchronization to DMA not possible. In case of synchonization to DMA, no I^{2}S-slave mode or NICAM is allowed. In case of I^{2}S-slave mode, no synchonization to DMA or NICAM is allowed. [2)] The normal operation mode is 'Active' [3)] To reduce radiation, the pins S_DA_OUT, S_CL, and S_ID should be switched to tristate if not used. IF S-Bus Mode = 'tristate', pins 'Frame', N_CL, and N_DA are also switched to tristate.				X: Depend-ing on mode

11.2.3. FIR-Parameter

The following data values (see Table 11–6) are to be transferred **8 bits at a time embedded LSB-bound in a 16 bit word**. Note: These sequences must be obeyed. To change a coefficient set, the complete block FIR_REG_1 or FIR_REG_2 must be transmitted. The new coefficient set will be active without a load_reg routine.

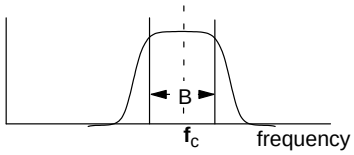
Table 11–6: Loading sequence for FIR-coefficients

FIR_REG_1 0001$_{hex}$ (Channel 1: NICAM/FM2)			
No.	**Symbol Name**	**Bits**	**Value**
1	NICAM/FM2_Coeff. (5)	8	see Table 11–7.
2	NICAM/FM2_Coeff. (4)	8	
3	NICAM/FM2_Coeff. (3)	8	
4	NICAM/FM2_Coeff. (2)	8	
5	NICAM/FM2_Coeff. (1)	8	
6	NICAM/FM2_Coeff. (0)	8	

FIR_REG_2 0005$_{hex}$ (Channel 2: FM1/FM mono)			
No.	**Symbol Name**	**Bits**	**Value**
1	* IMREG1 (8 LSBS)	8	04 HEX
2	* IMREG1 / IMREG2 (4 MSBs / 4 LSBs)	8	40 HEX
3	* IMREG2 (8 MSBs)	8	00 HEX
4	FM_Coef (5)	8	see Table 11–7.
5	FM_Coef (4)	8	
6	FM_Coef (3)	8	
7	FM_Coef (2)	8	
8	FM_Coef (1)	8	
9	FM_Coef (0)	8	
* IMREG_1/2: Two 12-bit off-set constants			

IMREG1 and IMREG2 are used to compensate for DC-offset, which are inherent to the FIR filter structure. IMREG1 is valid for the FIR_REG_1, IMREG2 for FIR_REG_2. In the Table above, IMREG1= IMREG2 = 004. Due to the partitioning to 8 bit units, the values 04hex, 40hex, and 00hex arise.

Table 11–7: 8 bit FIR-coefficients (decimal integer) for MSP 3410 B

FIR_REG_1 0001_{hex} and FIR_REG_2 0005_{hex}															
	NICAM		**FM-Terrestrial B/G, I**	**FM - Satellite** FIR filtering corresponds to a bandpass filtering with a band width of B = 130 kHz, 180 kHz, 200 kHz, ... 380 kHz  										**Auto-search or AM**
				Bandwidth (see also Table FM Volume Prescale)											
C (i)	**SC/SP/F FIR_REG1**	**UK FIR_REG1**	**German Dual FM FIR_REG1 and 2**	**130 kHz FIR_REG1 1)**	**130 kHz FIR_REG2 1)**	**180 kHz FIR_REG1**	**180 kHz FIR_REG2**	**200 kHz FIR_REG1**	**200 kHz FIR_REG2**	**280 kHz FIR_REG1**	**280 kHz FIR_REG2**	**380 kHz FIR_REG1**	**380 kHz FIR_REG2**	**500 kHz FIR_REG2**	**FIR_REG2**
0	–2	2	3	37	73	4	9	1	3	–4	–8	–1	–1	–1	75
1	–8	4	18	27	53	9	18	9	18	–4	–8	–6	–9	–1	19
2	–10	–6	27	32	64	14	28	14	27	2	4	–9	–16	–8	36
3	10	–4	48	60	119	23	47	24	48	19	36	4	5	2	35
4	50	40	66	51	101	27	55	33	66	41	78	38	65	59	39
5	86	94	72	65	127	32	64	37	72	57	107	70	123	126	40

1) The 130 kHz coefficients are based on subcarriers, which are 7 dB below an existent main carrier.

11.2.4. DCO-Increments

For a chosen TV standard a corresponding set of 24-bit increments determining the mixing frequencies of the quadrature mixers, has to be written into the IC. In Table 11–8 some examples of DCO increments are listed. It is necessary to divide them up into low part and high part. The formula for the calculation of the increments for any chosen IF-Frequency is as follows:

$$INCR_{dez} = int(f/fs \cdot 2^{24})$$

with: int = integer function
f = IF-frequency in MHz
f_S = sampling frequency (18.432 MHz)

Conversion of INCR into hex-format and separation of the 12-bit low and high parts lead to the required increments. (DCO1_HI or _LO for channel 1, DCO2_HI or LO for channel 2).

Table 11–8: DCO increments for the MSP 3410 B; frequency in MHz, increments in Hex

DCO1_LO 0093_{hex}, DCO1_HI $009B_{hex}$; DCO2_LO $00A3_{hex}$, DCO2_HI $00AB_{hex}$					
Frq. MHz	**DCO_HI**	**DCO_LO**	**Frq. MHz**	**DCO_HI**	**DCO_LO**
4.5	3E8	000			
5.04 5.5 5.58 5.7421875	460 4C6 4D8 4FC	000 38E 000 0AA	5.76 5.85 5.94	500 514 528	000 000 000
6.0 6.2 6.5 6.552	535 561 5A4 5B0	555 C71 71C 000	6.6 6.65 6.8	5BA 5C5 5E7	AAA C71 1C7
7.02	618	000	7.2	640	000
7.38	668	000	7.56	690	000

11.3. Read Registers: Listing and Addresses

The following 8-bit parameters can be read out of the RAM of the MSP 3410 B; functionally they all belong to the NICAM decoding process; their addresses are listed in Table 11–9.

All transmissions take place in 16 bit words. The valid 8 bit data are the 8 LSBs of the received data word.

To enable correct switching to NICAM sound, at least the register C_AD_BITS must be read and evaluated by the CCU. Additional data bits and CIB bits, if supplied by the NICAM transmitter, as well as information about the signal quality can be obtained by reading the remaining registers.

Table 11–9: Addresses of read registers

Read Registers	HEX
C_AD_BITS	0023
FAWCT_IST	0025
ADD_BITS	0038
CIB_BITS	003E
CONC_CT	0058

11.4. Read Registers: Functions and Values

C_AD_BITS: NICAM operation mode control bits and A[0–2] of the additional data bits.

Format:

MSB			C_AD_BITS 0023_{hex}				LSB
7	6	5	4	3	2	1	0
A[2]	A[1]	A[0]	C4	C3	C2	C1	S

Important: “S” = Bit[0] indicates correct NICAM-synchronization (S=1). If S = 0, no correct frame or sequence synchronization have been found yet and the read registers are not valid.

The operation mode is coded by C4-C1 as shown in Table 11–10.

ADD_BITS: Contains the remaining 8 of the 11 additional data bits. The additional data bits are yet not defined by the NICAM 728 system.

Format:

MSB			ADD_BITS 0038_{hex}				LSB
7	6	5	4	3	2	1	0
A[10]	A[9]	A[8]	A[7]	A[6]	A[5]	A[4]	A[3]

CIB_BITS: cib bits 1 and 2 (see NICAM 728 specifications)

Format:

MSB			CIB_BITS $003E_{hex}$				LSB
7	6	5	4	3	2	1	0
x	x	x	x	x	x	CIB1	CIB2

FAWCT_IST: The contents of this register give information on the actual position of the FAW-counter. For optimum NICAM performance, the value should be identical with or little below the value of ’FAW_SOLL’. If it reaches 0 the FP-software mutes and stops the NICAM-decoding automatically by searching for FAW synchronization once more.

CONC_CT: This register contains the actual number of bit errors of the previous 728 bit data frame. It may happen that in spite of acceptable FAWCT_IST the bit error rate result is too high for appropriate sound performance. In this case the CCU can switch to the analog FM-sound assumed to have the same program (Control bit C4).

Table 11–10: NICAM operation modes as defined by the EBU NICAM 728 specification

C4	C3	C2	C1	Operation Mode
0	0	0	0	Stereo sound (NICAMA/B), independent mono sound (FM1)
0	0	0	1	Two independent mono signals (NICAMA, FM1)
0	0	1	0	Three independent mono channels (NICAMA, NICAMB, FM1)
0	0	1	1	Data transmission only; no audio
1	0	0	0	Stereo sound (NICAMA/B), FM1 carries same channel
1	0	0	1	One mono signal (NICAMA). FM1 carries same channel as NICAMA
1	0	1	0	Two independent mono channels (NICAMA, NICAMB). FM1 carries same channel as NICAMA
1	0	1	1	Data transmission only; no audio
x	1	x	x	Unimplemented sound coding option (not yet defined by EBU NICAM 728 specification)

11.5. Sequences to Transmit Parameters and to Start Processing

After having been switched on, the MSP has to be initialized by transmitting the parameters according to the LOAD_SEQ_1/2 of Table 11–11. To make the data active, the load routine LOAD_REG_1/2 must be activated.

For NICAM operation the following steps listed in 'NICAM_START, _READ and _Check' in Table 11–11 must be taken.

For FM-stereo operation the evaluation of the identification signal must be performed. For positive identification check, the MSP 3410 B sound channels have to be switched corresponding to the detected operation mode.

Table 11–11: Sequences to initialize and start the MSP 3410 B

LOAD_SEQ_1/2: General Initialization, followed by LOAD_REG_1/2		
Write into MSP 3410 B: 0. AD_CV 1. Audio_PLL 2. FAWCT_SOLL 3. FAW_ER_TOL 4. FIR_REG_1 5. FIR_REG_2 6. MODE_REG 7. DCO1_LO 8. DCO1_HI 9. DCO2_LO 10. DCO2_HI 11. start LOAD_REG_1/2 process; FM-processing starts	 (only for NICAM mode) (only for NICAM mode)	**In the case "NICAM only" operation, the steps 9. and 10. can be skipped** **Note:** To ensure software compatibility to the MSP3400 B, before any modification of a demodulator parameter concerning an active output channel, this channel should be muted
NICAM_START: Start of the NICAM Software		
Write into MSP 3410 B: 1. Start SEARCH_NICAM Process 2. Wait at least 0.5 s		
NICAM_READ: Read NICAM specific information		
Read out of MSP 3410 B: 1. FAWCT_IST 2. C_AD_BITS 3. CONC_CT		
NICAM_CHECK: CCU checks for presence, operation mode and quality of NICAM signal		
1. Evaluation of all three parameters in the CCU (see section 11.4.) 2. If necessary, switch the corresponding sound channels within the audio processing part		
FM_IDENT_CHECK: Decoding of the identification signal		
1. Evaluation of the stereo detection register (DFP register 0018_{hex}, high part) 2. If necessary, switch the corresponding sound channels within the audio processing part		
LOAD_SEQ_1: Reinitialization of Channel 1 without affecting Channel 2, followed by LOAD_REG_1		
Write into MSP 3410 B: 1. FIR_REG_1 2. MODE_REG 3. DCO1_LO 4. DCO1_HI 5. start LOAD_REG_1 process	 (6 · 8 bit) (12 bit) (12 bit)	
PAUSE: Duration of "Pause" determines the repetition rate of the NICAM or the FM_IDENT-check		
AUDIO PROCESSING INIT: Initialization of Audio Processing Part, which may be customer dependant (see section 12.)		

11.6. Software Proposals for Multistandard TV-Sets

To familiarize the reader with the programming scheme of the MSP 3410 B demodulator part, three examples in the shape of flow diagrams are shown in the following sections.

11.6.1. Multistandard Including System B/G with NICAM/FM-Mono only

Fig. 11–1 shows a flow diagram for the CCU software, applied for the MSP 3410 B in a TV set, which facilitates NICAM and FM-mono sound. For the instructions, please refer to Table 11–11.

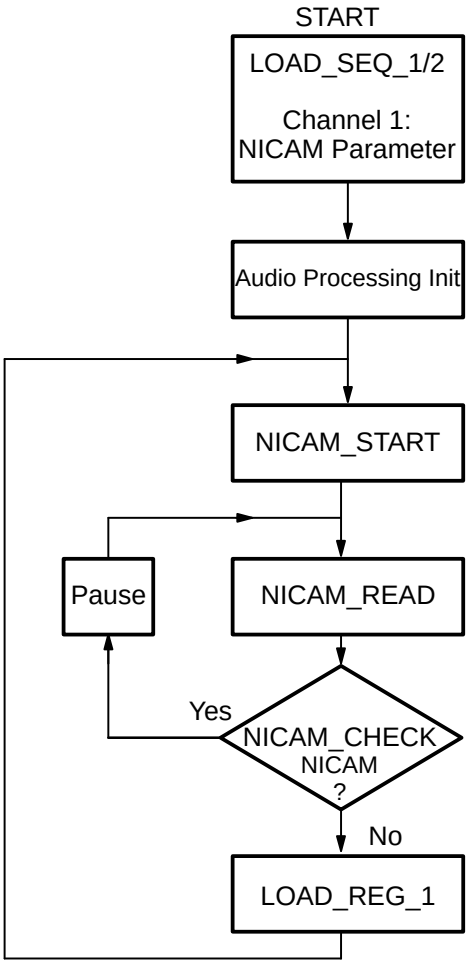


Fig. 11–1: CCU software flow diagram: Standard B/G/I NICAM/FM mono only

If the program is changed, resulting in another program within the Scandinavian System B/G no parameters of the MSP 3410 B have to be modified. To facilitate the check for NICAM the CCU has only to continue at the 'NICAM_START' instruction. During the 'NICAM_CHECK' the MSP 3410 B must be switched to the FM-mono sound.

11.6.2. Multistandard Including System I with NICAM/FM-Mono only

This case is identical to the one above. The only difference consists in selecting the UK parameters for DCO1_LO/HI, DCO2_LO/HI and FIR_REG_1.

11.6.3. Multistandard Including System B/G with NICAM/FM-Mono and German DUAL FM

Fig. 11–3 shows a flow diagram for the CCU software, applied for the MSP 3410 B in a TV set, which facilitates all standards according to System B/G. For the instructions used in the diagram, please refer to Table 11–11.

After having switched on the TV-set and having initialized the MSP 3410 B (LOAD_SEQ_1/2), FM-mono sound is available.

Fig. 11–3 shows that to check for any stereo or bilingual audio information in channel 1, its parameter should be loaded with NICAM and FM2 parameters alternately (LOAD_SEQ_1). In the case of success the MSP 3410 B has to switch to the desired audio mode.

11.6.4. Satellite Mode

Fig. 11–2 shows the simple flow diagram to be used for the MSP 3410 B in a satellite receiver. For FM-mono operation the corresponding FM carrier should preferably be processed at the MSP-channel 2.

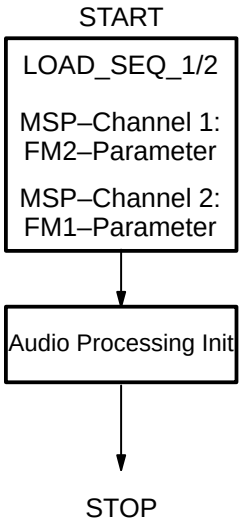


Fig. 11–2: CCU software flow diagram: SAT-mode

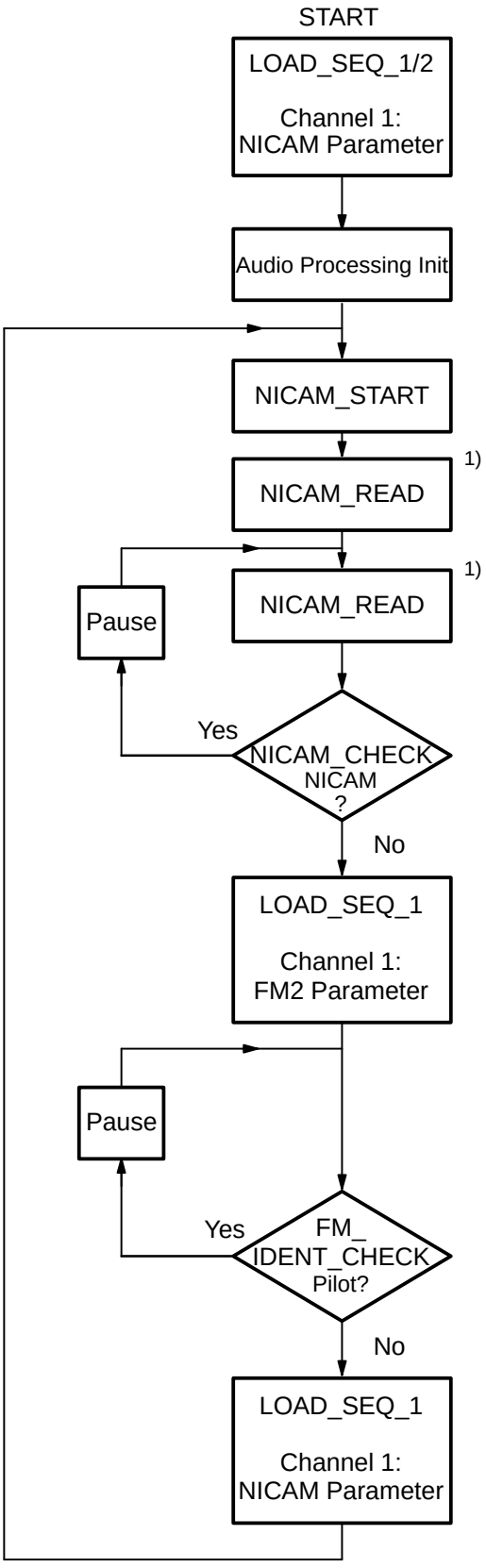


Fig. 11–3: CCU software flow diagram: Standard B/G with NICAM or FM stereo
[1)] The first READ could result in incorrect values.

11.6.5. Automatic Search Function for FM-Carrier Detection

The AM demodulation ability of the MSP 3410 B offers the possibility to calculate the “field strength” of the momentarily selected FM carrier which can be read out by the CCU. In SAT receivers this feature can be used to realize an automatic FM carrier search.

Therefore, the MSP has to be switched to AM-mode (Bit 8 of MODE_REG). The sound-IF frequency range must now be “scanned” in the MSP-channel 2 by means of the programmable quadrature mixer with an appropriate incremental frequency (i.e. 10 kHz).

After each incrementation there is a field strength value available at the DC level register FM1, which must be examined for relative maxima by the CCU. This results in either continuing search or switching the MSP back to FM demodulation mode.

During the search process the FIR_REG_2 must be loaded with the coefficient set “AUTOSEARCH”, which enables small bandwidth resulting in appropriate field strength characteristics. The absolute field strength value (can be read out of “DC Level Readout FM1”) also gives information on whether a main FM carrier or a subcarrier was detected, and as a practical consequence the FM bandwidth (FIR_REG_1/2) and the deemphasis (50 µs or adaptive) can be switched automatically. For a detailed description of the automatic search function please refer to the corresponding MUBI program.

11.6.6. Automatic Standard Detection

The AM demodulation ability of the MSP 3410 B enables also a simple method to decide between standard B/G (FM-carrier at 5.5 MHz) and standard I (FM-carrier at 6.0 MHz). It is achieved by tuning the MSP in the AM-mode to the two discrete frequencies and evaluating the field strength via the DC level register.

12. Programming the Audio Processing Part

12.1. Summary of the DSP Control Registers

Control registers are 16 bit wide. Transmissions via I^2C bus have to take place in 16 bit words. Single data entries are 8 bit. Some of the defined 16 bit words are divided into low and high byte, thus holding two different control entities.All control registers are readable.

Name	I^2C Bus Address	High/ Low	Adjustable Range, Operational Modes	Reset Mode
Volume loudspeaker channel	0000_{hex}	H	[+12 dB ... –94 dB, MUTE]	MUTE
Balance loudspeaker channel [L/R]	0001_{hex}	H	[0..100% / 100% or 100% / 0..100%]	100%/100%
Bass loudspeaker channel	0002_{hex}	H	[+12 dB ... –12 dB]	0 dB
Treble loudspeaker channel	0003_{hex}	H	[+12 dB ... –12 dB]	0 dB
Loudness loudspeaker channel	0004_{hex}	H	[0 dB ... +17 dB]	0 dB
Spatial effect loudspeaker channel	0005_{hex}	H	[OFF, ON]	OFF
Volume headphone channel	0006_{hex}	H	[+12 dB ... –77 dB, MUTE]	MUTE
Volume SCART channel	0007_{hex}	H	[00_{hex} ... $7F_{hex}$]	00_{hex}
Loudspeaker channel source	0008_{hex}	H	[FM, NICAM, SCART, SBUS12, SBUS34, I^2S]	FM
Loudspeaker channel matrix		L	[SOUNDA, SOUNDB, STEREO]	SOUNDA
Headphone channel source	0009_{hex}	H	[FM, NICAM, SCART, SBUS12, SBUS34, I^2S]	FM
Headphone channel matrix		L	[SOUNDA, SOUNDB, STEREO]	SOUNDA
SCART channel source	$000a_{hex}$	H	[FM, NICAM, SCART, SBUS12, SBUS34, I^2S]	FM
SCART channel matrix		L	[SOUNDA, SOUNDB, STEREO]	SOUNDA
I^2S channel source	$000b_{hex}$	H	[FM, NICAM, SCART, SBUS12, SBUS34, I^2S]	FM
I^2S channel matrix		L	[SOUNDA, SOUNDB, STEREO]	SOUNDA
Quasi-peak detector source	$000c_{hex}$	H	[FM, NICAM, SCART, SBUS12, SBUS34, I^2S]	FM (see note)
Prescale SCART	$000d_{hex}$	H	[00_{hex} ... $7F_{hex}$]	00_{hex}
Prescale FM	$000e_{hex}$	H	[00_{hex} ... $7F_{hex}$]	00_{hex}
FM matrix		L	[NO_MAT, GSTEREO, KSTEREO]	NO_MAT (see note)
Deemphasis FM	$000f_{hex}$	H	[OFF, 50 µs, 75 µs, J17]	50 µs
Adaptive Deemphasis FM		L	[OFF, WP1]	OFF (s. note)
Prescale NICAM	0010_{hex}	H	[00_{hex} ... $7F_{hex}$]	00_{hex}
Deemphasis NICAM	0011_{hex}	H	[OFF, J17]	J17 (s. note)
ACB Register (SCART Switches and DIG_OUT Pins)	0013_{hex}	H	Bits [7..0]	00_{hex}
Beeper	0014_{hex}	H/L	[00_{hex} ... $7F_{hex}$]/[00_{hex} ... $7F_{hex}$]	0/0 (s. note)
Identification Mode	0015_{hex}	L	[B/G, M]	B/G
Special SCART Mode	0016_{hex}		reserved for future use	–

Unused parts of the 16 bit registers must be zero.

Note: For future compatibility to new technical codes of the MSP3410 B or the MSP3400 B some coefficients concerning features not implemented or not changeable yet must nevertheless be initialized. Please consider the following compatibility restrictions:

– Quasi peak source must always be the same as the speaker source
– NICAM deemphasis switching facility not yet implemented, NICAM deemphasis must be switched on
– Panda1, if switched on, must always be activated together with 75 µs deemphasis
– Panda1 must be switched off if NICAM is selected
– FM dematrix must be switched off if Panda1 is selected
– Beeper off: set frequency to 0 and volume to 0;
– Beeper on: set frequency to 40_{hex} and set volume; beeper frequency not yet variable

Volume Loudspeaker Channel

Volume loudspeaker channel	0000_{hex}	H
+12 dB	0111 1111	$7F_{hex}$
+11 dB	0111 1110	$7E_{hex}$
+1 dB	0111 0100	74_{hex}
0 dB	0111 0011	73_{hex}
–1 dB	0111 0010	72_{hex}
–77 dB	0010 0110	26_{hex}
–94 dB	0001 0101	15_{hex}
Mute	0000 0000... 0001 0100	0 – 14_{hex}

The highest positive 8 bit number yields in a maximum possible gain of 12 dB. Decreasing the volume register by 1 LSB decreases volume by 1 dB. The minimum volume without loudness is –77 dB. Together with loudness, the volume range can be increased by the actual loudness setting. Setting loudness to 17 dB, the lowest possible volume is –94 dB. Volume settings lower than the given minimum mute the output. With large scale input signals, positive volume settings may lead to signal clipping.

To prevent severe clipping effects with bass or treble boosts, the internal volume is automatically limited to a level where in combination with either bass or treble setting the amplification does not exceed 12 dB. For example: setting bass to +9 dB and treble to +5, the maximum possible volume is +3 dB. Values higher than +3 dB are internally limited to +3 dB.

Please consider that even if the loudspeaker or the headphone or both channels are not used (i.e. satellite receiver, video recorder), they must be initialized after reset according to the tables Volume Loudspeaker Channel shown above and Volume Headphone Channel on page 28.

Balance Loudspeaker Channel

Balance loudspeaker channel [L/R]	0001_{hex}	H
Left muted, Right 100%	0111 1111	$7F_{hex}$
Left 0.8%, Right 100%	0111 1110	$7E_{hex}$
Left 99.2%, Right 100%	0000 0001	01_{hex}
Left 100%, Right 100%	0000 0000 RESET	00_{hex}
Left 100%, Right 99.2%	1111 1111	FF_{hex}
Left 100%, Right 0.8%	1000 0010	82_{hex}
Left 100%, Right muted	1000 0001	81_{hex}

Positive balance settings reduce the left channel without affecting the right channel, negative settings reduce the right channel leaving the left channel at 100%. A step by 1 LSB decreases or increases the balance by about 0.8% (exact figure: 100/127).

Bass Loudspeaker Channel

Bass loudspeaker channel	0002_{hex}	H
+12 dB	0110 0000	60_{hex}
+11 dB	0101 1000	58_{hex}
+1 dB	0000 1000	08_{hex}
0 dB	0000 0000 RESET	00_{hex}
–1 dB	1111 1000	$F8_{hex}$
–11 dB	1010 1000	$A8_{hex}$
–12 dB	1010 0000	$A0_{hex}$

With positive bass settings internal overflow may occur even with overall volume less than 0 dB. This will lead to a clipped output signal. Therefore, it is not recommended to set bass to a value that, in conjunction with volume, would result in an overall positive gain.

Treble Loudspeaker Channel

Treble loudspeaker channel	0003_{hex} H	
+12 dB	0110 0000	60_{hex}
+11 dB	0101 1000	58_{hex}
+1 dB	0000 1000	08_{hex}
0 dB	0000 0000 RESET	00_{hex}
–1 dB	1111 1000	$F8_{hex}$
–11 dB	1010 1000	$A8_{hex}$
–12 dB	1010 0000	$A0_{hex}$

With positive treble settings internal overflow may occur even with overall volume less than 0 dB. This will lead to a clipped output signal. Therefore it is not recommended to set treble to a value that in conjunction with volume would result in a overall positive gain.

Loudness Loudspeaker Channel

Loudness loudspeaker channel	0004_{hex} H	
+17 dB	0100 0100	44_{hex}
+16 dB	0100 0000	40_{hex}
+1 dB	0000 0100	04_{hex}
0 dB	0000 0000 RESET	00_{hex}

Loudness increases the volume of low and high frequency signals while keeping the amplitude of the 1 kHz reference frequency constant. The intended loudness has to be set according to the actual volume setting. Because loudness introduces gain, it is not recommended to set loudness to a value that in conjunction with volume would result in a overall positive gain.

Mode Loudness	00004_{hex} L	
Normal (constant volume at 1 kHz)	0000 0000 Reset	00_{hex}
Super Bass (constant volume at 2 kHz)	0000 0100	04_{hex}

By means of ‘Mode Loudness’, the corner frequency for bass amplification can be set to two different values. In Super Bass mode, the corner frequency is shifted up. The point of constant volume is shifted from 1 kHz to 2 kHz.

Spatial Effects Loudspeaker Channel

Spatial effect loudspeaker channel	0005_{hex} H	
OFF	0000 0000 RESET	00_{hex}
Stereo Basewidth Enlargement (SBE) or Pseudo Stereo Effect (PSE)	0011 1111	$3F_{hex}$

The kind of spatial effect depends on the source mode. If the incoming signal is in mono mode, Pseudo Stereo Effect is active, for stereo signals Stereo Basewidth Enlargement is effective.

Volume Headphone Channel

Volume Headphone Channel	0000_{hex} H	
+12 dB	0111 1111	$7F_{hex}$
+11 dB	0111 1111	$7E_{hex}$
+1 dB	0111 0100	74_{hex}
0 dB	0111 0011	73_{hex}
–1 dB	0111 0010	72_{hex}
–77 dB	0010 0110	26_{hex}
Mute	0000 0000... 0010 0101	0 – 25_{hex}

Volume SCART Channel

Volume SCART channel	0007_{hex} H	
OFF	00_{hex} RESET	
0 dB gain (digital full scale (FS) to 2 V_{RMS} output)	40_{hex}	
+6 dB gain (–6 dBFS to 2 V_{RMS} output)	$7F_{hex}$	

The highest positive 8 bit number yields in a maximum possible gain of 12 dB. Decreasing the volume register by 1 LSB decreases volume by 1 dB. The minimum volume is –77 dB. Lower volume settings mute the output. With large scale input signals, positive volume settings may lead to signal clipping.

Channel Source Modes

Loudspeaker channel source	**0008_{hex}**	**H**
Headphone channel source	**0009_{hex}**	**H**
SCART channel source	**$000a_{hex}$**	**H**
I^2S channel source	**$000b_{hex}$**	**H**
Quasi-peak detector source	**$000c_{hex}$**	**H**
FM	0000 0000 RESET	00_{hex}
NICAM[1)]	0000 0001	01_{hex}
SCART	0000 0010	02_{hex}
SBUS12	0000 0011	03_{hex}
SBUS34	0000 0100	04_{hex}
I^2S	0000 0101	05_{hex}

[1)] NICAM only possible if adaptive Deemphasis = off

Channel Matrix Modes (see also Table 4–1)

Loudspeaker channel matrix	**0008_{hex}**	**L**
Headphone channel matrix	**0009_{hex}**	**L**
SCART channel matrix	**$000a_{hex}$**	**L**
I^2S channel matrix	**$000b_{hex}$**	**L**
SOUNDA	0000 0000 RESET	00_{hex}
SOUNDB	0001 0000	10_{hex}
STEREO	0010 0000	20_{hex}

SCART Prescale

Volume Prescale SCART	**$000d_{hex}$**	**H**
OFF	00_{hex} RESET	
0 dB gain (2 V_{RMS} input to digital full scale)	19_{hex}	
+14 dB gain (400 mV_{RMS} input to digital full scale)	$7F_{hex}$	

FM Prescale

Volume Prescale FM (normal FM mode)	**$000e_{hex}$**	**H**
OFF	00_{hex} RESET	
Maximum Volume (28 kHz deviation [1)] recommended FIR-bandwidth: 130 kHz)	$7F_{hex}$	
Deviation 50 kHz[1)] recommended FIR-bandwidth: 200 kHz	48_{hex}	
Deviation 75 kHz[1)] recommended FIR-bandwidth: 200 or 280 kHz	30_{hex}	
Deviation 150 kHz[1)] recommended FIR-bandwidth: 380 kHz	18_{hex}	
Maximum deviation 192 kHz[1)] recommended FIR-bandwidth: 380 kHz	13_{hex}	
Prescale for adaptive deemphasis WP1 recommended FIR-bandwidth: 130 kHz	10_{hex}	

Volume Prescale FM (High Deviation Mode)	000e$_{hex}$	H
Deviation 150 kHz[1] recommended FIR-bandwidth: 380 kHz	0011 0000	30_{hex}
Maximum deviation 384 kHz[1] recommended FIR-bandwidth: 500 kHz	0001 0011	13_{hex}

For the **High Deviation Mode,** the FM prescaling values can be used in the range between 13_{hex} to 30_{hex}. Please consider the internal reduction of 6 dB for this mode. The FIR-bandwidth should be selected to 500 kHz.

[1] Given deviations will result in internal digital full scale signals. Appropriate clipping headroom has to be set by the customer. This can be done by decreasing the listed values by a specific factor.

FM Matrix Modes (see also Table 4–1)

FM matrix	000e$_{hex}$	L
NO MATRIX	0000 0000 RESET	00_{hex}
GSTEREO	0000 0001	01_{hex}
KSTEREO	0000 0010	02_{hex}

NO_MATRIX is used for terrestrial mono or satellite stereo sound. GSTEREO dematrixes (L+R, 2R) to (2L, 2R) and is used for German dual carrier stereo system (Standard B/G). KSTEREO dematrixes (L+R, L–R) to (2L, 2R) and is used for the Korean dual carrier stereo system (Standard M).

FM Fixed Deemphasis

Deemphasis FM	000f$_{hex}$	H
50 µs	0000 0000 RESET	00_{hex}
75 µs	0000 0001	01_{hex}
J17	0000 0100	04_{hex}
OFF	0011 1111	$3F_{hex}$

FM Adaptive Deemphasis

Adaptive Deemphasis FM	000f$_{hex}$	L
OFF	0000 0000 RESET	00_{hex}
WP1	0011 1111	$3F_{hex}$

Must be set to 'OFF' in case of NICAM or dual carrier stereo (German or Korean). If 'ON' FM fixed deemphasis must be set to 75 µs and FM matrix mode must be set to 'NO MATRIX'.

NICAM Prescale

Volume Prescale NICAM	0010$_{hex}$	H
OFF	00_{hex} RESET	
0 dB gain	20_{hex}	
+12 dB gain	$7F_{hex}$	

NICAM Deemphasis
(not yet switchable, see note in section 12.1.)

Deemphasis NICAM	0011$_{hex}$	H
J17	0000 0000 RESET	00_{hex}
OFF	0011 1111	$3F_{hex}$

ACB Register (see Fig. 4–3), Definition of the SCART-Switches and DIG_CTR_OUT Pins

ACB Register	0013_{hex}	H
DFP In Selection		
SCART1_IN	xxxx xx00	RESET
MONO_IN	xxxx xx01	
SCART2_IN	xxxx xx10	
SCART3_IN	xxxx xx11	
SCART1_OUT Selection		
SCART3_IN	xxxx 00xx	RESET
SCART2_IN	xxxx 01xx	
MONO_IN	xxxx 10xx	
DA_SCART	xxxx 11xx	
SCART2_OUT Selection		
DA_SCART	xx00 xxxx	RESET
SCART1_IN	xx01 xxxx	
MONO_IN	xx10 xxxx	
DIG_CTR_OUT1		
low	x0xx xxxx	RESET
high	x1xx xxxx	
DIG_CTR_OUT2		
low	0xxx xxxx	RESET
high	1xxx xxxx	
RESET: The RESET state is taken at the time of the first write transmission on the control bus to the audio processing part (DFP). By writing to the ACB register first, the RESET state can be redefined.		

Note: If “MONO_IN” is selected at the DFP_IN selection, the channel matrix mode of the corresponding output channel(s) must be set to “sound A”.

Beeper
(Frequency not yet variable, see note in section 12.1.)

Beeper Volume	0014_{hex}	H
OFF	0000 0000 RESET	00_{hex}
Maximum Volume (full digital scale DFS)	1111 1111	$7F_{hex}$

Beeper Frequency	0014_{hex}	L
Lowest Frequency (16 Hz)	0000 0001	01_{hex}
about 1 kHz	0100 0000	40_{hex}
Maximum Frequency (4 kHz)	1111 1111	FF_{hex}

A squarewave beeper can be added to the loudspeaker channel and the headphone channel. The addition point is just before the volume adjustment.

Identification Mode

Identification Mode	0015_{hex}	L
Standard B/G (German Stereo)	0000 0000 RESET	00_{hex}
Standard M (Korean Stereo)	0000 0001	01_{hex}
Reset of Ident-Filter	0011 1111	$3F_{hex}$

To shorten the response time of the identification algorithm after a program change between two FM-stereo capable programs, the reset of ident-filter can be applied.

Sequence:

1. Program change
2. Reset ident-filter
3. Set identification mode back to standard B/G or M
4. Wait approx. 1 sec.
5. Read stereo detection register

12.2. Exclusions

In general, all functions can be switched independently of the others. Some exceptions exist: 1. NICAM cannot be processed simultaneously to the FM2 channel. 2. If the adaptive deemphasis is activated (Reg. $000f_{hex}$ L), the NICAM channels and the identification register (0018_{hex} H) are no longer valid. The FM fixed deemphasis (Reg. $000f_{hex}$ H) must be set to 75 µs and the FM matrix mode (Reg $000e_{hex}$ H) must be set to ‘NO MATRIX’.

12.3. Summary of Readable Registers

All readable registers are 16 bit wide. Transmissions via I^2C bus have to take place in 16 bit words. Single data entries are 8 bit. Some of the defined 16 bit words are divided into low and high byte, thus holding two different control entities.

These registers are not writable.

Name	Address	High/Low	Output Range	
Stereo detection register	0018_{hex}	H	$[80_{hex} ... 7F_{hex}]$	8 bit two's complement
Quasi peak readout left	0019_{hex}	H&L	$[00_{hex} ... 7FFF_{hex}]$	16 bit binary
Quasi peak readout right	$001a_{hex}$	H&L	$[00_{hex} ... 7FFF_{hex}]$	16 bit binary
DC level readout FM1	$001b_{hex}$	H&L	$[00_{hex} ... 7FFF_{hex}]$	16 bit binary
DC level readout FM2	$001c_{hex}$	H&L	$[00_{hex} ... 7FFF_{hex}]$	16 bit binary
DFP software version[1)]	$001e_{hex}$	H	$[00_{hex} ... FF_{hex}]$	
FP software version[1)]		L	$[00_{hex} ... FF_{hex}]$	
MSP family code	$001f_{hex}$	H	$[00_{hex} ... FF_{hex}]$	
MSP hardware version[1)]		L	$[00_{hex} ... FF_{hex}]$	

[1)] Only for internal use. Subject to change without notice!

Stereo Detection Register

Stereo Detection Register	**0018_{hex} H**
Stereo Mode	Reading (two's complement)
MONO	near zero
STEREO	positive value (ideal reception: $7F_{hex}$)
BILINGUAL	negative value (ideal reception: 80_{hex})

Quasi Peak Detector

Quasi peak readout left	**0019_{hex} H+L**
Quasi peak readout right	**$001a_{hex}$ H+L**
Quasi peak readout	[0_{hex} ... $7FFF_{hex}$] values are 16 bit binary

The quasi peak readout register can be used to read out the quasi peak level of any input source, in order to adjust all inputs to the same normal listening level. The refresh rate is 32 kHz. The feature is based on a filter time constant:

attack-time: 1.3 ms
decay-time: 37 ms

DC Level Register

DC level readout FM1	**$001b_{hex}$ H+L**
DC level readout FM2	**$001c_{hex}$ H+L**
DC Level	[0_{hex} ... $7FFF_{hex}$] values are 16 bit binary

The DC level register measures the DC component of the incoming FM signals (FM1 and FM2). This can be used for seek functions in satellite receivers and for IF FM frequencies fine tuning. For further processing, the DC content of the demodulated FM signals is suppressed. The time constant τ, defining the transition time of the DC Level Register, is approximately 28 ms.

DFP Software Version

DFP software version	**$001e_{hex}$ H**
DFP software version number	[00_{hex} ... FF_{hex}]

FP Software Version

FP software version	**$001e_{hex}$ L**
FP software version number	[00_{hex} ... FF_{hex}]

MSP Family Code

MSP Family Code	**$001f_{hex}$ H**
MSP 3400 C	0000 0000
MSP 3400 B	0000 1010
MSP 3410 B	0000 1010

By means of the MSP-Family Code, the control processor is able to decide whether or not NICAM-controlling should be accomplished.

MSP Hardware Version

MSP hardware version	**$001f_{hex}$ L**
MSP technical code number (TC)[1)]	[00_{hex} ... FF_{hex}]

[1)] TC27 denotes the version F7

13. Specifications

13.1. Outline Dimensions

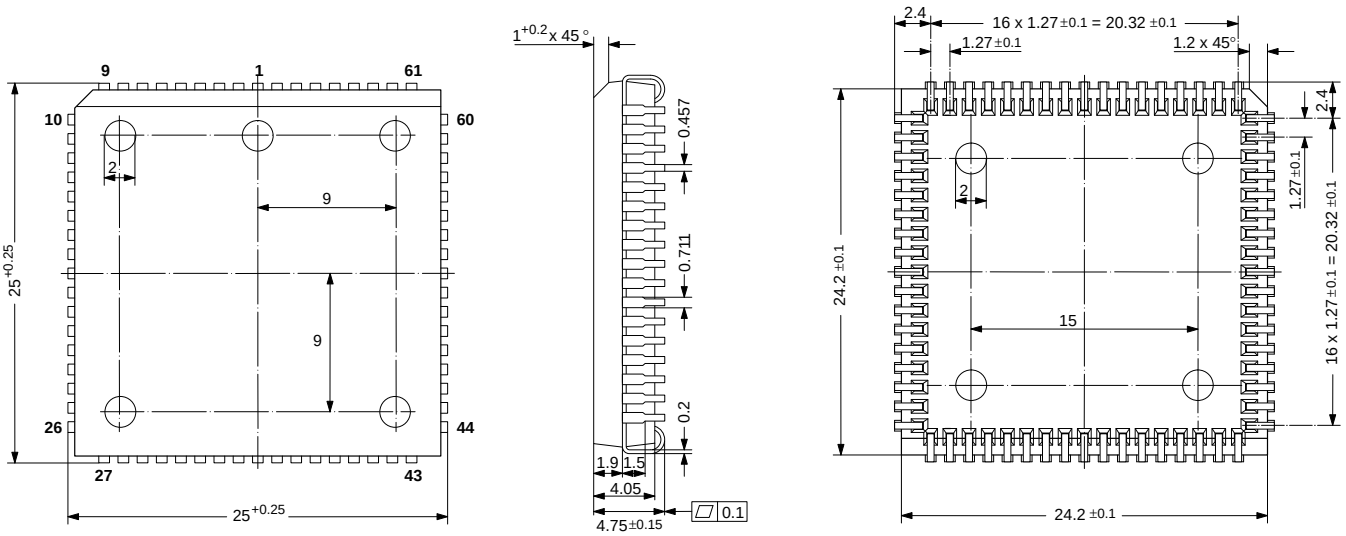


Fig. 13–1:
68-Pin Plastic Leaded Chip Carrier Package
(PLCC68)
Weight approximately 4.8 g
Dimensions in mm

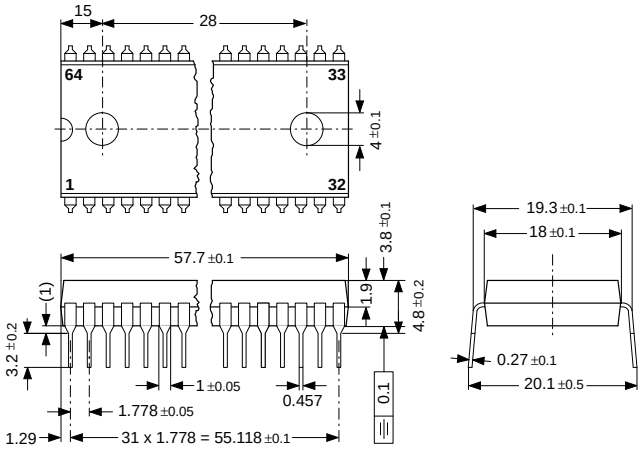


Fig. 13–2:
64-Pin Plastic Shrink Dual Inline Package
(PSDIP64)
Weight approximately 9.0 g
Dimensions in mm

13.2. Pin Connections and Descriptions

NC = not connected; leave vacant
LV = if not used, leave vacant
S.T.B. = shorted to BAGNDI if not used
DVSS: if not used, connect to DVSS
X = obligatory; connect as described in circuit diagram
AHVSS: connect to AHVSS

Pin No. PLCC 68-pin	Pin No. PSDIP 64-pin	Connection (if not used)	Pin Name	Type	Short Description
1	16	LV	S_ID	OUT	SBUS ident
2	–		NC		Not connected
3	15	LV	S_DA_IN	IN	SBUS data input
4	14	LV	I^2S_DA_IN	IN	I^2S data input
5	13	LV	I^2S_DA_OUT	OUT	I^2S data output
6	12	LV	I^2S_WS	OUT	I^2S wordstrobe
7	11	LV	I^2S_CL	OUT	I^2S clock
8	10	X	I^2C_DA	I/OUT	I^2C data
9	9	X	I^2C_CL	IN	I^2C clock
10	8	DVSS	D_CTR_IN	IN	for future use
11	7	X	STANDBYQ	IN	Standby (low-active)
12	6	X	ADR_SEL	IN	Control bus address select
13	5	LV	D_CTR_OUT0	OUT	Digital control output0
14	4	LV	D_CTR_OUT1	OUT	Digital control output1
15	3	DVSS	CW_DA	IN	Pay-TV control data
16	2	DVSS	CW_CL	IN	Pay-TV control clock
17	–		NC		Not connected
18	1	LV	AUD_CL_OUT	OUT	Audio clock output
19	64	DVSS	DMA_SYNC	IN	DMAC-sync: signal
20	63	X	XTAL_OUT	OUT	Crystal oscillator
21	62	X	XTAL_IN	IN	Crystal oscillator
22	61	X	TESTIO1	IN	Test pin 1
23	60	LV	ANA_IN2+	IN	IF input 2 (if ANA_IN1+ is used only, connect to AVSS with 50 pF Capacitor)
24	59	LV	ANA_IN–	IN	IF common
25	58	LV	ANA_IN1+	IN	IF input 1
26	57	X	AVSUP		Analog power supply +5 V
27	56	X	AVSS		Analog ground
28	55	S.T.B.	MONO_IN	IN	Mono input

Pin No. PLCC 68-pin	Pin No. PSDIP 64-pin	Connection (if not used)	Pin Name	Type	Short Description
29	54	X	VREFTOP		Reference voltage IF A/D converter
30	53	S.T.B.	SC1_IN_R	IN	Scart input1 in, right
31	52	S.T.B.	SC1_IN_L	IN	Scart input1 in, left
32	51	AHVSS	ASG1		Analog Shield Ground1
33	50	S.T.B.	SC2_IN_R	IN	Scart input2 in, right
34	49	S.T.B.	SC2_IN_L	IN	Scart input 2 in, left
35	48	AHVSS	ASG2		Analog Shield Ground2
36	47	S.T.B.	SC3_IN_R	IN	Scart input3 in, right
37	46	S.T.B.	SC3_IN_L	IN	Scart input3 in, left
38	–	AHVSS or LV	NC		Not connected
39	45	X	BAGNDI		Buffered AGNDC
40	44	X	PDMC2		Capacitor to BAGNDI
41	43	X	PDMC1		Capacitor to BAGNDI
42	42	X	AGNDC		Analog reference voltage high voltage part
43	41	X	AHVSS		Analog ground
44	40	X	CAPL_M		Volume capacitor MAIN
45	39	X	AHVSUP		Analog power supply 8.0 V
46	38	X	CAPL_A		Volume capacitor AUX
47	37	LV	SC1_OUT_L	OUT	Scart output1, left
48	36	LV	SC1_OUT_R	OUT	Scart output1, right
49	35	X	VREF1		Reference ground1 high voltage part
50	34	LV	SC2_OUT_L	OUT	Scart output 2, left
51	33	LV	SC2_OUT_R	OUT	Scart output 2, right
52	–	AHVSS	ASG3		Analog Shield Ground3
53	32	X	C_DACS_L		SCART output capacitor to ground
54	31	X	C_DACS_R		SCART output capacitor to ground
55	30	X	TESTIO2	IN	Test pin 2
56	29	LV	DACM_L	OUT	Analog output MAIN, left
57	28	LV	DACM_R	OUT	Analog output MAIN, right
58	27	X	VREF2		Reference ground2 high voltage part

Pin No.		Connection	Pin Name	Type	Short Description
PLCC 68-pin	PSDIP 64-pin	(if not used)			
59	26	LV	DACA_L	OUT	Analog output AUX, left
60	25	LV	DACA_R	OUT	Analog output AUX, right
61	24	X	RESETQ	IN	Power-on-reset
62	23	LV	N_DA	OUT	NBUS data
63	22	LV	N_CL	OUT	NBUS clock
64	21	LV	FRAME	OUT	NBUS frame
65	20	LV	S_DA_OUT	OUT	SBUS data output (FM/NICAM-test)
66	19	X	DVSS		Digital ground
67	18	X	DVSUP		Digital power supply +5 V
68	17	LV	S_CL	OUT	SBUS clock

13.3. Pin Configurations

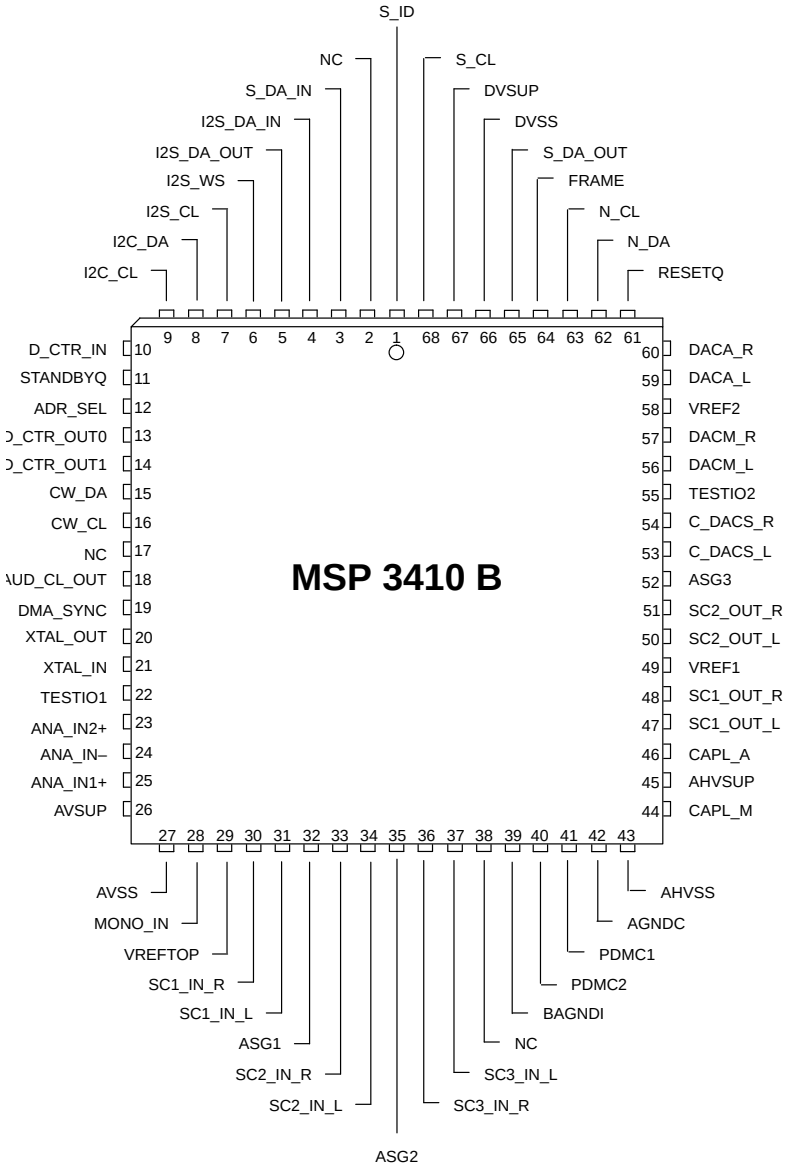


Fig. 13–3: 68-pin PLCC package

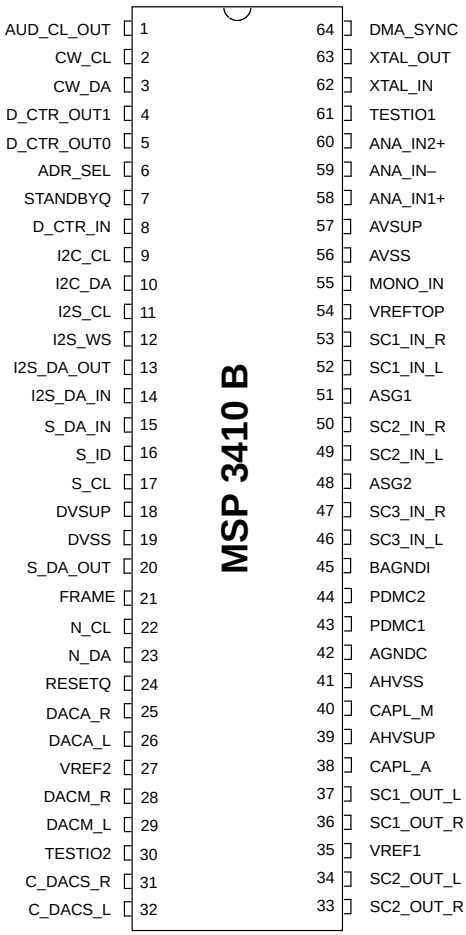


Fig. 13–4: 64-pin PSDIP package

13.4. Pin Circuits (pin numbers refer to PLCC68 package)

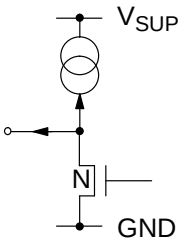


Fig. 13–5: Input Pins 3, 4 (S_DA_IN, I^2S_DA_IN)

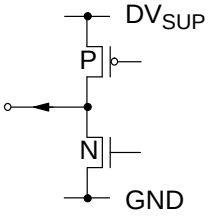


Fig. 13–6: Output Pins 1, 5, 13, 14, 64, 65, and 68 (S_ID, I^2S_DA_OUT, D_CTR_OUT0/1, FRAME, S_DA_OUT, S_CL)

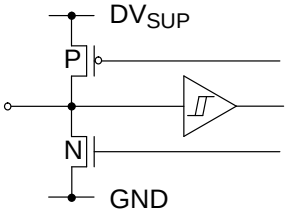


Fig. 13–7: Output Pins 6, 7, 62, and 63 (I^2S_WS, I^2S_CL, N_DA, N_CL)

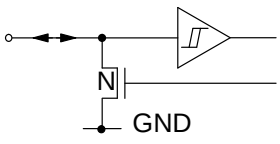


Fig. 13–8: Input/Output Pins 8 and 9 (I^2C_DA, I^2C_CL)

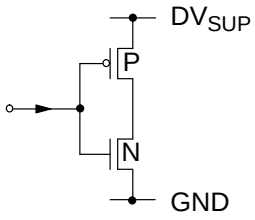


Fig. 13–9: Input Pins 10, 11, 12, 15, 16, 22, and 55 (D_CTR_IN, STANDBYQ, ADR_SEL, CW_DA, CW_CL, TESTIO1, TESTIO2)

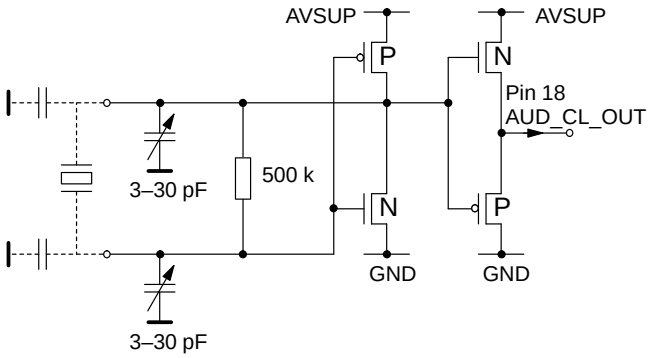


Fig. 13–10: Output Pins 18 and 20; Input Pin 21 (AUD_CL_OUT, XTALOUT; XTALIN)

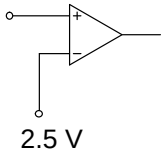


Fig. 13–11: Input Pin 19 (DMA_SYNC)

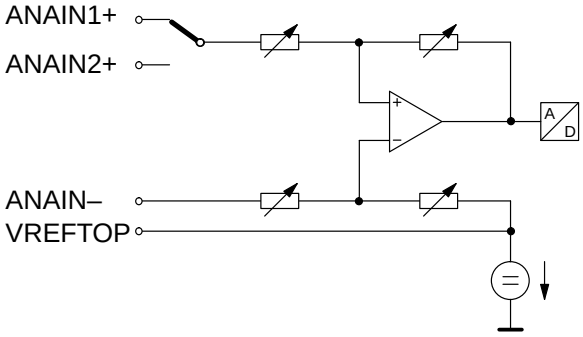


Fig. 13–12: Input Pins 23–25 and 29 (ANA_IN2+, ANA_IN–, ANA_IN1+, VREFTOP)

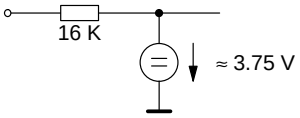


Fig. 13–13: Input Pin 28 (MONO_IN)

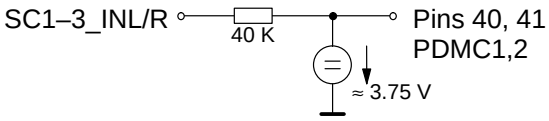


Fig. 13–14: Input Pins 30, 31, 33, 34, 36, and 37 (SC1–3_IN_L/R)

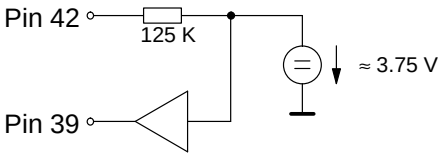


Fig. 13–15: Pins 39 and 42 (BAGNDI, AGNDC)

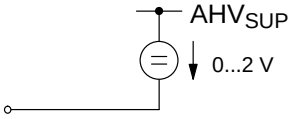


Fig. 13–16: Capacitor Pins 44 and 46 (CAPL_M, CAPL_A)

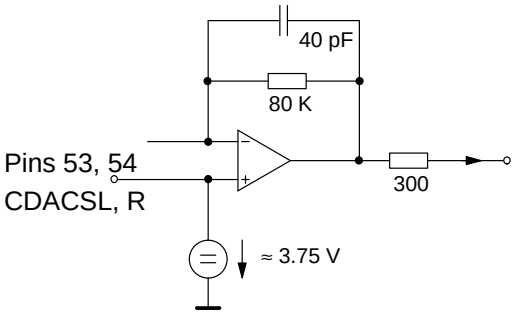


Fig. 13–17: Output Pins 47, 48, 50, 51, 53, and 54 (SC_1/2_OUT_L/R, C_DACS_L/R)

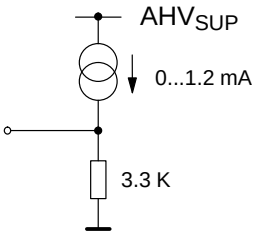


Fig. 13–18: Output Pins 56, 57, 59, and 60 (DACA_L/R, DACM_L/R)

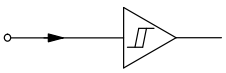


Fig. 13–19: Input Pin 61 (RESETQ)

13.5. Electrical Characteristics

13.5.1. Absolute Maximum Ratings

Symbol	Parameter	Pin Name	Min.	Max.	Unit
T_A	Ambient Operating Temperature	–	0	70	°C
T_S	Storage Temperature	–	–40	125	°C
V_{SUP1}	First Supply Voltage	AHVSUP	–0.3	9.0	V
V_{SUP2}	Second Supply Voltage	DVSUP	–0.3	6.0	V
V_{SUP3}	Third Supply Voltage	AVSUP	–0.3	6.0	V
dV_{SUP23}	Voltage between AVSUP and DVSUP	AVSUP, DVSUP	–0.5	0.5	V
P_{TOT}	Chip Power Dissipation PLCC68 without Heat Spreader PSDIP64 without Heat Spreader	AHVSUP, DVSUP, AVSUP		 1100 1300	 mW mW
V_{Idig}	Input Voltage, all Digital Inputs		–0.3	V_{SUP2}+0.3	V
I_{Idig}	Input Current, all Digital Pins	–	–20	+20	mA[1]
V_{Iana}	Input Voltage, all Analog Inputs	SCn_IN_s,[2] MONO_IN	–0.3	V_{SUP1}+0.3	V
V_{Idig}	Input Voltage, all Digital Inputs		–0.3	V_{SUP2}+0.3	V
I_{Iana}	Input Current, all Analog Inputs	SCn_IN_s,[2] MONO_IN	–5	+5	mA[1]
I_{Oana}	Output Current, all SCART Outputs	SCn_OUT_s[2]	[3], [4]	[3], [4]	
I_{Oana}	Output Current, all Analog Outputs except SCART Outputs	DACp_s[2]	[3]	[3]	
I_{Cana}	Output Current, other pins connected to capacitors	PDMCs,[2] C_DACS_s,[2] CAPL_p,[2] AGNDC, BAGNDI	[3]	[3]	

1) positive value means current flowing into the circuit
2) “n” means “1”, “2” or “3”, “s” means “L” or “R”, “p” means “M” or “A”
3) The Analog Outputs are short circuit proof with respect to First Supply Voltage and Ground.
4) Total chip power dissipation must not exceed absolute maximum rating.

Stresses beyond those listed in the “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only. Functional operation of the device at these or any other conditions beyond those indicated in the “Recommended Operating Conditions/Characteristics” of this specification is not implied. Exposure to absolute maximum ratings conditions for extended periods may affect device reliability.

13.5.2. Recommended Operating Conditions

(at T_A = 0 to 70 °C)

Symbol	Parameter	Pin Name	Min.	Nom.	Max.	Unit
V_{SUP1}	First Supply Voltage	AHVSUP	7.6	8.0	8.4	V
V_{SUP2}	Second Supply Voltage	DVSUP	4.75	5.0	5.25	V
V_{SUP3}	Third Supply Voltage	AVSUP	4.75	5.0	5.25	V
V_{REIL}	RESET Input Low Voltage	RESETQ			0.8	V
V_{REIH}	RESET Input High Voltage		2.4			V
t_{REIL}	RESET Low Time after DVSUP Stable and Oscillator Startup		5			µs
V_{DMAIL}	Sync Input Low Voltage	DMA_SYNC			a)	V
V_{DMAIH}	Sync Input High Voltage		b)			V
t_{DMA}	Sync Input Frequency			18.0		kHz
R_{DMA}	Sync Input Clock High-Level Time		500			ns
V_{DIGIL}	Digital Input Low Voltage	D_CTR_IN, CW_DA, CW_CL, STANDBYQ, ADR_SEL, TESTIO1, TESTIO2,			0.8	V
V_{DIGIH}	Digital Input High Voltage		2.4			V
t_{STBYQ1}	STANDBYQ Setup Time before Turn-off of Second Supply Voltage	STANDBYQ, DVSUP	1			µs
I^2C-Bus Recommendations						
V_{IMIL}	I^2C-BUS Input Low Voltage	I^2C_CL, I^2C_DA			1.5	V
V_{IMIH}	I^2C-BUS Input High Voltage		3.0			V
f_{IM}	I^2C-BUS Frequency	I^2C_CL			1.0	MHz
t_{I2C1}	I^2C START Condition Setup Time	I^2C_CL, I^2C_DA	120			ns
t_{I2C2}	I^2C STOP Condition Setup Time		120			ns
t_{I2C3}	I^2C-Clock Low Pulse Time	I^2C_CL	500			ns
t_{I2C4}	I^2C-Clock High Pulse Time		500			ns
t_{I2C5}	I^2C-Data Setup Time Before Rising Edge of Clock	I^2C_CL, I^2C_DA	55			ns
t_{I2C6}	I^2C-Data Hold Time after Falling Edge of Clock		55			ns
t_{I2C7}	I^2C-Slew Rate at I^2C-Clock = 1 MHz		50			V/µs

a) $\frac{DVSUP}{2} - 300\ mV$ b) $\frac{DVSUP}{2} + 300\ mV$

Symbol	Parameter	Pin Name	Min.	Nom.	Max.	Unit
I^2S-Bus Recommendations						
V_{I2SIL}	I^2S-Data Input Low Voltage	I^2S_DA_IN			0.6	V
I_{I2SIL}	I^2S-Data Input Low Current		0.9	1.7	3.2	mA
$V_{I2STRIG}$	I^2S-Data Input Trigger Voltage		0.8		1.2	V
t_{I2S1}	I^2S-Data Input Setup Time before Rising Edge of Clock	I^2S_DA_IN, I^2S_CL	20			ns
t_{I2S2}	I^2S-Data Input Hold Time after Falling Edge of Clock		0			ns
V_{I2SIDL}	I^2S-Input Low Voltage when MSP 3410 B in I2S-Slave-Mode	I^2S_CL, I^2S_WS			0.8	V
V_{I2SIDH}	I^2S-Input High Voltage when MSP 3410 B in I2S-Slave-Mode		2.4			V
f_{I2SCL}	I^2S-Clock Input Frequency when MSP 3410 B in I2S-Slave-Mode	I^2S_CL		1.024		MHz
R_{I2SCL}	I^2S-Clock Input Ratio when MSP 3410 B in I2S-Slave-Mode		0.9		1.1	MHz
f_{I2SWS}	I^2S-Wordstrobe Input Frequency when MSP 3410 B in I2S-Slave-Mode	I^2S_WS		32.0		kHz
t_{I2SWS1}	I^2S-Wordstrobe Input Setup Time before Rising Edge of Clock when MSP 3410 B in I2S-Slave-Mode	I^2S_WS, I^2S_CL	60			ns
t_{I2SWS2}	I^2S-Wordstrobe Input Hold Time after Falling Edge of Clock when MSP 3410 B in I2S-Slave-Mode		0			ns
V_{SBUSIL}	SBUS-Data Input Low Voltage	S_DA_IN			0.6	V
I_{SBUSIL}	SBUS-Data Input Low Current		0.9	1.7	3.2	mA
$V_{SBUSTRIG}$	SBUS-Data Input Trigger Voltage		0.8		1.2	V
t_{SBUS1}	SBUS-Data Input Setup Time before Rising Edge of Clock	S_DA_IN, S_CL	10			ns
t_{SBUS2}	SBUS-Data Input Hold Time after Falling Edge of Clock		0			ns

Symbol	Parameter	Pin Name	Min.	Nom.	Max.	Unit
Crystal Recommendations for **Master-Slave** Applications						
f_P	Parallel Resonance Frequency at 12 pF Load Capacitance			18.432		MHz
f_{TOL}	Accuracy of Adjustment		–20		+20	ppm
D_{TEM}	Frequency Variation versus Temperature		–20		+20	ppm
R_R	Series Resistance			8	25	Ω
C_0	Shunt (Parallel) Capacitance			6.2	7.0	pF
C_1	Motional (Dynamic) Capacitance		19	24		fF
Load Capacitance Recommendations for **Master-Slave** Applications						
C_L	External Load Capacitance[1)]	XTAL_IN, XTAL_OUT	PSDIP PLCC	3.3	1.5	pF pF
f_{CL}	Required Open Loop Clock Frequency (T_{amb} = 25 °C)		18.431		18.433	MHz
Crystal Recommendations for **FM / NICAM** Applications (No Master-Slave Mode possible)						
f_P	Parallel Resonance Frequency at 12 pF Load Capacitance			18.432		MHz
f_{TOL}	Accuracy of Adjustment		–30		+30	ppm
D_{TEM}	Frequency Variation vs Temp.		–30		+30	ppm
R_R	Series Resistance			8	25	Ω
C_0	Shunt (Parallel) Capacitance			6.2	7.0	pF
C_1	Motional (Dynamic) Capacitance		15			fF
Load Capacitance Recommendations for **FM / NICAM** Applications (No Master-Slave Mode possible)						
C_L	External Load Capacitance[1)]	XTAL_IN, XTAL_OUT	PSDIP PLCC	3.3	1.5	pF pF
f_{CL}	Required Open Loop Clock Frequency (T_{amb} = 25 °C)		18.4305		18.4335	MHz
Amplitude Recommendation for Operation with External Clock Input						
V_{XCA}	External Clock Amplitude	XTAL_IN	0.7			V_{pp}

[1)] External capacitors at each crystal pin to ground are required. They are necessary to tune the open-loop frequency of the internal PLL and to stabilize the frequency in closed-loop operation. The higher the capacitors, the lower the clock frequency results. The nominal free running frequency should match 18.432 MHz as closely as possible. Due to different layouts of customer PCBs the matching capacitor size should be defined in the application. The suggested values are figures based on experience with various PCB layouts.

Symbol	Parameter	Pin Name	Min.	Nom.	Max.	Unit
Analog Input and Output Recommendations						
C_{AGNDC}	AGNDC-Filter-Capacitor	AGNDC	–20%	3.3	+20%	µF
	Ceramic Capacitor in Parallel		–20%	100	+20%	nF
C_{PDM}	PDM-Capacitor between PDMCx and BAGNDI1 (Low Loss type, e.g. ceramic type1)	PDMC1, PDMC2, BAGNDI1	–5%	470	+5%	pF
C_{inSC}	DC-Decoupling Capacitor in front of SCART Inputs	SCn_IN_s[2)]	–20%	330	+20%	nF
V_{inSC}	SCART Input Level				2.0	V_{RMS}
V_{inMONO}	Input Level, Mono Input	MONO_IN			2.0	V_{RMS}
C_{DACS}	Filter Capacitor for SCART DACs	C_DACS_s[2)]	–10%	390	+10%	pF
R_{LSC}	SCART Load Resistance	SCn_OUT_s[2)]	10			kΩ
C_{LSC}	SCART Load Capacitance				500	pF
C_{VMA}	Main/AUX Volume Capacitor	CAPL_M, CAPL_A		10		µF
C_{FMA}	Main/AUX Filter Capacitor	DACM_s, DACA_s[2)]	–10%	1	+10%	nF

[2)] “n” means “1”, “2” or “3”, “s” means “L” or “R”, “p” means “M” or “A”

Symbol	Parameter	Pin Name	Min.	Nom.	Max.	Unit
Recommendations for Analog Sound IF Input Signal						
V_{IF}	Analog Input Range (Complete Sound IF, 0 – 9 MHz)	ANA_IN1+, ANA_IN2+, ANA_IN–	0.14	0.8	3[4]	Vpp
R_{FMNI}	Ratio: NICAM Carrier/FM Carrier (**unmodulated carriers**)[3] BG: I:		 –17 –20	 –7 –10	 0 0	 dB dB
R_{FM}	Ratio: FM-Main/FM-Sub Satellite			7		dB
$R_{FM1/FM2}$	Ratio: FM1/FM2 German FM-System			7		dB
R_{FC}	Ratio: Main FM Carrier/Color Carrier		15	–	–	dB
R_{FV}	Ratio: Main FM Carrier/Luma Components		15	–	–	dB
PR_{IF}	Passband Ripple		–	–	±2 dB	dB
SUP_{HF}	Suppression of Spectrum Above 9.0 MHz		15		–	dB
FM_{MAX}	Maximum FM-Deviation normal mode high deviation mode				 apprx ±192 apprx ±360	kHz

[3] Measuring modulated NICAM carriers, the amplitude of the highest frequency components are about 5–6 dB lower than the unmodulated carrier. The MSP 3410 B will work down to –23 dB (BG) and –25 dB (I) respectively.

[4] Under normal conditions of FM/NICAM or FM1/FM2 ratio. For signals above 1.4 Vpp, overflow of the AD converter may result. Due to the robustness of the internal processing, the IC works up to and even more than 3 Vpp, if norm conditions of FM/NICAM or FM1/FM2 ratio are supposed. In this overflow case, a loss of FM-S/N-ratio of about 10 dB may appear.

13.5.3. Characteristics

at T_A = 0 to 70 °C, f_{CLOCK} = 18.432 MHz, T_J = Junction Temperature

Symbol	Parameter	Pin Name	Min.	Typ.	Max.	Unit	Test Condition
f_{CLOCK}	Clock Input Frequency	XTAL_IN		18.432		MHz	
D_{CLOCK}	Clock High to Low Ratio		45		55	%	
t_{JITTER}	Clock Jitter (Verification not provided in Production test)				50	ps	
V_{xtalDC}	DC-Voltage Oscillator			2.5		V	
$t_{Startup}$	Oscillator Startup Time at VDD Slew-rate of 1 V/1 µs	XTAL_IN, XTAL_OUT		0.4	1.0	ms	
I_{SUP1A}	First Supply Current (active) Analog Volume for Main and Aux at 0dB Analog Volume for Main and Aux at –30dB at T_j = 27 °C	AHVSUP	 11 7.5	 15.8 11.0	 25.0 17.4	 mA mA	f = 18.432 MHz AHVSUP = 8 V DVSUP = 5 V AVSUP = 5 V
I_{SUP2A}	Second Supply Current (active)	DVSUP	100	115	150	mA	f = 18.432 MHz DVSUP = 5 V
I_{SUP3A}	Third Supply Current (active)	AVSUP		25		mA	f = 18.432 MHz AVSUP = 5 V
I_{SUP1S}	First Supply Current (standby mode) at T_j = 27 °C	AHVSUP	4.9	7.0	11.1	mA	STANDBYQ = low VSUP = 8 V
V_{APUAC}	Audio Clock Output AC Voltage	AUD_CL_OUT	1.2			V_{pp}	load = 40 pF
V_{APUDC}	Audio Clock Output DC Voltage		0.4		0.6	V_{SUP1}	I_{max} = 0.2 mA
I_{APUOL}	Audio Clock Output Low Current				–2	mA	$V_{APUDC} - V_{APUAC}$
I_{APUOH}	Audio Clock Output High Current		2			mA	$V_{APUDC} + V_{APUAC}$
f_{APU}	Audio Clock Output Frequency			18432		kHz	NICAM-mode, PLL closed
t_{APU}	Audio Clock Output Transition Time				15	ns	Load = 30 pF
V_{DCTROL}	Digital Output Low Voltage	D_CTR_OUT0 D_CTR_OUT1			0.4	V	I_{DDCTR} = 1 mA
V_{DCTROH}	Digital Output High Voltage		4.0			V	I_{DDCTR} = –1 mA
V_{NBOL}	NBUS Output Low Voltage	N_CL, N_DA. FRAME			0.4	V	I_{DDNB} = 1 mA
V_{NBOH}	NBUS Output High Voltage		4.0			V	I_{DDNB} = –1 mA
V_{IMOL}	I^2C-Data Output Low Voltage	I^2C_DA			0.4	V	I_{MOL} = 3 mA
I_{IMOL}	I^2C-Data Output High Current				1	µA	V_{IMOH} = 5 V
t_{IMOL1}	I^2C-Data Output Hold Time after Falling Edge of Clock	I^2C_DA, I^2C_CL	15			ns	
t_{IMOL2}	I^2C-Data Output Setup Time before Rising Edge of Clock		100			ns	f_{IM} = 1 MHz DVSUP = 5 V
V_{SBOL}	SBUS-Data Output Low Voltage	S_CL, S_ID, S_DA_OUT			0.4	V	I_{SBOL} = 6 mA
I_{SBOL}	SBUS-Data Output High Current				1	µA	V_{SBOH} = 5 V
f_{SB}	SBUS-Clock Frequency	S_CL		4608		kHz	DVSUP = 5 V, NICAM-PLL closed
$t_{SB1/SB2}$	SBUS-Clock High/Low-Ratio		0.9	1.0	1.1	ns	

Symbol	Parameter	Pin Name	Min.	Typ.	Max.	Unit	Test Condition
t_{SB3}	SBUS-Clock Setup Time before Ident End Pulse	S_CL, S_ID	210			ns	DVSUP = 5.25 V
t_{SB4}	SBUS-Data Setup Time before Rising Edge of Clock	S_CL, S_DA_OUT	50			ns	DVSUP = 4.75 V
t_{S5}	SBUS-Data Stable Time		120			ns	DVSUP = 5.25 V
t_{S6}	SBUS-Ident End Pulse Time	S_ID	210			ns	DVSUP = 5.25 V
V_{I2SOL}	I^2S Output Low Voltage	I^2S_WS, I^2S_CL, I^2S_DA_OUT	0.4			V	I_{I2SOL} = 2 mA
V_{I2SOH}	I^2S Output High Voltage				4.0	V	I_{I2SOH} = –2 mA
f_{I2SCL}	I^2S-Clock Output Frequency	I^2S_CL		1204		kHz	DVSUP = 5 V, NICAM-PLL closed
f_{I2SWS}	I^2S-Wordstrobe Output Frequency	I^2S_WS		32.0		kHz	DVSUP = 5 V, NICAM-PLL closed
$t_{I2S1/I2s2}$	I^2S-Clock High/Low-Ratio	I^2S_CL	0.9	1.0	1.1		
t_{I2S3}	I^2S-Data Setup Time before Rising Edge of Clock	I^2S_CL, I^2S_DA_OUT	200			ns	DVSUP = 4.75 V
t_{I2S4}	I^2S-Data Hold Time after Falling Edge of Clock		12			ns	DVSUP = 5.25 V
t_{I2S5}	I^2S-Wordstrobe Setup Time before Rising Edge of Clock	I^2S_CL, I^2S_WS	100			ns	DVSUP = 4.75 V
t_{I2S6}	I^2S-Wordstrobe Hold Time after Falling Edge of Clock		50			ns	DVSUP = 5.25 V
Analog Ground							
V_{AGNDC0}	AGNDC Open Circuit Voltage	AGNDC	3.73	3.83	3.93	V	$R_{load} \geq 10$ MΩ
dV_{BAGNDI}	Deviation of BAGNDI1 Voltage from AGNDC Voltage	BAGNDI1, AGNDC	–20		+20	mV	
$R_{outBAGN}$	BAGNDI1 Output Resistance	BAGNDI1		6		Ω	f_{signal} = 1 kHz, I = 0.1 mA
Analog Input Resistance							
R_{inSC}	SCART Input Resistance at T_j = 27 °C from T_A = 0 to 70 °C	SCn_IN_s[1]	 26 25	40	 56 61	 kΩ kΩ	f_{signal} = 1 kHz, I = 0.05 mA
R_{inMONO}	MONO Input Resistance at T_j = 27 °C from T_A = 0 to 70 °C	MONO_IN	 10.5 10	16	 23 25	 kΩ kΩ	f_{signal} = 1 kHz, I = 0.1 mA
Audio Analog-to-Digital-Converter							
V_{AICL}	Effective Analog Input Clipping Level for Analog-to-Digital-Conversion	SCn_IN_s,[1] MONO_IN	2.02	2.12	2.22	V_{RMS}	
SCART Outputs							
R_{outSC}	SCART Output Resistance at T_j = 27 °C from T_A = 0 to 70 °C	SCn_OUT_s[1]	 0.215 0.21	0.33	 0.46 0.5	 kΩ kΩ	f_{signal} = 1 kHz, I = 0.1 mA
dV_{OUTSC}	Deviation of DC-Level at SCART Output from AGNDC Voltage		–50		+50	mV	

[1] "n" means "1", "2" or "3", "s" means "L" or "R", "p" means "M" or "A"

Symbol	Parameter	Pin Name	Min.	Typ.	Max.	Unit	Test Condition
A_{SCtoSC}	Gain from Analog Input to SCART Output	SCn_IN_s[1] MONO_IN → SCn_OUT_s[1]	–1.0	0	+0.5	dB	f_{signal} = 1 kHz
$f_{rSCtoSC}$	Frequency Response from Analog Input to SCART Output bandwidth: 0 to 20000 Hz		–0.5	0	+0.5	dB	with resp. to 1 kHz
V_{outSC}	Effective Signal Level at SCART-Output during full-scale digital input signal from DSP	SCn_OUT_s[1]	1.8	1.9	2.0	V_{RMS}	f_{signal} = 1 kHz
Main and AUX Outputs							
R_{outMA}	Main/AUX Output Resistance at T_j = 27 °C from T_A = 0 to 70 °C	DACp_s[1]	2.1 2.1	3.3	4.6 5.0	kΩ kΩ	f_{signal} = 1 kHz, I = 0.1 mA
$V_{outDCMA}$	DC-Level at Main/AUX-Output for Analog Volume at 0 dB for Analog Volume at –30 dB		1.74 –	1.94 61	2.14 –	V mV	
V_{outMA}	Effective Signal Level at Main/AUX-Output during full-scale digital input signal from DSP for Analog Volume at 0 dB		1.23	1.37	1.51	V_{RMS}	f_{signal} = 1 kHz
Analog Performance							
SNR	Signal-to-Noise Ratio						
	from Analog Input to DSP	MONO_IN, SCn_IN_s[1]	82	88		dB	Input Level = –20 dB with resp. to V_{AICL}, f_{sig}=1 kHz, equally weighted 20 Hz ... 16 kHz[2]
	from Analog Input to SCART Output	MONO_IN, SCn_IN_s[1] → SCn_OUT_s[1]	93	96		dB	Input Level = –20 dB, f_{sig} = 1 kHz, equally weighted 20 Hz ... 20 kHz
	from DSP to SCART Output	SCn_OUT_s[1]	85	88		dB	Input Level = –20 dB, f_{sig} = 1 kHz, equally weighted 20 Hz ... 15 kHz[3]
	from DSP to Main/AUX-Output for Analog Volume at 0 dB for Analog Volume at –30 dB	DACp_s[1]	85 78	88 83		dB dB	Input Level = –20 dB, f_{sig} =1 kHz, equally weighted 20 Hz ... 15 kHz[3]

1) "n" means "1", "2" or "3", "s" means "L" or "R", "p" means "M" or "A"
2) DSP measured at I^2S-Output
3) DSP Input at I^2S-Input

Symbol	Parameter	Pin Name	Min.	Typ.	Max.	Unit	Test Condition
THD	Total Harmonic Distortion						
	from Analog Input to DSP	MONO_IN, SCn_IN_s[1)]			0.05	%	Input Level = –3 dBr with resp. to V_{AICL}, f_{sig} = 1 kHz, equally weighted 20 Hz ... 16 kHz[2)]
	from Analog Input to SCART Output	MONO_IN, SCn_IN_s → SCn_OUT_s[1)]		0.01	0.03	%	Input Level = –3 dBr, f_{sig} = 1 kHz, equally weighted 20 Hz ... 20 kHz
	from DSP to SCART Output	SCn_OUT_s[1)]		0.01	0.03	%	Input Level = –3 dBr, f_{sig} = 1 kHz, equally weighted 20 Hz ... 16 kHz[3)]
	from DSP to Main or AUX Output	DACA_s, DACM_s[1)]		0.01	0.03	%	Input Level = –3 dBr, f_{sig} = 1 kHz, equally weighted 20 Hz ... 16 kHz[3)]
XTALK	Crosstalk attenuation – PLCC68 – PSDIP64						Input Level = –3 dB, f_{sig} = 1 kHz, unused analog inputs connected to ground by Z < 1 kΩ
	between left and right channel within SCART Input/Output pair (L→R, R→L)						equally weighted 20 Hz ... 20 kHz
	SCn_IN → SCn_OUT[1)]	PLCC68 PSDIP64	80 80			dB dB	
	SC1_IN or SC2_IN → DSP[1)]	PLCC68 PSDIP64	80 80			dB dB	[2)]
	SC3_IN → DSP[1)]	PLCC68 PSDIP64	75 75			dB dB	
	DSP → SCn_OUT[1)]	PLCC68 PSDIP64	80 70			dB dB	[3)]
	between left and right channel within Main or AUX Output pair						equally weighted 20 Hz ... 16 kHz
	DSP → DACp[1)]	PLCC68 PSDIP64	80 75			dB dB	[3)]

1) "n" means "1", "2" or "3", "s" means "L" or "R", "p" means "M" or "A"
2) DSP measured at I^2S-Output
3) DSP Input at I^2S-Input

Symbol	Parameter	Pin Name	Min.	Typ.	Max.	Unit	Test Condition
XTALK	between SCART Input/Output pairs[1)] D = disturbing program O = observed program						(equally weighted 20 Hz ... 20 kHz) same signal source on left and right disturbing channel, effect on each observed output channel
	D: MONO/SCn_IN → SCn_OUT	PLCC68	100			dB	
	O: MONO/SCn_IN → SCn_OUT[1)]	PSDIP64	100			dB	
	D: MONO/SC1/2_IN → SCn_OUT	PLCC68	95			dB	[2)]
	O: or unsel. MONO/SCn_IN → DSP[1)]	PSDIP64	95			dB	
	D: SC3_IN → SCn_OUT	PLCC68	75			dB	[2)]
	O: or unsel. MONO/SCn_IN → DSP[1)]	PSDIP64	75			dB	
	D: MONO/SCn_IN → SC1_OUT	PLCC68	100			dB	[3)]
	O: DSP → SC2_OUT[1)]	PSDIP64	100			dB	
	D: MONO/SCn_IN → SC2_OUT	PLCC68	80			dB	[3)]
	O: DSP → SC1_OUT[1)]	PSDIP64	85			dB	
	D: MONO/SCn_IN → unselected	PLCC68	100			dB	[3)]
	O: DSP → SC1_OUT[1)]	PSDIP64	100			dB	
	Crosstalk between Main and AUX Output pairs DSP → DACp[1)]	PLCC68	95			dB	(equally weighted 20 Hz ... 16 kHz)[3)] same signal source on left and right disturbing channel, effect on each observed output channel
		PSDIP64	90			dB	
	Crosstalk from Main or AUX Output to SCART Output and vice versa D = disturbing program O = observed program						(equally weighted 20 Hz ... 20 kHz) same signal source on left and right disturbing channel, effect on each observed output channel
	D: MONO/SCn_IN/DSP → SCn_OUT	PLCC68	90			dB	SCART output load resistance 10 kΩ
	O: DSP → DACp[1)]	PSDIP64	85			dB	
	D: MONO/SCn_IN/DSP → SCn_OUT	PLCC68	95			dB	SCART output load resistance 30 kΩ
	O: DSP → DACp[1)]	PSDIP64	85			dB	
	D: DSP → DACp	PLCC68	100			dB	[3)]
	O: MONO/SCn_IN → SCn_OUT[1)]	PSDIP64	95			dB	
	D: DSP → DACM	PLCC68	83			dB	
	O: DSP → SCn_OUT[1)]	PSDIP64	74			dB	
	D: DSP → DACA	PLCC68	100			dB	
	O: DSP → SCn_OUT[1)]	PSDIP64	90			dB	

1) "n" means "1", "2" or "3", "S" means "L" or "R", "p" means "M" or "A"
2) DSP measured at I^2S-Output
3) DSP Input at I^2S-Input

Symbol	Parameter	Pin Name	Min.	Typ.	Max.	Unit	Test Condition
PSRR: rejection of noise on AHVSUP at 1 kHz							
	AGNDC BAGNDI	AGNDC BAGNDI		80 80		dB dB	
	From Analog Input to DSP	MONO_IN, SCn_IN_s[1)]		69		dB	
	From Analog Input to SCART Output	MONO_IN, SCn_IN_s[1)] SCn_OUT_s[1)]		77		dB	
	From DSP to SCART Output	SCn_OUT_s[1)]		67		dB	
	From DSP to MAIN/AUX Output	DACp_s[1)]		71		dB	
S/N_{FM}	FM Input to Main/AUX/SCART Output	DACp_s, SCn_OUT_s[1)]	70		–	dB	1 FM-carrier 5.5 MHz, 50 µs, 1 kHz, 40 kHz deviation; RMS, unweighted 0 to 15 kHz; full input range
S/N_{NICAM}	Signal to Noise ratio of NICAM baseband signal on Main/AUX/ SCART outputs	DACp_s, SCn_OUT_s[1)]	TBD		–	dB	
S/N_{D2MAC}	Signal to Noise ratio of D2MAC baseband signal on Main/AUX/ SCART outputs	DACp_s, SCn_OUT_s[1)]	TBD		–	dB	
THD_{FM}	Total Harmonic Distortion + Noise of FM demodulated signal on Main/AUX/SCART output	DACp_s, SCn_OUT_s[1)]	–		0.3	%	1 FM-carrier 5.5 MHz, 1 kHz, 50 µs; 40 kHz deviation; full input range
THD_{NICAM}	Total Harmonic Distortion + Noise of NICAM baseband signal on Main/AUX/SCART output	DACp_s, SCn_OUT_s[1)]	–	0.01	0.1	%	2.12 kHz, Modulator input level = 0 dBref
THD_{D2MAC}	Total Harmonic Distortion + Noise of D2MAC baseband signal for Main/AUX/SCART output	DACp_s, SCn_OUT_s[1)]	–	0.01	0.1	%	2.12 kHz, Modulator input level = 0 dBref
BER_{NI}	NICAM: Bit Error Rate	–	–	–	10^{-7}	/s	FM+NICAM, norm conditions
R_{IFIN}	Input Impedance	ANA_IN1+, ANA_IN2+, ANA_IN–	1.2 6.0	2.0 9.1	3.1 13.8	kOhm kOhm	Gain AGC = 20 dB Gain AGC = 3 dB
$DC_{VREFTOP}$	DC voltage at VREFTOP	VREFTOP	–	2.67	–	V	$V_{SUPANALOG}$ = 5 V
DC_{ANA_IN+}	DC voltage on active IF input	ANA_IN1+, ANA_IN2+	–	1.5	–	V	$V_{SUPANALOG}$ = 5 V
DC_{ANA_IN-}	DC voltage on common IF input	ANA_IN–	–	1.5	–	V	$V_{SUPANALOG}$ = 5 V
dV_{FMOUT}	Tolerance of output voltage of FM demodulated signal	DACp_s, SCn_OUT_s[1)]	–1.5		+1.5	dB	1 FM-carrier, 50 µs, 1 kHz 40 kHz deviation; RMS
$dV_{NICAMOUT}$	Tolerance of output voltage of NICAM baseband signal	DACp_s, SCn_OUT_s[1)]	–1.5		+1.5	dB	2.12 kHz, Modulator input level = 0 dBref
$dV_{D2MACOUT}$	Tolerance of output voltage of D2MAC baseband signal	DACp_s, SCn_OUT_s[1)]	–1.5		+1.5	dB	2.12 kHz, Modulator input level = 0 dBref
fR_{FM}	FM Frequency Response on Main/ AUX/SCART Outputs, Bandwidth 20 to 15000 Hz	DACp_s, SCn_OUT_s[1)]	–1.0		+1.0	dB	1 FM-carrier 5.5 MHz, 50 µs, Modulator input level = –14.6 dBref; RMS

1) “n” means “1”, “2” or “3”, “s” means “L” or “R”, “p” means “M” or “A”

Symbol	Parameter	Pin Name	Min.	Typ.	Max.	Unit	Test Condition
fR_{NICAM}	NICAM Frequency Response on Main/AUX/SCART Outputs, Bandwidth 20 to 15000 Hz	DACp_s, SCn_OUT_s[1)]	–1.0		+1.0	dB	Modulator input level = –12 dB dBref; RMS
fR_{D2MAC}	D2MAC Frequency Response on Main/AUX/SCART Outputs, Bandwidth 20 to 15000 Hz	DACp_s, SCn_OUT_s[1)]	–1.0		+1.0	dB	Modulator input level = –12 dB dBref; RMS
SEP_{FM}	FM Channel Separation (Stereo)	DACp_s, SCn_OUT_s[1)]	50			dB	2 FM-carriers 5.5/5.74 MHz, 50 µs, 1 kHz, 40 kHz deviation; RMS
SEP_{NICAM}	NICAM Channel Separation (Stereo)	DACp_s, SCn_OUT_s[1)]	80			dB	
SEP_{D2MAC}	D2MAC Channel Separation (Stereo)	DACp_s, SCn_OUT_s[1)]	80			dB	
$XTALK_{FM}$	FM Crosstalk Attenuation (Dual)	DACp_s, SCn_OUT_s[1)]	80			dB	2 FM-carriers 5.5/5.74 MHz, 50 µs, 1 kHz, 40 kHz deviation; RMS
$XTALK-_{NICAM}$	NICAM Crosstalk Attenuation (Dual)	DACp_s, SCn_OUT_s[1)]	80			dB	
$XTALK-_{D2MAC}$	D2MAC Crosstalk Attenuation (Dual)	DACp_s, SCn_OUT_s[1)]	80			dB	

1) “n” means “1”, “2” or “3”, “s” means “L” or “R”, “p” means “M” or “A”

14. Timing Diagrams

14.1. Power-up Sequence

The reset should not reach high level before the oscillator has started. This requires a reset delay of > 1 ms (see Fig.14–1).

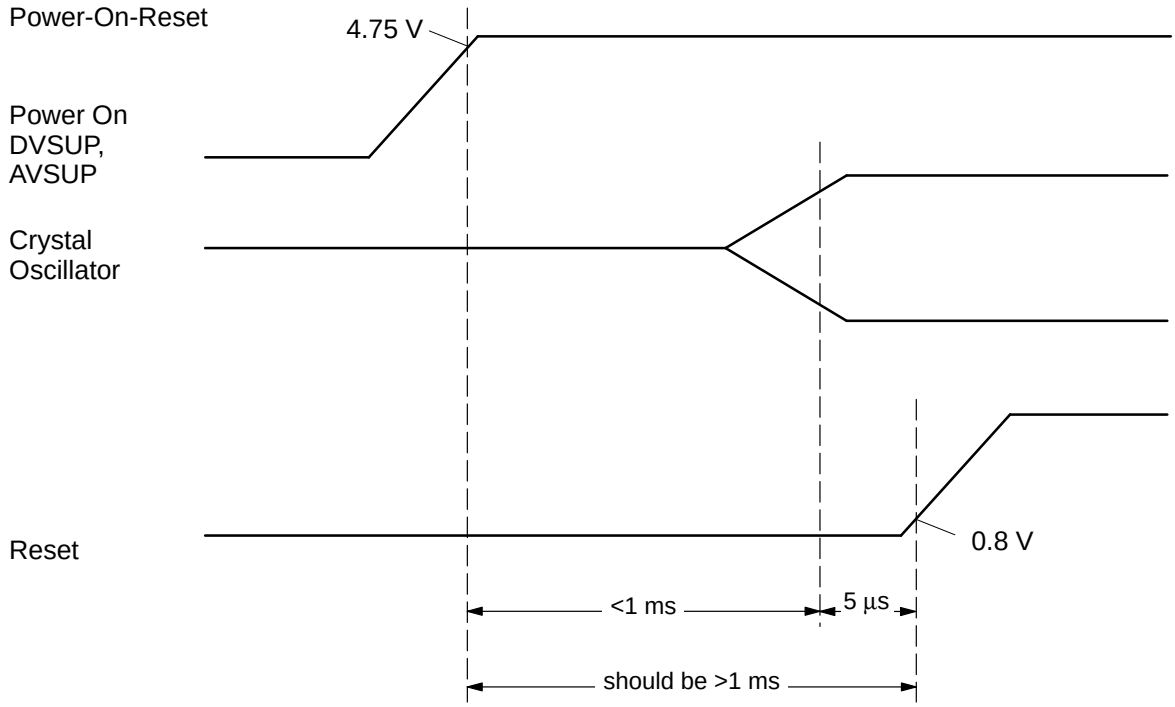


Fig. 14–1: Power-up sequence

14.2. I²C Bus Timing Diagram

(Data: MSB first)

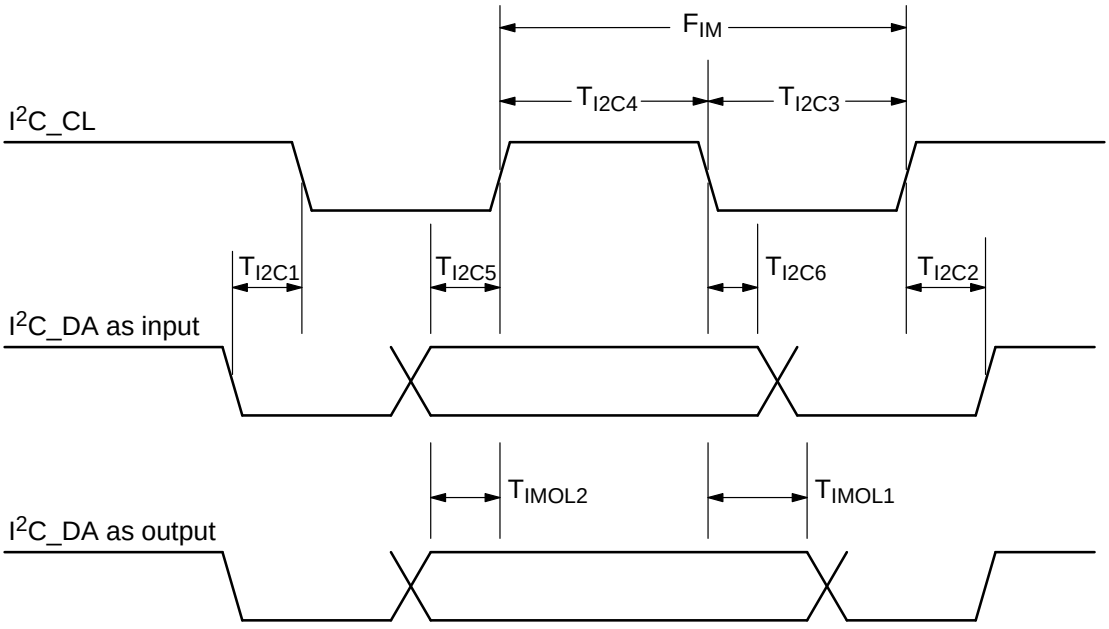
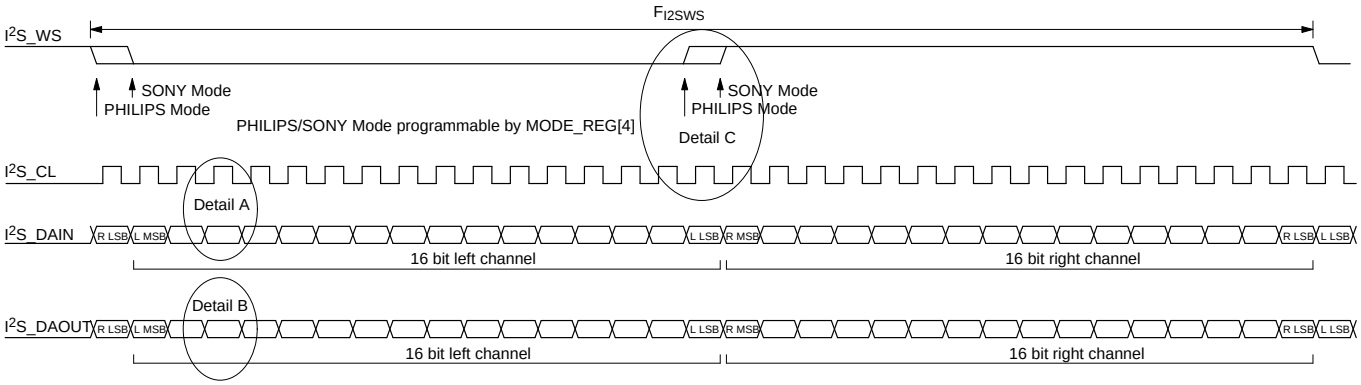


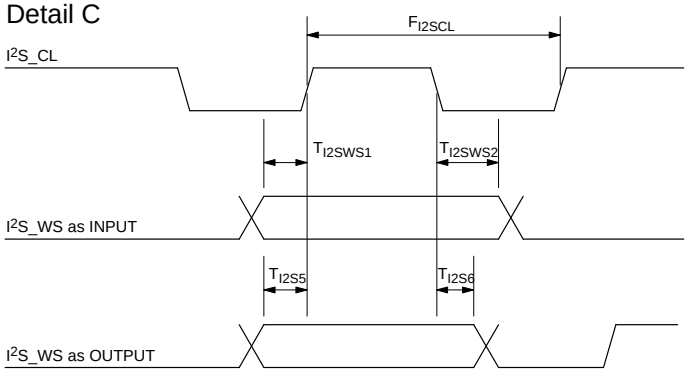
Fig. 14–2: I²C bus timing diagram

14.3. I²S Bus Timing Diagram

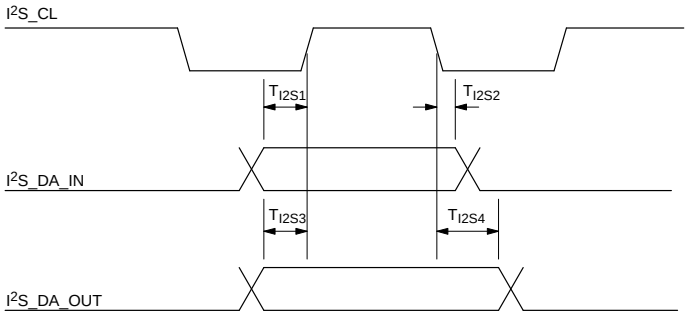
(Data: MSB first)



Detail C

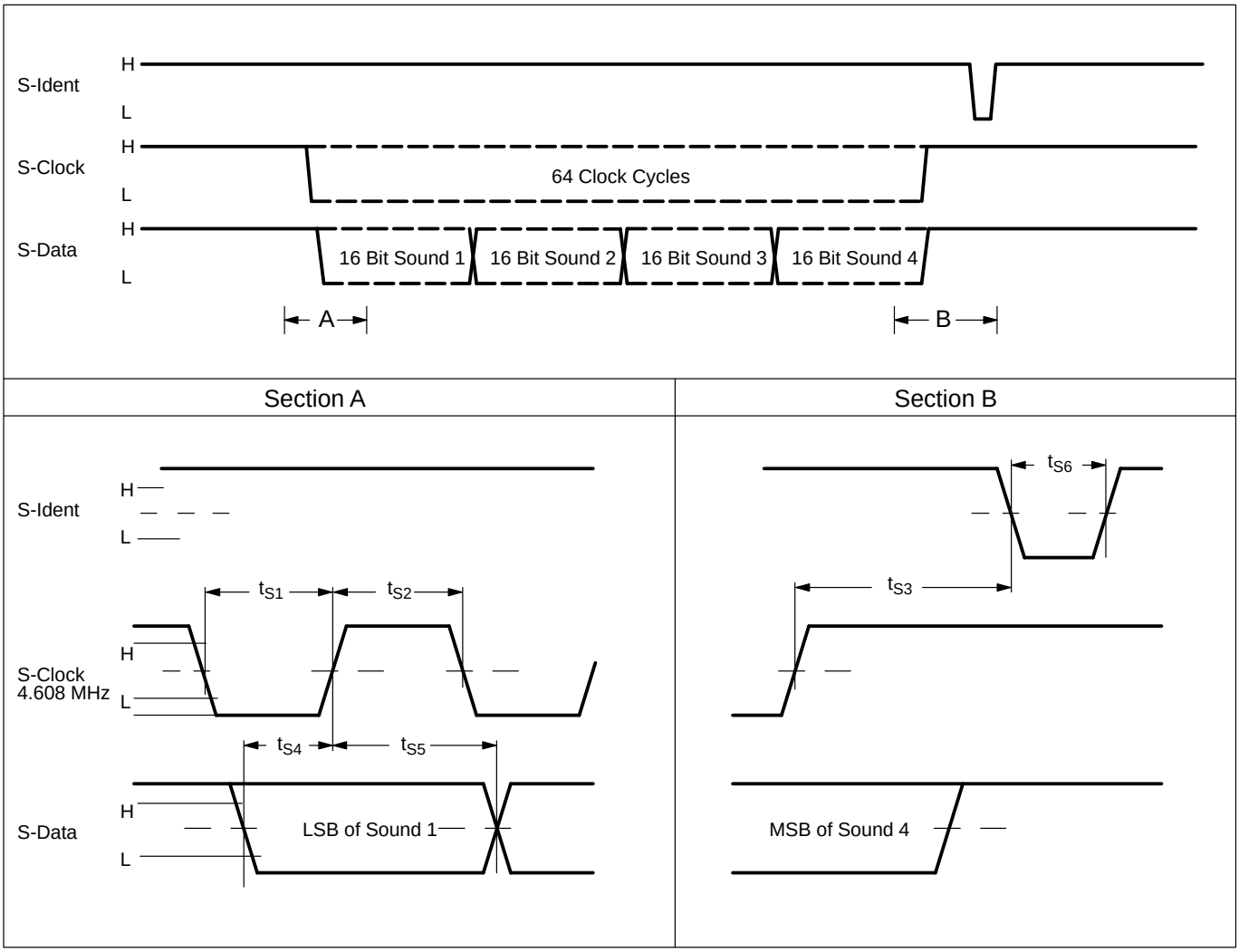


Detail A,B

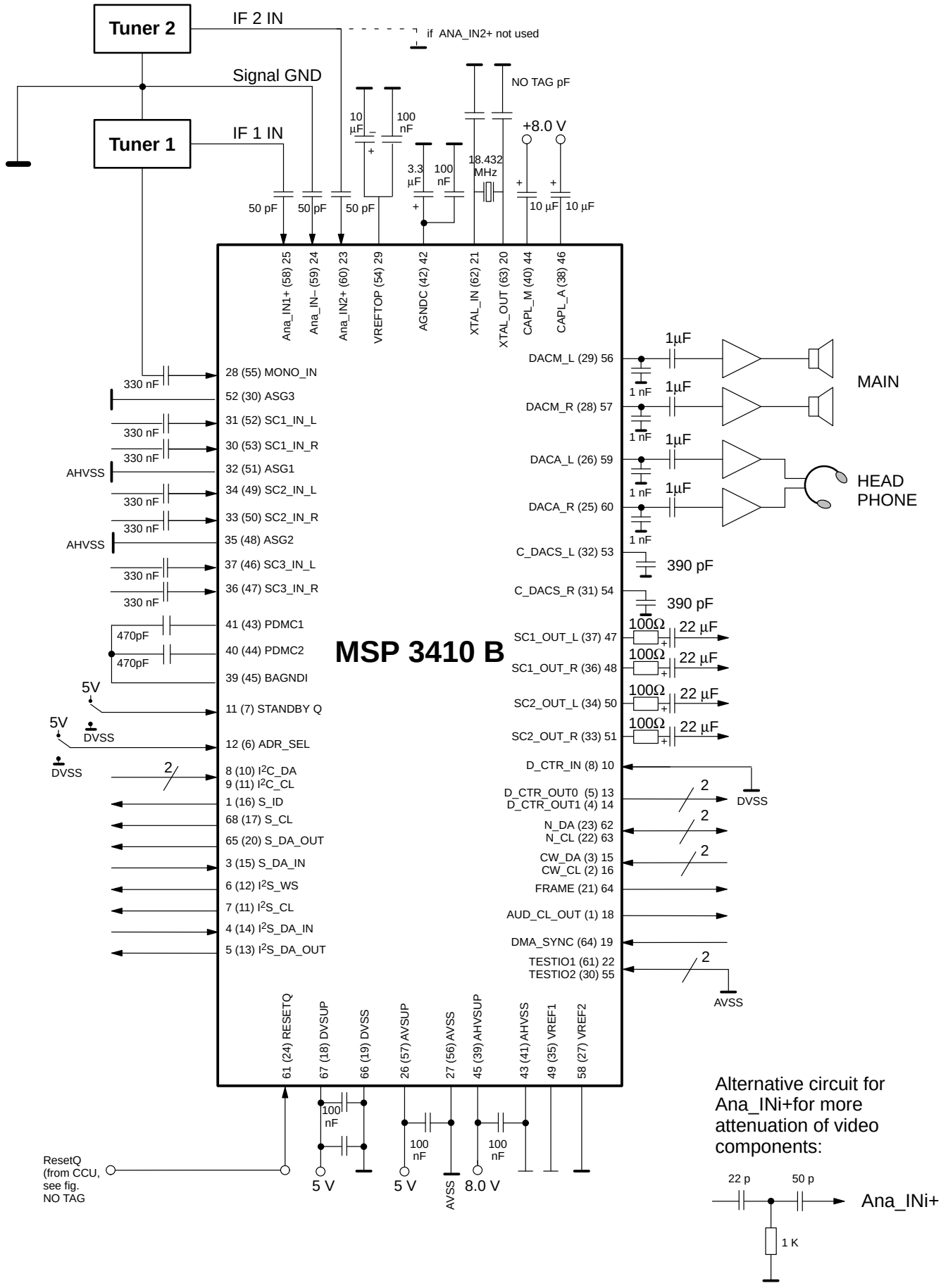


14.4. SBUS Timing Diagram

(Data: LSB first)



15. Application Circuit



16. DMA Application

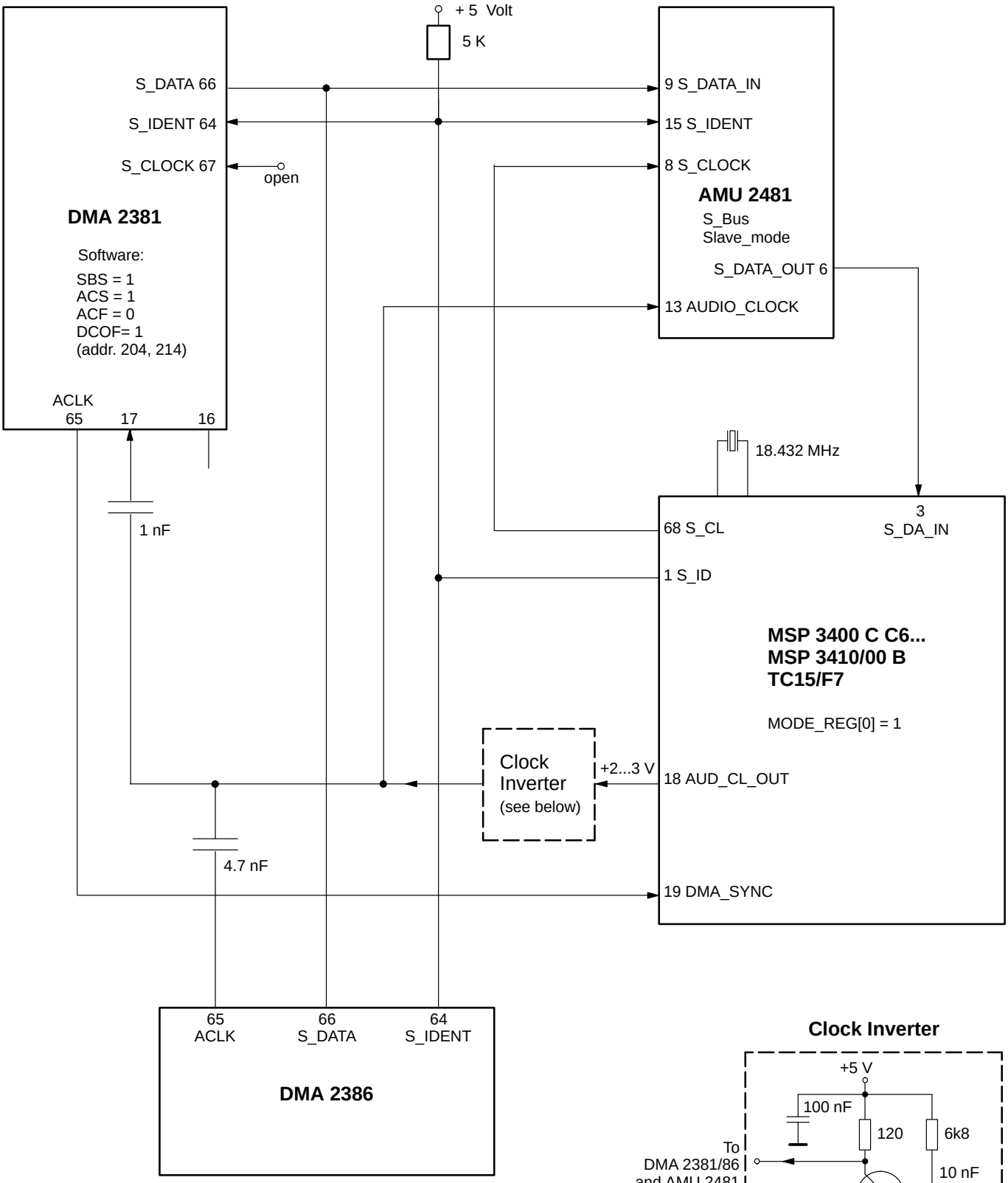


Fig. 16–1: DMA application with MSP 3410 TC15 or F7

Note: Pin numbers refer to PLCC packages for DMA 2381 and MSP3410, and to PSDIP package for AMU 2481.

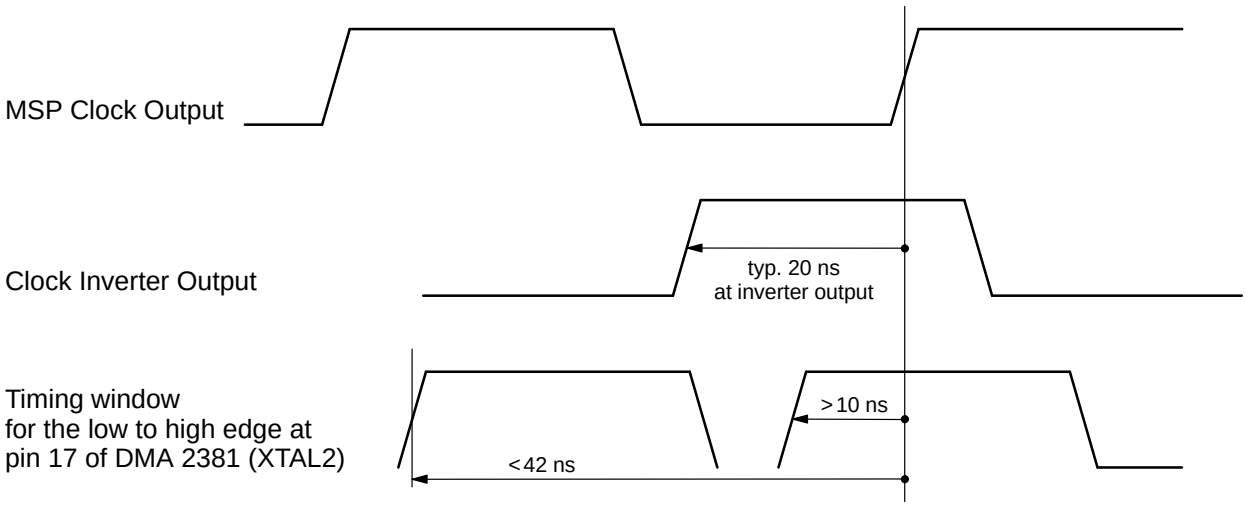


Fig. 16–2: Timing requirements for the clock signal at the DMA 2381 clock input

In the following table, the input/output clock-specification of the D2MAC circuit is shown.

Table 16–1: Clock input and output specification for MSPs

	MSP 3400 C –C6 new Version	**MSP 3410/00B –F7** new Version	**MSP 3410/00B TC15** actual Version
XTAL_IN min (minimum amplitude) C input (after Reset)	>0.7 Vpp 22 pF	>0.7 Vpp 22 pF	>0.7 Vpp 31 pF
AUD_CL_OUT min with C load **Rout (HF) typ.**	>1.2 Vpp 40 pF 150 Ω	>1.2 Vpp 40 pF 120 Ω	>1.0 Vpp 43 pF 120 Ω

Table 16–2: Clock input and output specification for ICs connected to MSP

	DMA 2381	**DMA 2386**	**AMU2481**
XTAL_IN min **Clock-in min** (minimal amplitude) C input	>0.7 Vpp 24 pF 10 pF with: Adr. 204,14=1	>0.7 Vpp 7pF	>0.7 Vpp 7pF

For the DMA_SYNC input specification of the MSP, please refer to page 42 “V_{DMAIL}, V_{DMAIH}.”

17. I²S Bus in Master/Slave Configuration with Standby Mode

In a master/slave application, both MSP, after power up and reset, will start as master by default. This means that before the slave MSP is set to slave-mode, relatively large current-pulses (~20 mA) in the I2S_CL and I2S_WS lines can cause some crackling noise during startup time, if the the MSP is demuted before the slave MSP is set to slave mode.

These high current pulses are also possible, if the active I2S_CL and I2S_WS outputs of the master MSP are clipped by the correspondent inputs of the slave MSP, which is switched to standby mode.

To avoid this, it is recommended, that the I2S-bus lines I2S_CL and I2S_WS are current-limited to about 5 mA with series resistors of about 390 Ω (330...470 Ω).

Fig. 17–1 depicts the recommended application circuit for two MSP 3410/00B or MSP 3400 C, which are connected via I2S Bus in a master/slave configuration, and where the slave MSP can be switched in standby mode (+5 Volt power is switched off).

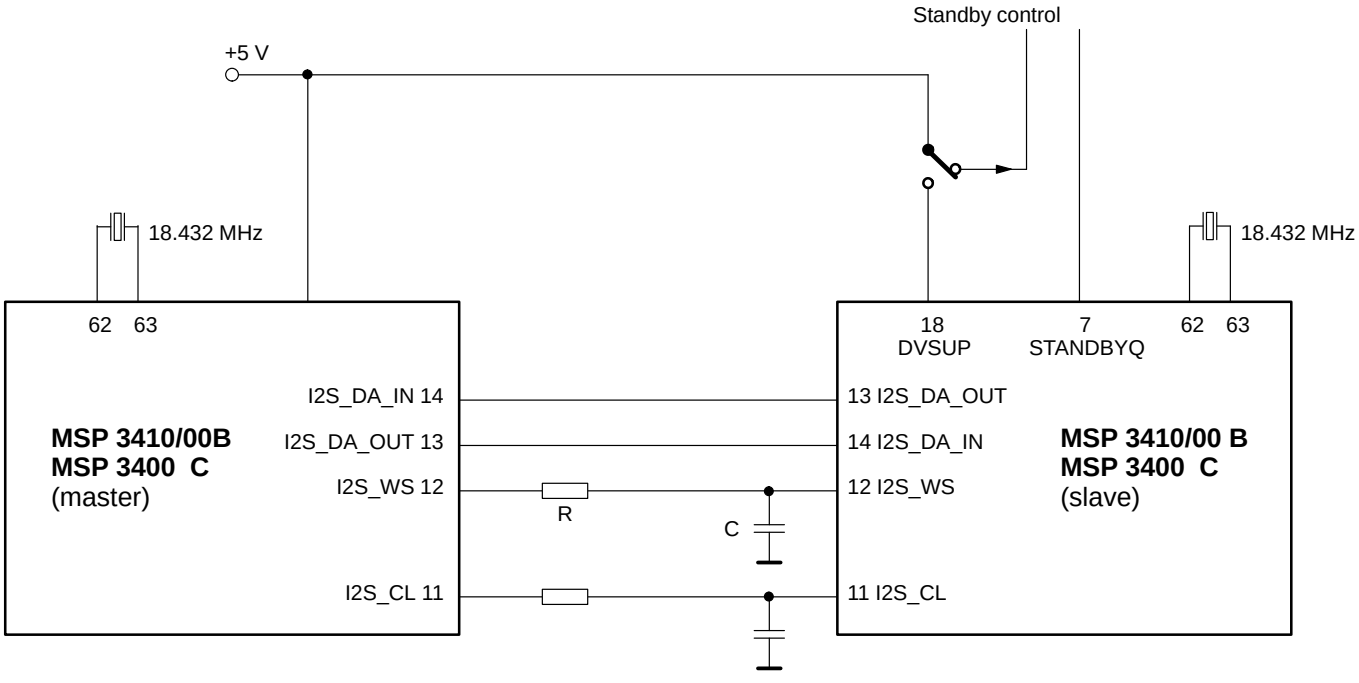


Fig. 17–1: I²S master/slave application

18. APPENDIX A: MSP 3410/3400 B Technical Code History

TC01

First hardware release with basic software for TV sets. Date: December 1992. Missing software features: Identification, spatial effects, DC level readout, adaptive Deemphasis, D2MAC processing, full feature volume control, quasi peak detector, balance, loudness, beeper.

Bug list:

1. no NICAM-synchronisation with digital test signals
2. Error in the d/a-converter; this fault is notable with full scale output signals.
3. insufficient THD quality of the Main a. Aux outputs
4. Software reset has no effect to the FP.
5. I^2C-Bus: DFP-RAM-Address '6' causes troubles: The problem preliminary can be solved by means of a trick in the control program.

TC02

Emulator version of TC01.

TC03

Hardware as in TC01 with additional software features: Identification, spatial effects, DC level readout, adaptive Deemphasis (first release with bugs).

TC04

Second hardware release with new pinning (given in this document), new I^2C bus protocol and completed software for basic TV receivers. Date: June 1993. Missing features to full spec: adaptive Deemphasis, D2MAC processing.

TC05

Reserved technical code for emulator version of TC04.

TC06

Same hardware version as TC04 but with basic software for satellite applications (D2MAC and Wegener). Missing features: Identification, spatial effects, MQ oversampling switchable, full feature volume control, quasi peak detector, balance, loudness, bass, treble, NICAM, beeper (see diagram below).

Note: TC04 and TC06 unfortunately show a number of failures. For a detailed list, together with application notes, see separate document.

TC07

Emulator version for software development.

TC08

Hardware and software of TC04 with aluminium corrections.

TC09

Satellite version based on TC06 without I^2C-Bus problem and startup-problem of TC06.

TC10

Projected final hardware. Software completed, but without D2MAC.

TC12

1. As TC10, but without start-up problem.
2. I^2S slave mode not working
3. High deviation mode switchable by 'HDEV' = 1 **and** 'FM1FM2' = 0

TC13

Emulator version for software development.

TC14

Alternative I^2C Device Address (84/85), new bass/treble characteristics, new carrier mute algorithm (not working properly yet), switchable AUDIO_CLOCK_OUT.

TC15

New features:

1. High deviation mode ok
2. Open loop frequency of crystal oscillator is approx. 0.5 kHz higher.
3. FM-carrier mute improved
4. Various internal modifications to minimize radiation problems
5. Slightly modified loudness characteristic
6. Reset facility for identification filters
7. Beeper no longer effected by loudness
8. Beeper gain reduced by 6 dB
9. Volume-main effects beeper in 1 dB steps
10. I^2S slave mode o.k.

Known restrictions:

1. I^2C bus problem for multibus systems (see Appendix C). This problem was resident in all technical codes before.
2. I^2C-problem concerning Time_Out_Enable: This bit should not be set and will have no function for future technical codes.
3. Mute positions for volume of loudspeaker and headphone channels are to be modified.

F7

1. DFP-part now controllable before having loaded any demodulator parameters.

2. switchable loudness characteristic

3. Nicam-processing: overload level increased by 6 dB

4. I^2C-bus:
   – Time-out bit CONTROL[14] is cancelled and must be set to 0.
   – I^2C-clock will no longer be pulled down for more than 1 ms in the non-error condition.
   – I^2C-error condition is now indicated by NAKs after a 7 ms low period of the I^2C-clock.
   – I^2C-bus problem for multibus systems is solved.

5. Oscillator: modified crystal specs

6. Various minor changes to reduce radiation, i.e. SBUS can be switched to tristate by means of MODE_REG[11], modified clock buffer, and decoupling capacities on-chip.

7. Audio_Clock_Output AC voltage 1.0 $\rightarrow$ 1.2 V_{pp}

19. APPENDIX B: Documentation History

19.1. MSP 3410

1. Data sheet “MSP 3410 Multistandard Sound Processor Preliminary” version 0.0, April 1993, 6251-366-1PD: First preliminary release of the data sheet.

2. Data sheet “MSP 3410 Multistandard Sound Processor Preliminary” version 0.1, June 1993, 6251-366-2PD: Second preliminary release of the data sheet. Major changes:

– definition of standby mode

– definition of the DSP software features of TC04

– correction of I^2C read operation

– new chapter S-Bus interface

– new chapter I^2S-Bus interface

– new definition of volume, balance, loudness and beeper control registers

– some changes in the specification chapter

– timing diagrams of I^2C, I^2S, and S-BUS

– application diagram for D2MAC operations

– changes in the application diagram: use of 50 pF caps for IF inputs, pins STANDBYQ, ADR_SEL and D_CTR_IN0 should not be left open.

3. Data sheet “MSP 3410 Multistandard Sound Processor Preliminary” version 0.2, September 1993, 6251-366-3PD: Third preliminary release of the data sheet. Major changes:

– high deviation FM mode

– compatibility restrictions regarding future Technical Codes and MSP3400

– new I^2C-Bus alternative address

– complemented application circuit

4. Data sheet “MSP 3410 Multistandard Sound Processor Preliminary” version 0.3, January 19, 1994, 6251-366-4PD: Fourth preliminary release of the data sheet. Major changes:

– Table 10–1: Recommended channel assignments for demodulator and audio processing part

5. Data sheet “MSP 3410 Multistandard Sound Processor Preliminary” version 0.4, February 15, 1994, 6251-366-5PD: Fifth preliminary release of the data sheet. No major changes. Changes have been made to improve comprehension.

19.2. MSP 3410 and MSP 3400

With this release of the data sheet, two versions are available: The MSP 3410 and the MSP 3400 version.

1. Data sheet “MSP 3410 Multistandard Sound Processor Preliminary” version 0.5, April 12, 1994, 6251-366-6PD: Sixth preliminary release of the data sheet and data sheet “MSP 3400 Multistandard Sound Processor Preliminary” March 28, 1994, 6251-378-1PD: First preliminary release of the data sheet.

Major changes:

– D2MAC registers 12hex and 20hex–2fhex no longer supported.

– New recommendation for FM prescale for adaptive deemphasis.

– Appendix C: Documentation of known hardware restrictions.

– Table 3–3: “Summary of NICAM 728 sound modulation paramters”: Specification for France inserted.

– Table 4–1: “Some examples for recommended channel assignments for demodulator and audio processing part”: New modes inserted.

2. Data sheet “MSP 3410 Multistandard Sound Processor Preliminary” version 0.6, July 12, 1994, 6251-366-7PD: Seventh preliminary release of the data sheet and data sheet “MSP 3400 Multistandard Sound Processor Preliminary” July 12, 1994, 6251-378-2PD: Second preliminary release of the data sheet.

– new volume table for loudspeaker and headphone channel

– new I^2C-Bus failure mode

– modified crystal specs

3. Data sheet “MSP 3410 Multistandard Sound Processor Preliminary” version 0.7, Oct. 6, 1995, 6251-366-8PD: Eighth preliminary release of the data sheet and data sheet “MSP 3400 Multistandard Sound Processor Preliminary”, Oct. 6 1995, 6251-378-3PD: Third preliminary release of the data sheet.

– switchable loudness characteristic

– oscillator: modified crystal specs

– section 13.4.: pin circuits new

– new circuit recommendations for MSP-DMA applications

19.3. MSP 3410 B and MSP 3400 B

With this release of the data sheet, two versions are available: The MSP 3410 **B** and the MSP 3400 **B** version.

1. Data sheet “MSP 3410 B Multistandard Sound Processor Preliminary” version 0.8, Nov. 20, 1995, 6251-366-9PD: Ninth preliminary release of the data sheet and data sheet “MSP 3400 B Multistandard Sound Processor Preliminary”, Nov. 20, 1995, 6251-378-4PD: Fourth preliminary release of the data sheet. Major changes:

– Fig. 13–1: PLCC68 package dimensions changed

– Fig. 13–2: PSDIP64 package dimensions changed

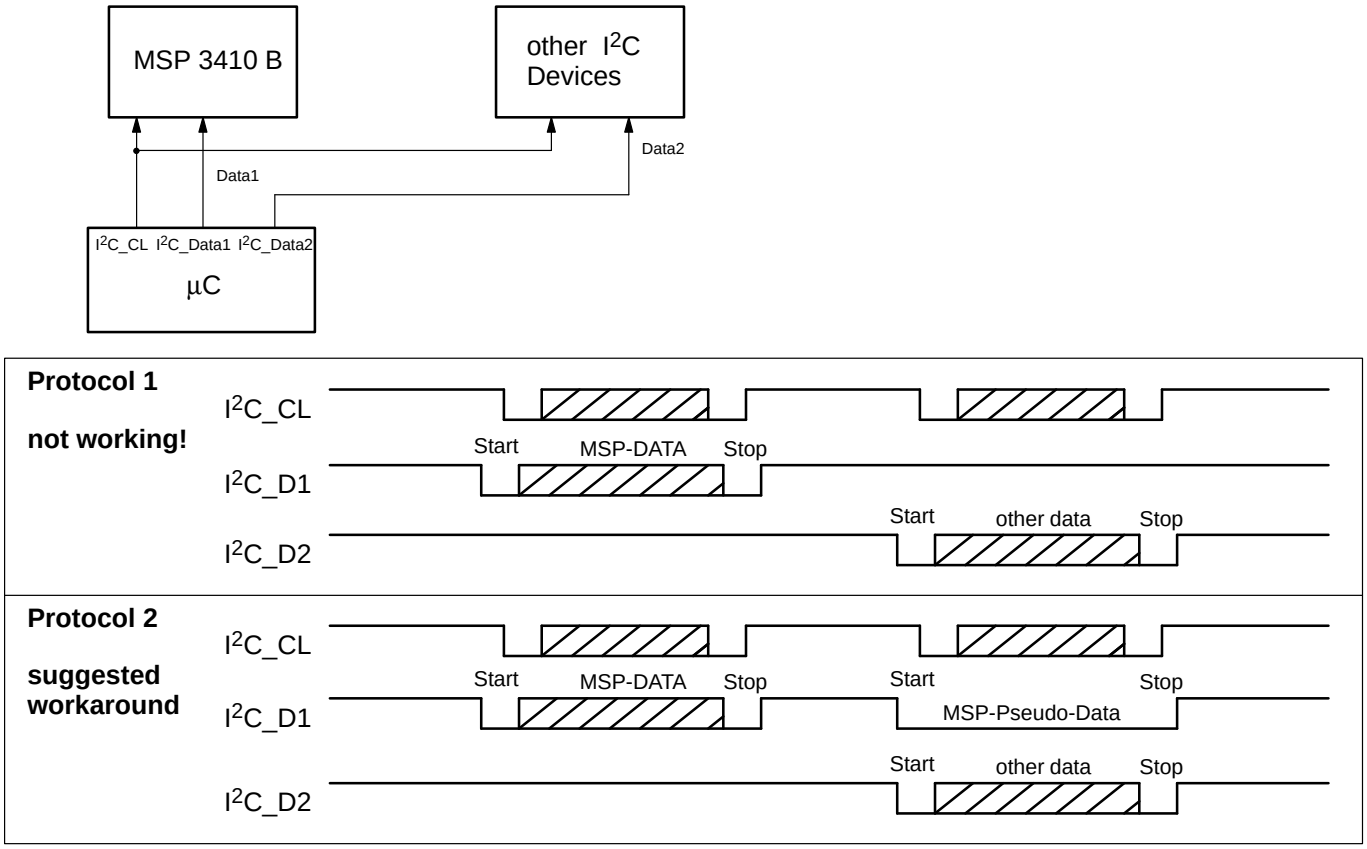
– Fig. 4–3: changes have been made to improve comprehension

20. APPENDIX C: Documentation of known hardware restrictions for TC≤15

I²C-Bus

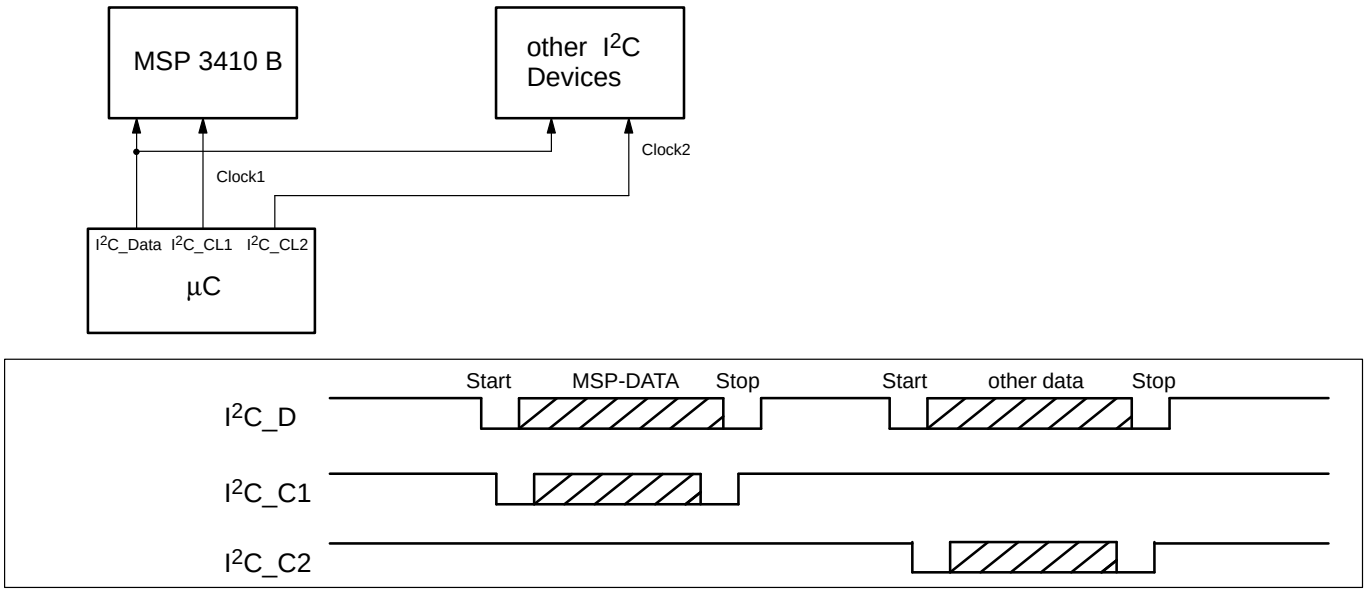
The I²C-Clock line must not be clocked in between two data transmissions (from last stop condition to next start condition). This may occur in multi bus I²C-systems with shared clock line (s. Figure 1), if protocol 1 is applied. As a preliminary workaround we recommend using protocol 2.

Figure 1



No problem was found in multi bus I²C-systems with shared data line and multiple clock lines (s. Figure 2):

Figure 2



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