NOVEMBER 2014

1Mx8 LOW VOLTAGE, ULTRA LOW POWER CMOS STATIC RAM

KEY FEATURES

- High-speed access time: 45ns, 55ns
- CMOS low power operation
  – 36 mW (typical) operating
  – 12 µW (typical) CMOS standby
- TTL compatible interface levels
- Single power supply
  –1.65V-2.2V VDD (62/65WV10248EALL)
  – 2.2V-3.6V VDD (62/65WV10248EBLL)
- Data control for upper and lower bytes
- Automotive temperature (-40°C to +125°C)
- Lead-free available

DESCRIPTION

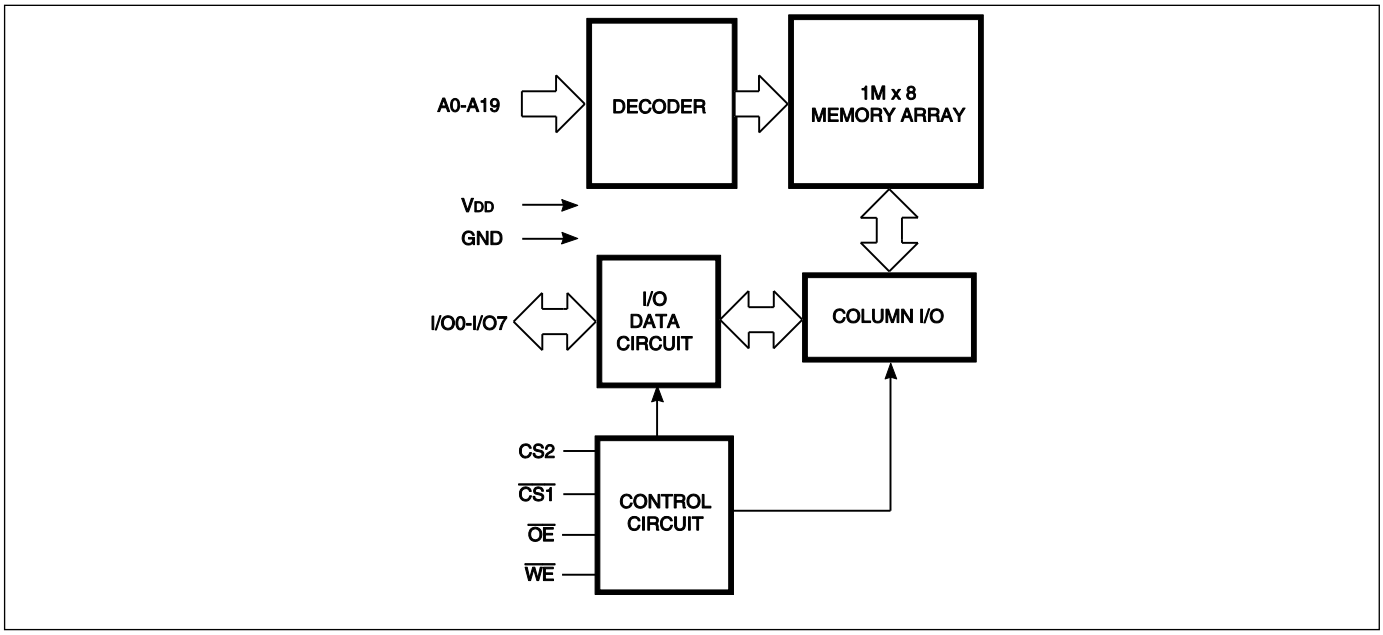
The ISSI IS62WV10248EALL/ IS62WV10248EBLL are high-speed, 8M bit static RAMs organized as 1M words by 8 bits. It is fabricated using ISSI's high-performance CMOS technology. This highly reliable process coupled with innovative circuit design techniques, yields high-performance and low power consumption devices.

When $\overline{CS1}$ is HIGH (deselected) or when CS2 is low (deselected), the device assumes a standby mode at which the power dissipation can be reduced down with CMOS input levels.

Easy memory expansion is provided by using Chip Enable and Output Enable inputs. The active LOW Write Enable ($\overline{WE}$) controls both writing and reading of the memory.

The IS62WV10248EALL and IS62WV10248EBLL are packaged in the JEDEC standard 48-pin mini BGA (6mm x 8mm) and 44-Pin TSOP (TYPE II).

BLOCK DIAGRAM



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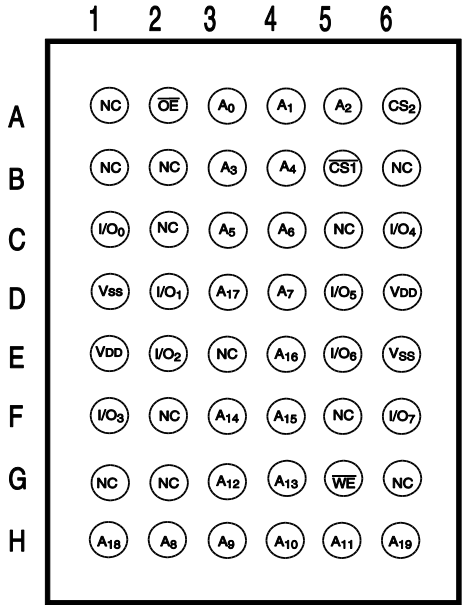
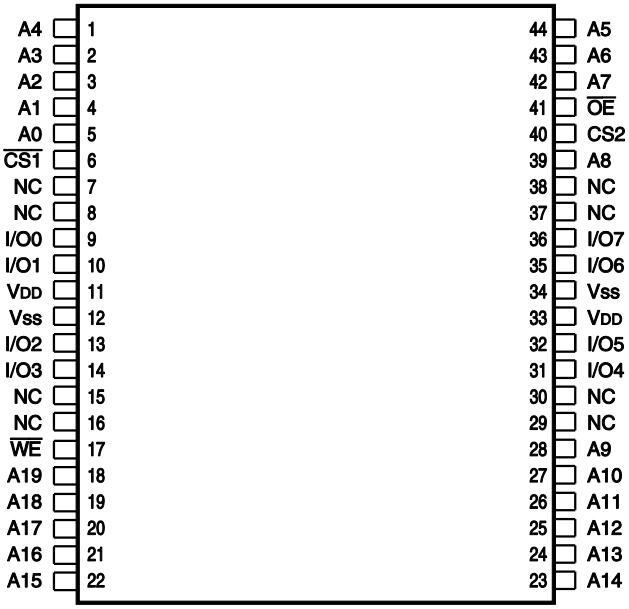
a.) the risk of injury or damage has been minimized;
b.) the user assume all such risks; and
c.) potential liability of Integrated Silicon Solution, Inc is adequately protected under the circumstances

PIN CONFIGURATIONS (1Mx8)

48-pin mini BGA (B) (6mm x 8mm)



44-Pin TSOP (Type II)



PIN DESCRIPTIONS

A0-A19	Address Inputs
$\overline{CS1}$	Chip Enable 1 Input
CS2	Chip Enable 2 Input
$\overline{OE}$	Output Enable Input
$\overline{WE}$	Write Enable Input
I/O0-I/O7	Input/Output
NC	No Connection
VDD	Power
Vss	Ground

FUNCTION DESCRIPTION

SRAM is one of random access memories. Each byte has an address and can be accessed randomly. SRAM has three different modes supported. Each function is described below with Truth Table.

STANDBY MODE

Device enters standby mode when deselected ($\overline{CS1}$ HIGH or CS2 LOW). The input and output pins (I/O0-7) are placed in a high impedance state. The current consumption in this mode will be either ISB1 or ISB2 depending on the input level. CMOS input in this mode will maximize saving power.

WRITE MODE

Write operation issues with Chip selected ($\overline{CS1}$ LOW and CS2 HIGH) and Write Enable ($\overline{WE}$) input LOW. The input and output pins(I/O0-7) are in data input mode. Output buffers are closed during this time even if $\overline{OE}$ is LOW.

READ MODE

Read operation issues with Chip selected ($\overline{CS1}$ LOW and CS2 HIGH) and Write Enable ($\overline{WE}$) input HIGH. When $\overline{OE}$ is LOW, output buffer turns on to make data output. Any input to I/O pins during READ mode is not permitted.

In the READ mode, output buffers can be turned off by pulling $\overline{OE}$ HIGH. In this mode, internal device operates as READ but I/Os are in a high impedance state. Since device is in READ mode, active current is used.

TRUTH TABLE

Mode	$\overline{WE}$	$\overline{CS1}$	CS2	$\overline{OE}$	I/O Operation	VDD Current
Not Selected	X	H	X	X	High-Z	ISB1, ISB2
(Power-down)	X	X	L	X	High-Z	ISB1, ISB2
Output Disabled	H	L	H	H	High-Z	Icc
Read	H	L	H	L	Dout	Icc
Write	L	L	H	X	Din	Icc

ABSOLUTE MAXIMUM RATINGS AND OPERATING RANGE

ABSOLUTE MAXIMUM RATINGS(1)

Symbol	Parameter	Value	Unit
Vterm	Terminal Voltage with Respect to GND	–0.2 to +3.9(V_{DD}+0.3V)	V
tBIAS	Temperature Under Bias	–55 to +125	°C
V_{DD}	V_{DD} Related to GND	–0.2 to +3.9(V_{DD}+0.3V)	V
tStg	Storage Temperature	–65 to +150	°C
I_{OUT}	DC Output Current (LOW)	20	mA

Notes:

Stress greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

OPERATING RANGE(1)

Range	Device Marking	Ambient Temperature	VDD(min)	VDD(typ)	VDD(max)
Commercial	IS62WV10248EALL	0°C to +70°C	1.65V	1.8V	2.2V
Industrial	IS62WV10248EALL	-40°C to +85°C	1.65V	1.8V	2.2V
Automotive	IS65WV10248EALL	-40°C to +125°C	1.65V	1.8V	2.2V
Commercial	IS62WV10248EBLL	0°C to +70°C	2.2V	3.3V	3.6V
Industrial	IS62WV10248EBLL	-40°C to +85°C	2.2V	3.3V	3.6V
Automotive	IS65WV10248EBLL	-40°C to +125°C	2.2V	3.3V	3.6V

Note:

1. Full device AC operation assumes a 100 µs ramp time from 0 to Vcc(min) and 200 µs wait time after Vcc stabilization.

PIN CAPACITANCE (1)

Parameter	Symbol	Test Condition	Max	Units
Input capacitance	C_{IN}	T_A = 25°C, f = 1 MHz, V_{DD} = V_{DD}(typ)	10	pF
DQ capacitance (IO0–IO7)	$C_{I/O}$		10	pF

Note:

1. These parameters are guaranteed by design and tested by a sample basis only.

THERMAL CHARACTERISTICS (1)

Parameter	Symbol	Rating	Units
Thermal resistance from junction to ambient (airflow = 1m/s)	$R_{\theta JA}$	43.22	°C/W
Thermal resistance from junction to case	$R_{\theta JC}$	13.35	°C/W

Note:

1. These parameters are guaranteed by design and tested by a sample basis only.

ELECTRICAL CHARACTERISTICS

IS62(5)WV10248EALL DC ELECTRICAL CHARACTERISTICS-I (OVER THE OPERATING RANGE)

Symbol	Parameter	Test Conditions	Min.	Max.	Unit
V_{OH}	Output HIGH Voltage	I_{OH} = -0.1 mA	1.4	—	V
V_{OL}	Output LOW Voltage	I_{OL} = 0.1 mA	—	0.2	V
V_{IH}(1)	Input HIGH Voltage		1.4	V_{DD} + 0.2	V
V_{IL}(1)	Input LOW Voltage		–0.2	0.4	V
I_{LI}	Input Leakage	GND < V_{IN} < V_{DD}	–1	1	µA
I_{LO}	Output Leakage	GND < V_{IN} < V_{DD}, Output Disabled	–1	1	µA

Notes:
1. VILL(min) = -1.0V AC (pulse width < 10ns). Not 100% tested.
   VIHH (max) = VDD + 1.0V AC (pulse width < 10ns). Not 100% tested.

IS62(5)WV10248EBLL DC ELECTRICAL CHARACTERISTICS-I (OVER THE OPERATING RANGE)

Symbol	Parameter	Test Conditions	Min.	Max.	Unit
V_{OH}	Output HIGH Voltage	2.2 ≤ V_{DD} < 2.7, I_{OH} = -0.1 mA	2.0	—	V
		2.7 ≤ V_{DD} ≤ 3.6, I_{OH} = -1.0 mA	2.4	—	V
V_{OL}	Output LOW Voltage	2.2 ≤ V_{DD} < 2.7, I_{OL} = 0.1 mA	—	0.4	V
		2.7 ≤ V_{DD} ≤ 3.6, I_{OL} = 2.1 mA	—	0.4	V
V_{IH}(1)	Input HIGH Voltage	2.2 ≤ V_{DD} < 2.7	1.8	V_{DD} + 0.3	V
		2.7 ≤ V_{DD} ≤ 3.6	2.2	V_{DD} + 0.3	V
V_{IL}(1)	Input LOW Voltage	2.2 ≤ V_{DD} < 2.7	–0.3	0.6	V
		2.7 ≤ V_{DD} ≤ 3.6	–0.3	0.8	V
I_{LI}	Input Leakage	GND < V_{IN} < V_{DD}	–1	1	µA
I_{LO}	Output Leakage	GND < V_{IN} < V_{DD}, Output Disabled	–1	1	µA

Notes:
1. VILL(min) = -2.0V AC (pulse width < 10ns). Not 100% tested.
   VIHH (max) = VDD + 2.0V AC (pulse width < 10ns). Not 100% tested.

IS62(5)WV10248EALL DC ELECTRICAL CHARACTERISTICS-II FOR POWER (OVER THE OPERATING RANGE)

Symbol	Parameter	Test Conditions	Grade	Typ.	Max.	Unit
ICC	V_{DD} Dynamic Operating Supply Current	$V_{DD}=V_{DD}(max)$, I_{OUT}=0mA, f=f_{MAX}	Com.	-	12	mA
			Ind.	-	15	
			Auto.	-	15	
ICC1	V_{DD} Static Operating Supply Current	$V_{DD}=V_{DD}(max)$, I_{OUT} = 0mA, f=0Hz	Com.	-	6	mA
			Ind.	-	6	
			Auto.	-	6	
ISB1	CMOS Standby Current (CMOS Inputs)	$V_{DD}=V_{DD}(max)$, (1) 0V ≤ CS2 ≤ 0.2V or (2) $\overline{CS1}$ ≥ V_{DD} - 0.2V, CS2 ≥ V_{DD} - 0.2V	Com.	-	20	µA
			Ind.	-	25	µA
			Auto.	-	50	µA

Note:
Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at VDD = VDD(typ), TA = 25°C

IS62(5)WV10248EBLL DC ELECTRICAL CHARACTERISTICS-II FOR POWER (OVER THE OPERATING RANGE)

Symbol	Parameter	Test Conditions	Grade	Typ.	Max.	Unit
ICC	V_{DD} Dynamic Operating Supply Current	$V_{DD}=V_{DD}(max)$, I_{OUT}=0mA, f=f_{MAX}	Com.	-	15	mA
			Ind.	-	15	
			Auto.	-	15	
ICC1	V_{DD} Static Operating Supply Current	$V_{DD}=V_{DD}(max)$, I_{OUT} = 0mA, f=0Hz	Com.	-	6	mA
			Ind.	-	6	
			Auto.	-	6	
ISB1	CMOS Standby Current (CMOS Inputs)	$V_{DD}=V_{DD}(max)$, (1) 0V ≤ CS2 ≤ 0.2V or (2) $\overline{CS1}$ ≥ V_{DD} - 0.2V, CS2 ≥ V_{DD} - 0.2V	Com.	-	20	µA
			Ind.	-	25	µA
			Auto.	-	50	µA

Note:
Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at VDD = VDD(typ), TA = 25℃

AC TEST CONDITIONS (OVER THE OPERATING RANGE)

Parameter	Symbol	Conditions	Units
Input Rise Time	T_R	1.0	V/ns
Input Fall Time	T_F	1.0	V/ns
Output Timing Reference Level	V_{REF}	½ V_{TM}	V
Output Load Conditions	Refer to Figure 1 and 2		

OUTPUT LOAD CONDITIONS FIGURES

Figure1

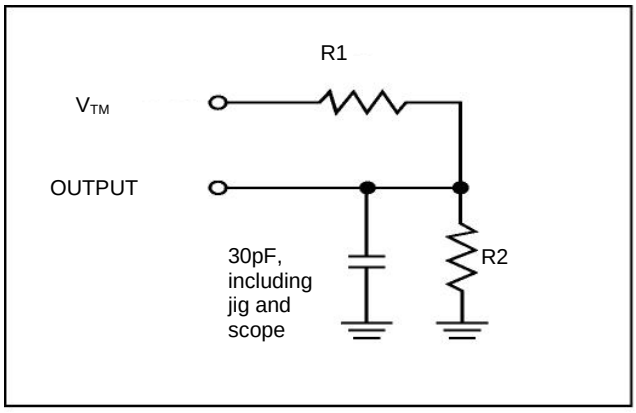
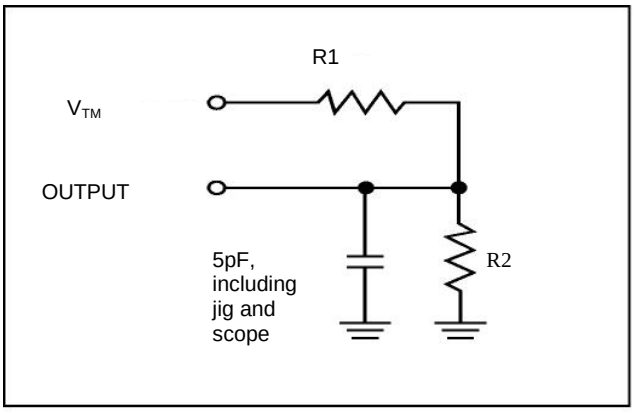


Figure2



Parameters	V_{DD}=1.65~1.98V	V_{DD}=2.2~2.7V	V_{DD}=2.7~3.6V
R1	13500Ω	16667Ω	1103Ω
R2	10800Ω	15385Ω	1554Ω
V_{TM}	VDD	VDD	VDD

AC CHARACTERISTICS[6] (OVER OPERATING RANGE)

READ CYCLE AC CHARACTERISTICS

Parameter	Symbol	45ns		55ns		unit	notes
		Min	Max	Min	Max		
Read Cycle Time	tRC	45	-	55	-	ns	1,5
Address Access Time	tAA	-	45	-	55	ns	1
Output Hold Time	tOHA	8	-	8	-	ns	1
$\overline{CS1}$, CS2 Access Time	tACS1/tACS2	-	45	-	55	ns	1
$\overline{OE}$ Access Time	tDOE	-	22	-	25	ns	1
$\overline{OE}$ to High-Z Output	tHZOE	-	18	-	18	ns	2
$\overline{OE}$ to Low-Z Output	tLZOE	5	-	5	-	ns	2
$\overline{CS1}$, CS2 to High-Z Output	tHZCS/tHZCS2	-	18	-	18	ns	2
$\overline{CS1}$, CS2 to Low-Z Output	tLZCS/tLZCS2	10	-	10	-	ns	2

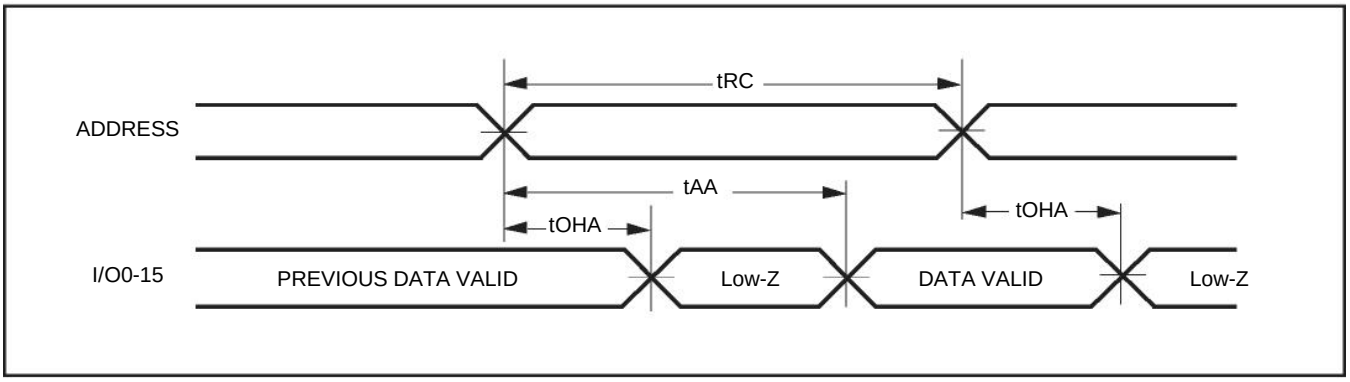
WRITE CYCLE AC CHARACTERISTICS

Parameter	Symbol	45ns		55ns		unit	notes
		Min	Max	Min	Max		
Write Cycle Time	tWC	45	-	55	-	ns	1,3,5
$\overline{CS1}$,CS2 to Write End	tSCS1/tSCS2	35	-	40	-	ns	1,3
Address Setup Time to Write End	tAW	35	-	40	-	ns	1,3
Address Hold from Write End	tHA	0	-	0	-	ns	1,3
Address Setup Time	tSA	0	-	0	-	ns	1,3
$\overline{WE}$ Pulse Width	tPWE	35	-	40	-	ns	1,3,4
Data Setup to Write End	tSD	28	-	28	-	ns	1,3
Data Hold from Write End	tHD	0	-	0	-	ns	1,3
$\overline{WE}$ LOW to High-Z Output	tHZWE	-	18	-	18	ns	2,3
$\overline{WE}$ HIGH to Low-Z Output	tLZWE	10	-	10	-	ns	2,3

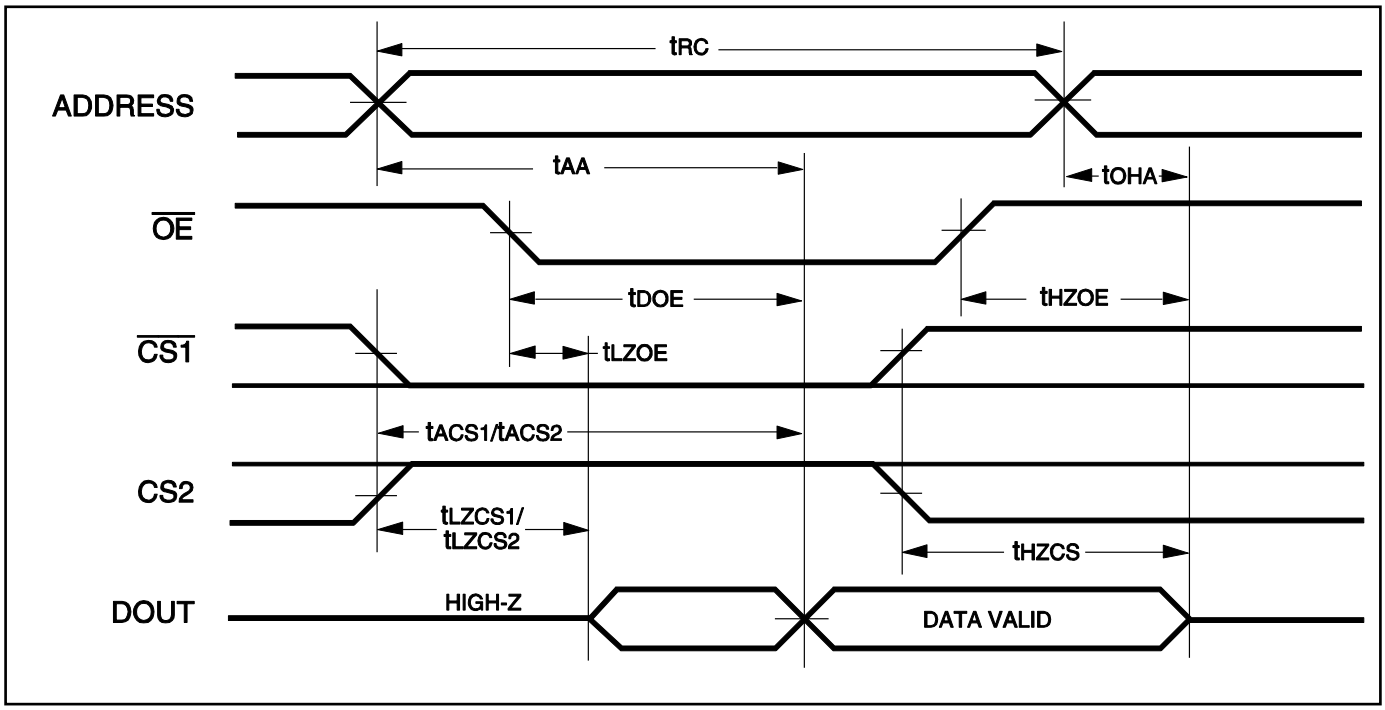
Notes:
1. Tested with the load in Figure 1.
2. Tested with the load in Figure 2. tHZOE, tHZCS and tHZWE transitions are measured when the output enters a high impedance state. Not 100% tested.
3. The internal write time is defined by the overlap of $\overline{CS1}$=LOW, CS2=HIGH and $\overline{WE}$=LOW. All four conditions must be in valid states to initiate a Write, but any condition can go inactive to terminate the Write. The Data Input Setup and Hold timing are referenced to the rising or falling edge of the signal that terminates the write.
4. tPWE > tHZWE + tSD when OE is LOW.
5. Address inputs must meet V_{IH} and V_{IL} SPEC during this period. Any glitch or unknown inputs are not permitted. Unknown input with standby mode is acceptable.
6. Data retention characteristics are defined later in DATA RETENTION CHARACTERISTICS.

TIMING DIAGRAM

READ CYCLE NO. 1[1,2] (ADDRESS CONTROLLED) ($\overline{CS1}$=$\overline{OE}$=V_{IL}, CS2=$\overline{WE}$=V_{IH})

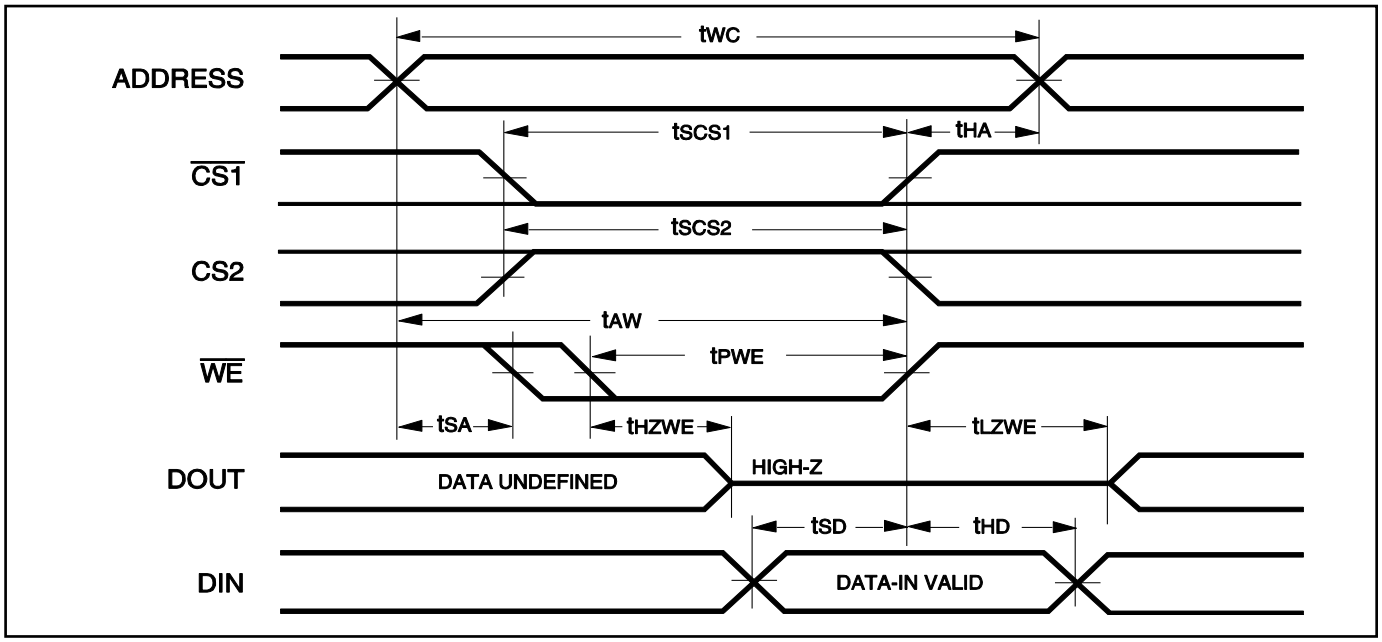


READ CYCLE NO. 2[1,3] ($\overline{CS1}$, CS2, AND $\overline{OE}$ CONTROLLED)



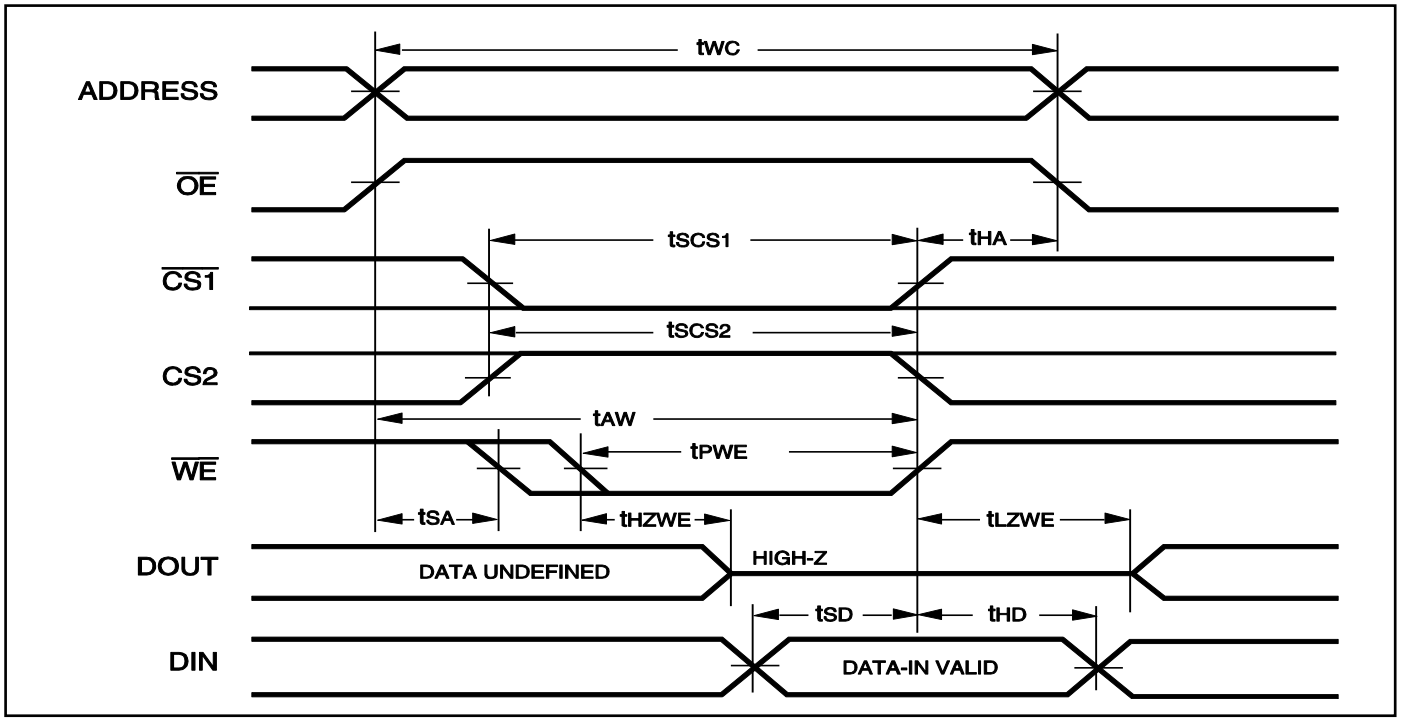
Notes:
1. $\overline{WE}$ is HIGH for a Read Cycle.
2. The device is continuously selected. $\overline{OE}$, $\overline{CS1}$= Vil. CS2=$\overline{WE}$=V_{IH}.
3. Address is valid prior to or coincident with $\overline{CS1}$ LOW and CS2 HIGH transition.

WRITE CYCLE NO. 1 ($\overline{CS1}$ CONTROLLED, $\overline{OE}$ = HIGH OR LOW)



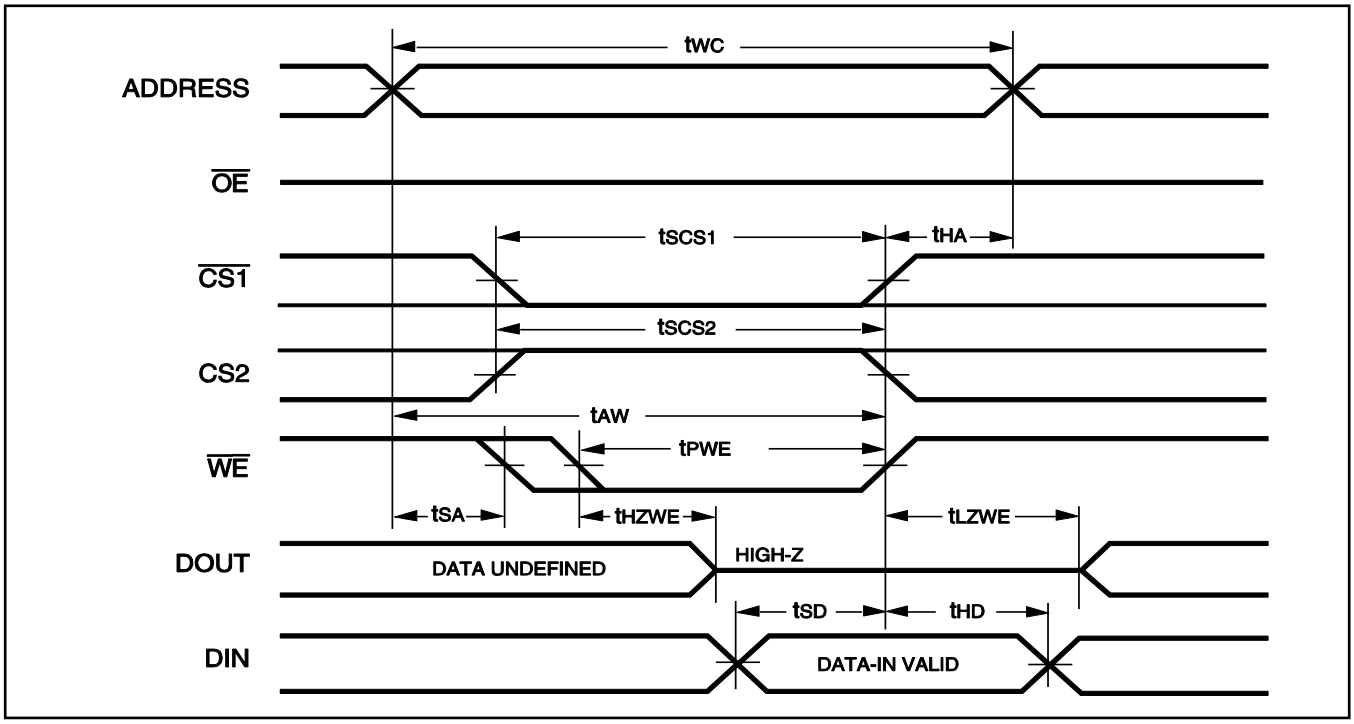
Notes:
1. tHZWE is based on the assumption when tSA=0nS after READ operation. Actual DOUT for tHZWE may not appear if $\overline{OE}$ goes high before Write Cycle. tHZOE is the time DOUT goes to High-Z after $\overline{OE}$ goes high.
2. During this period the I/Os are in output state. Do not apply input signals.

WRITE CYCLE NO. 2 ($\overline{WE}$ Controlled: $\overline{OE}$ is HIGH During Write Cycle)



Notes:
1. tHZWE is based on the assumption when tSA=0nS after READ operation. Actual DOUT for tHZWE may not appear if $\overline{OE}$ goes high before Write Cycle. tHZOE is the time DOUT goes to High-Z after goes high.
2. During this period the I/Os are in output state. Do not apply input signals

WRITE CYCLE NO. 3 ($\overline{WE}$ CONTROLLED: $\overline{OE}$ IS LOW DURING WRITE CYCLE)



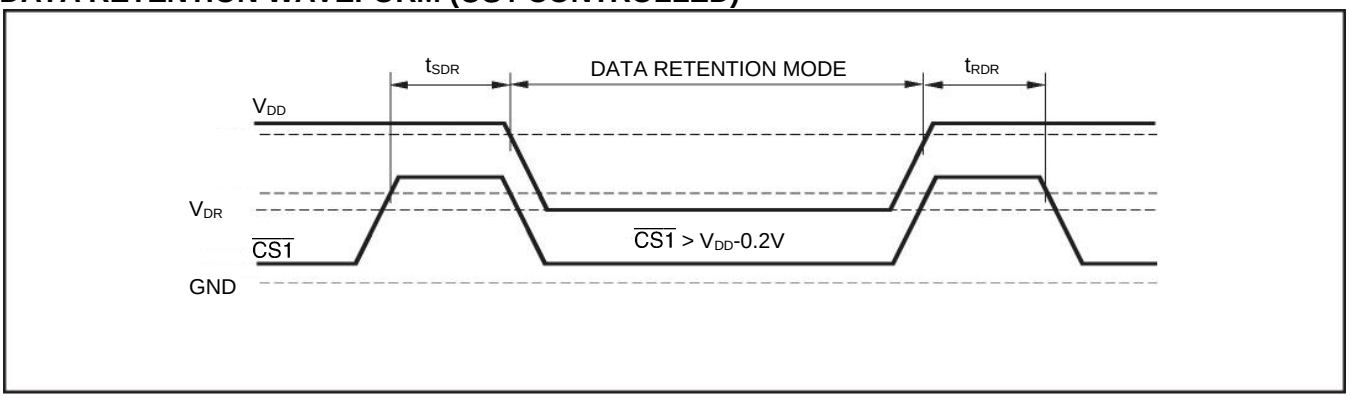
Notes:
If $\overline{OE}$ is low during write cycle, tHZWE must be met in the application. Do not apply input signal during this period. Data output from the previous READ operation will drive IO BUS.

DATA RETENTION CHARACTERISTICS

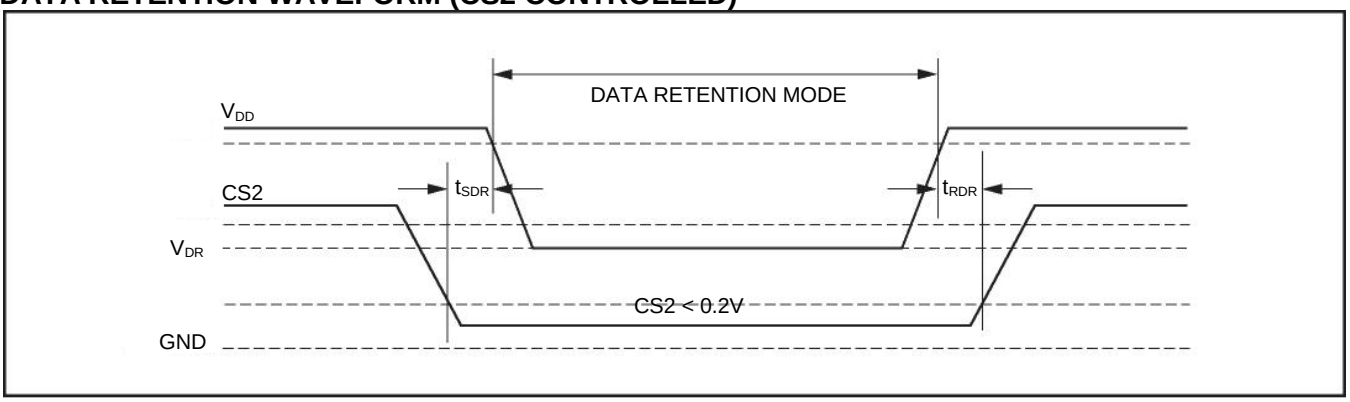
Symbol	Parameter	Test Condition	OPTION	Min.	Typ.(1)	Max.	Unit
V_{DR}	V_{DD} for Data Retention	See Data Retention Waveform	IS62(5)WV10248EALL	1.5		-	V
			IS62(5)WV10248EBLL	1.5		-	V
I_{DR}	Data Retention Current	V_{DD}= V_{DR}(min), (1) 0V ≤ CS2 ≤ 0.2V, or (2) $\overline{CS1}$ ≥ V_{DD} – 0.2V, CS2 ≥ V_{DD} - 0.2V	Com.	-	-	20	uA
			Ind.	-	-	25	
			Auto	-	-	50	
t_{SDR}	Data Retention Setup Time	See Data Retention Waveform		0	-	-	ns
t_{RDR}	Recovery Time	See Data Retention Waveform		tRC	-	-	ns

Note:
1. Typical values are measured at VDD=VDR(min), TA = 25℃ and not 100% tested.

DATA RETENTION WAVEFORM ($\overline{CS1}$ CONTROLLED)



DATA RETENTION WAVEFORM (CS2 CONTROLLED)



ORDERING INFORMATION
IS62WV10248EALL (1.65V - 2.2V)

Industrial Range: –40°C to +85°C

Speed (ns)	Order Part No.	Package
55	IS62WV10248EALL-55TI	TSOP-II
	IS62WV10248EALL-55TLI	TSOP-II, Lead-free
	IS62WV10248EALL-55BI	mini BGA
	IS62WV10248EALL-55BLI	mini BGA, Lead-free

IS62WV10248EBLL (2.2V - 3.6V)

Industrial Range: –40°C to +85°C

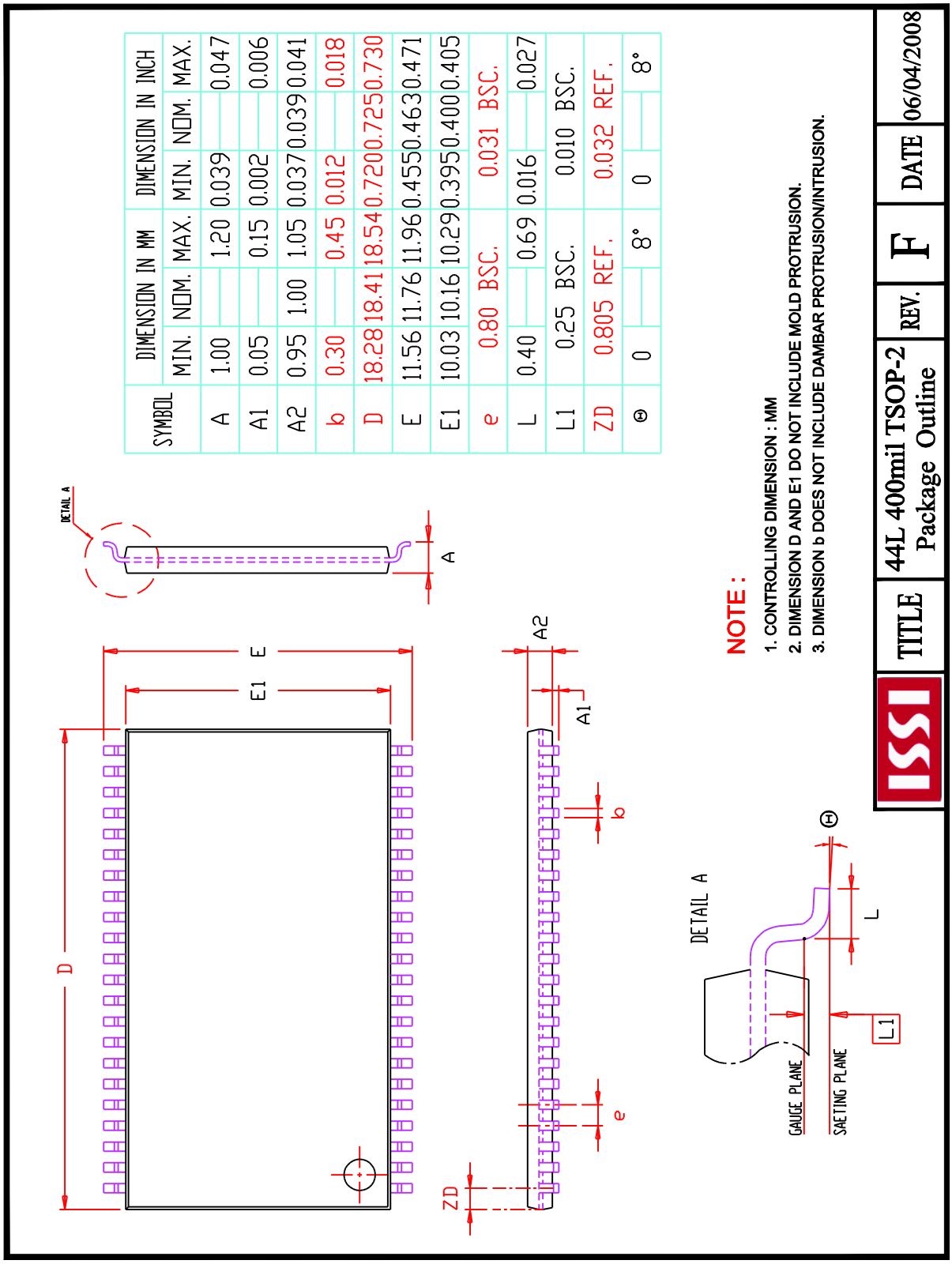
Speed (ns)	Order Part No.	Package
45	IS62WV10248EBLL-45TI	TSOP-II
	IS62WV10248EBLL-45TLI	TSOP-II, Lead-free
	IS62WV10248EBLL-45BI	mini BGA
	IS62WV10248EBLL-45BLI	mini BGA, Lead-free
55	IS62WV10248EBLL-55TI	TSOP-II
	IS62WV10248EBLL-55TLI	TSOP-II, Lead-free
	IS62WV10248EBLL-55BI	mini BGA
	IS62WV10248EBLL-55BLI	mini BGA, Lead-free

IS65WV10248EBLL (2.2V - 3.6V)

Automotive Range: –40°C to +125°C

Speed (ns)	Order Part No.	Package
45	IS65WV10248EBLL-45CTLA3	TSOP-II, Lead-free, Copper Lead-frame

PACKAGE INFORMATION



PACKAGE INFORMATION